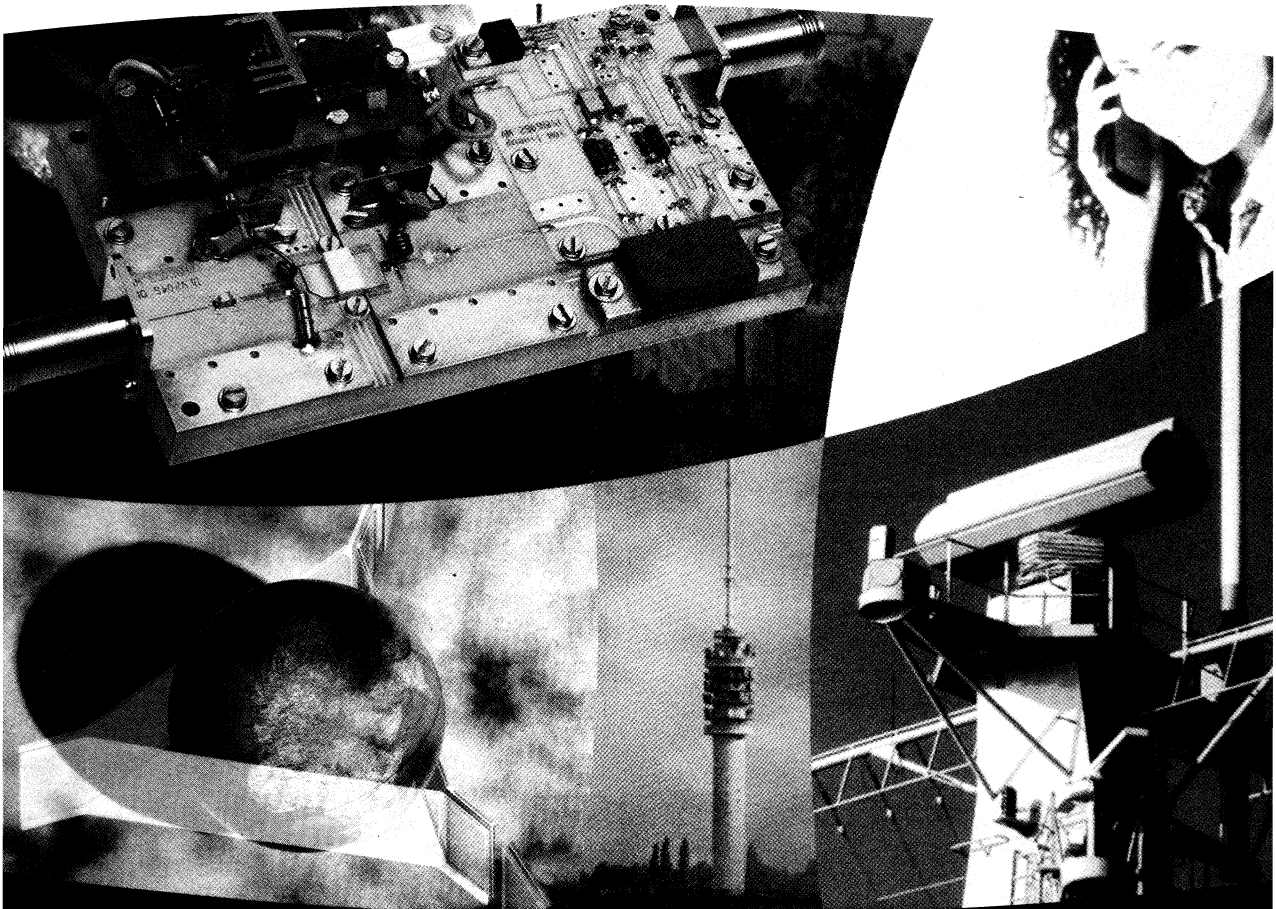
SCRETE SEMICONDUCTORS

RF & Microwave Power Transistors and Circulators/Isolators

Application Handbook SC19b
1998



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SC19B - IMPROVED APPLICATION SUPPORT

Dear Reader,

This book (SC19b) is a major revision of Philips Application Reports Handbook. A significant improvement on the previous version is the addition of a comprehensive section covering the basic design of RF transmitting transistors and amplifiers. Compiled and indexed to provide easy access to individual subjects, this section (Part 1) is intended as a practical reference and reminder of the most important design considerations.

Part 2 is a compilation of application reports covering broadcast, cellular and radar (pulse-microwave) applications. These reports can lessen the work of the engineer designing and prototyping driver and output stages of professional transmitters.

For up-to-date product data, consult RF Power Data Handbook SC19a and, of course, visit our Internet site regularly.

If you have any questions or comment on either book, don't hesitate to contact the Philips representative in your country (address on back cover), or myself.

Volker van Hoorn
International Product Marketing Manager
RF Power Transistors
PG Discrete Semiconductors Nijmegen
Philips Semiconductors
Gerstweg 2, Building BZ1.047
6534 AE Nijmegen
The Netherlands

Fax. +31-(0)24-3532901

RF & Microwave Power Transistors and Circulators/Isolators

CONTENTS

READ THIS FIRST

This publication is divided into two main parts. The first, *'RF transmitting transistor and power amplifier fundamentals'* describes the basic design of an RF transmitting transistor, and how to interpret the published transistor data. Part 1 also describes the main types of amplifier and the fundamental design considerations (biasing, impedance matching, input/output compensation, interstage networks) to obtain the optimum performance from our products.

For those new to transmitting transistors and amplifier design, Part 1 provides a good all-round introduction. Experienced designers will probably prefer to refer to individual sections of Part 1 as needed. Note, the application reports referred to in Part 1 can be found in Part 2.

FINDING THE INFORMATION YOU NEED

Part 2, *'Application reports'*, provides extensive application information from Philips' System Laboratories to help you design-in our transistors. We have arranged the reports to enable you to find relevant information quickly, grouping them for base station, broadcast & general and microwave applications with further classification according to frequency.

ACKNOWLEDGEMENT

The marketing staff of Philips' Product Group Discrete Semiconductors Nijmegen,
The Netherlands would like to thank all who have contributed to this book with information, suggestion and criticism.
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PART 1

RF transmitting transistor and power amplifier fundamentals

CONTENTS

1 TRANSMITTING TRANSISTOR DESIGN

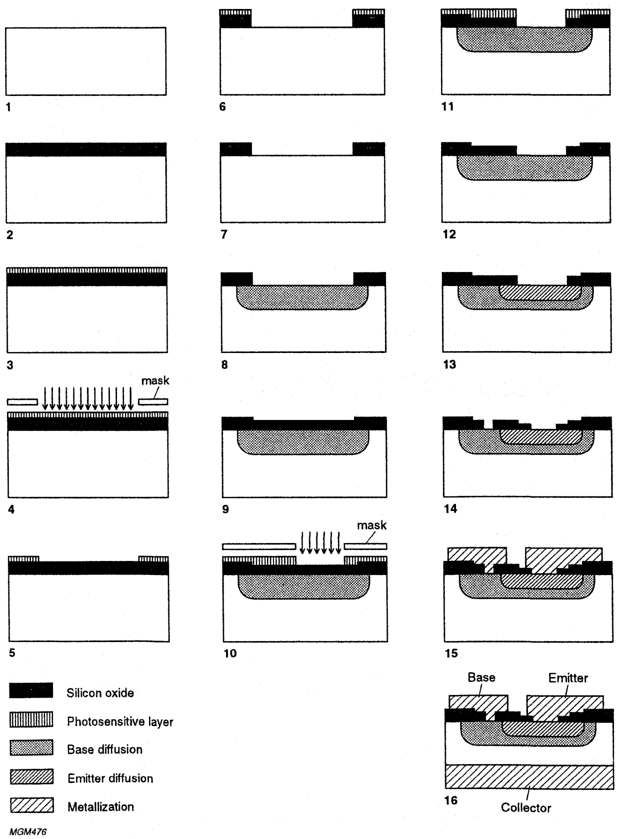
1.1 Die technology and design

A transmitting transistor has to deliver high power at high frequency (>1 MHz). This means that a large transistor die with a fine structure is required. Bipolar and MOS transistors are suitable, see panel, and Philips Semiconductors' portfolio includes both types. Their relative merits are summarized later in this section. First, however, let's look at the basic aspects of design that contribute to the reliability and high-performance of a modern RF transmitting transistor.

TRANSISTOR FABRICATION

As is well-known, most transistors are fabricated from silicon wafers (5" dia. or larger, and about 0.25 mm thick) in a multi-stage batch process that involves precise, localized doping of an epitaxial layer grown on the silicon substrate to form the different transistor regions. The main process steps for fabricating bipolar transistors are shown here as a reminder. MOS transistors are fabricated using similar techniques. Though semiconductor manufacturers have many processes available to meet different commercial and technical specifications, they all are based on the principles outlined below.

1. Silicon wafer
2. Oxidize to form oxide layer
3. Apply photosensitive layer
4. Expose through high-resolution mask
5. Develop photosensitive layer
6. Etch base window through oxide layer
7. Remove remaining photosensitive layer
8. Diffuse or ion-implant the base
9. Oxidize base window
10. Expose emitter window
11. Etch emitter window through oxide layer
12. Remove remaining photosensitive layer
13. Diffuse or ion-implant the emitter
14. Create metallization window
15. Metallize base and emitter regions
16. Polish and metallize bottom (collector).



1.1.1 *Bipolar transistor dies*

1.1.1.1 THE COLLECTOR (SUBSTRATE MATERIAL)

All of Philips' present bipolar types are NPN silicon planar epitaxial transistors, see Figs 1-1 and 1-2. The basic epitaxial material consists of a highly doped n-substrate (100 to 200 μm thick) with a rather high ohmic n-layer (epi-layer) deposited on top. The resistivity of this layer determines the collector-base breakdown voltage of the device ($V_{(BR)CBO}$). Most Philips transistors intended for operation at a supply voltage of 28 V have a *guaranteed* breakdown voltage of 65 V (and a typical value of about 80 V). The required resistivity of the epi-layer for this breakdown voltage is 1.6 to 2.0 Ωcm, the exact value having a very small tolerance.

A second important design parameter is the epi-layer thickness, which must be thicker than the collector depletion layer thickness at breakdown to prevent reverse second breakdown when the base current is negative. This occurs when the collector voltage is higher than the collector-emitter breakdown voltage with open base, $V_{(BR)CEO}$. Normally, this voltage is about half the collector-base breakdown voltage mentioned earlier. When the collector voltage is between these two collector breakdown voltages ($V_{(BR)CBO}$ and $V_{(BR)CEO}$), the situation is as shown in Fig.1-3.

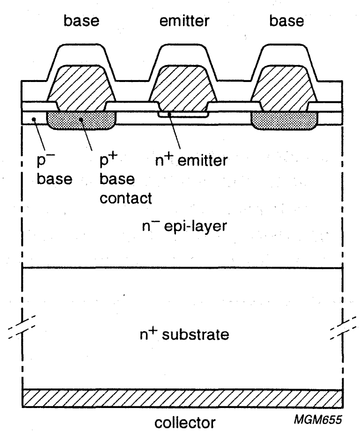


Fig.1-1 Cross-section of a bipolar transmitting transistor.

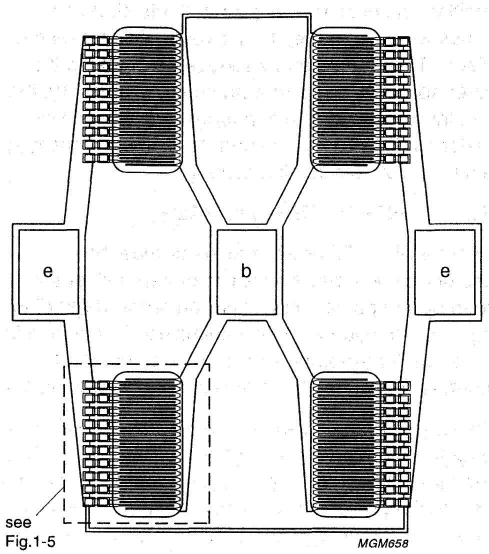


Fig.1-2 Layout of a typical bipolar transmitting transistor die.

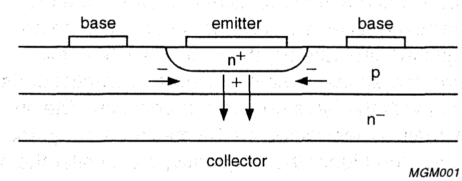


Fig.1-3 When the collector voltage is between $V_{(BR)CBO}$ and $V_{(BR)CEO}$, very high current densities are formed under the emitter. The arrows indicate the direction of electron current.

As Fig.1-3 shows, the collector current is concentrated in the middle of the emitter which can lead to very high current densities. The base is negative along the edge of the emitter and positive beneath it. If this situation continues for a long time, it will eventually destroy the transistor. This effect can be reduced by making the epi-layer somewhat thicker than strictly necessary, the chosen thickness being a compromise between the transistor's RF performance and its ability to withstand certain forms of output mismatching.

1.1.1.2 THE EMITTER AND BASE

The emitter of an RF power transistor must be dimensioned such that the transistor can deliver the required output power with all performance-degrading effects such as capacitances minimized. To achieve this, both the emitter area and periphery are important parameters, because of 'emitter-crowding', see Fig.1-4.

The base (electron) current makes the base positive along the edge of the emitter but negative in the middle. This means that collector current only flows at the edge of the emitter, so the potential output power is mainly determined by the emitter periphery. Under normal operating conditions, only 1 to 2 µm of the edge of the emitter is active; the rest of the emitter merely introduces parasitic capacitance. A practical choice for emitter width is 2 to 4 µm.

For a 2 to 4 µm wide emitter, a good design rule of thumb is that every watt of output power requires about 2 mm of emitter periphery. A narrower emitter can improve some characteristics, but requires more emitter periphery per watt.

Of course, it is not very practical to make one extremely long, narrow emitter, so transistor designers use an interdigitated structure as shown in Fig.1-5. In this structure, the emitter is split into several parallel parts ('fingers') with the base contacts in between. The finger pitch is mainly determined by the maximum frequency of operation - the higher the frequency, the smaller the pitch.

The emitter fingers are normally connected at one end by metallization. As a result, there is a voltage drop along each finger. This must not exceed 25 to 30 mV at maximum collector current otherwise part of the finger will be cut off near the other end.

Splitting the emitter into many sections is thus required for practical reasons and for good operation. This is also true to some extent for the base, but for different reasons. In fact, if the required output power is low, say 2 to 3 W, a single base area is acceptable. At higher powers, it is necessary to split the base area into several parts as this:

- Reduces the thermal resistance of the die
- Increases the base periphery, improving the distribution of dissipation at breakdown since collector breakdown occurs first along the edges of the base areas
- Allows more base and emitter bonding pads to be included, which reduces the emitter lead inductance, increasing the power gain. In addition, splitting the base area reduces the current through each bonding wire.

The preferred distance between successive base areas is approximately twice the die thickness, say about 300 µm, to obtain a low thermal resistance. A disadvantage of splitting the base is higher parasitic capacitances.

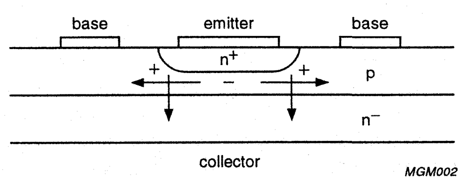


Fig.1-4 Emitter crowding effect. The arrows indicate the direction of electron current in normal operation. Note, to prevent confusion, the base current has also been drawn as an electron current.

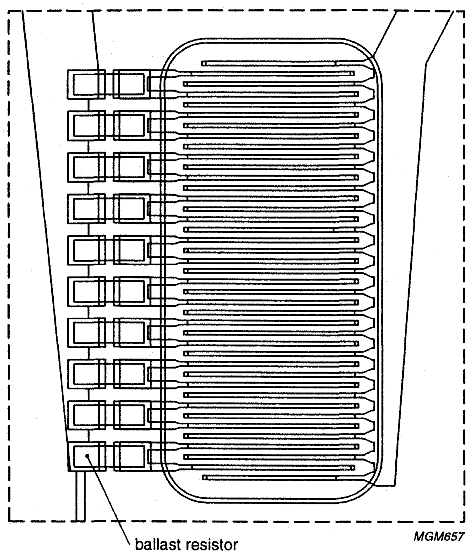


Fig.1-5 Interdigitated base-emitter structure.

1.1.1.3 EMITTER BALLAST RESISTORS

For electrical ruggedness, a built-in emitter ballast resistor is virtually a necessity. This is certainly the case when class-A or class-AB operation can be expected. In class-A for instance, without such an emitter resistor, the collector current can become restricted to a small area in the middle of the die where the temperature is highest. This causes a large increase in the thermal resistance which can destroy the transistor at a much-reduced DC power.

To prevent this effect, each emitter finger or group of two fingers, is provided with an emitter resistor. Good current distribution is obtained if the total emitter resistance is such that the voltage drop across it is approximately 200 to 300 mV at the normal DC collector current.

Emitter resistors can be made as a p^+-diffusion beside the base areas (Fig.1-6a) or as a doped polysilicon layer on top of the oxide (Fig.1-6b), the latter producing less parasitic capacitance.

The temperature coefficient (t.c.) of a diffused emitter resistance is positive, and at practical operating temperatures (~125 °C), the resistance increases by approximately 0.1%/K. The t.c. of a polysilicon resistor is much smaller.

1.1.1.4 DIFFUSION AND IMPLANTATION PROCESSES

The first transmitting transistors were made using diffusion processes. Nowadays, ion implantation followed by temperature treatment is the preferred manufacturing process as it provides superior reproducibility and sharper (i.e. better defined) doping transitions. The specific implantation process used depends primarily on the maximum frequency of operation required. For the highest frequency transistors, extremely shallow implantations are used, giving a thin base and a high f_T. The resulting h_{FE}, usually about 50, is ample for RF operation.

1.1.2 Vertical DMOS transistor dies

1.1.2.1 THE DRAIN (SUBSTRATE MATERIAL)

Philips' RF power MOS transistors are all silicon n-channel enhancement types, (see Fig.1-7). The considerations for and dimensioning of the epitaxial material are principally the same as those for bipolar transistors (Section 1.1.1.1).

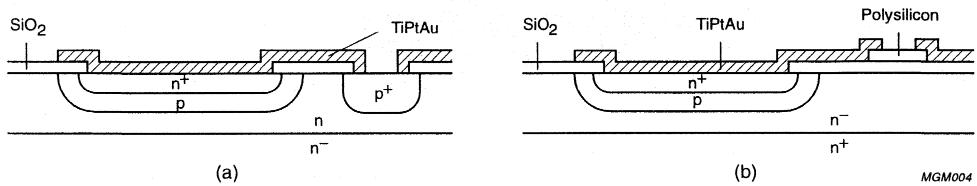


Fig.1-6 Emitter resistance formed (a) by a p+-diffusion beside the base areas, and (b) as a doped polysilicon layer on top of the oxide.

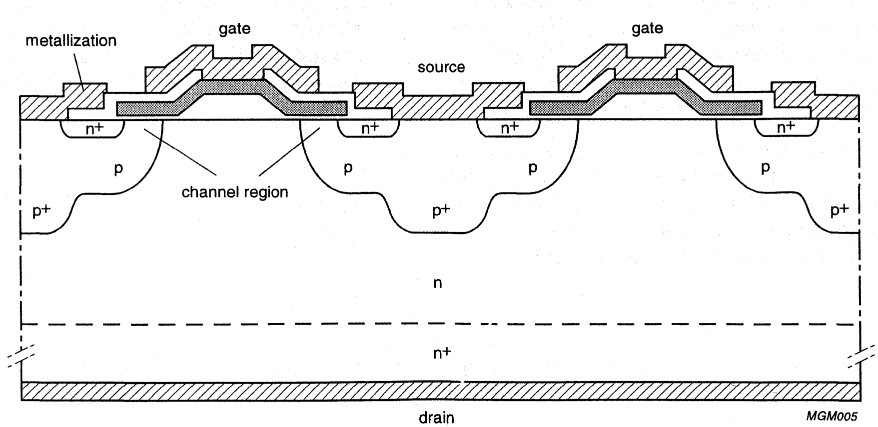


Fig.1-7 Cross-section of a vertical DMOS transmitting transistor. The *length* of the gate (the channel length) is in the plane of the paper; the channel *width* is into the plane of the paper.

1.1.2.2 THE SOURCE AND GATE

The configuration of source and gate in most MOS transmitting transistors is similar to the interdigitated emitter and base of a bipolar transistor, see Fig.1-9.

The RF output power that such a device can deliver depends of course on the maximum drain current (I_{DSX}) which, in turn, is directly proportional to the width of the gate (approximately equal to the 'channel width'). To facilitate comparison with bipolar transistors, the source periphery (virtually the same as the total channel width) is used. Dimensioning is then very similar to that of a bipolar transistor, namely 2 to 3 mm of source periphery per watt of output power.

An equivalent to the emitter ballast resistors of a bipolar transistor is not required. This is because the temperature coefficient of the drain current as a function of the gate voltage is negative at high drain currents, providing automatic protection against thermal runaway, see Fig.1-8.

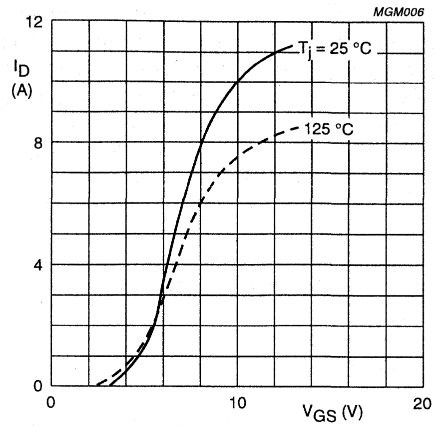


Fig.1-8 At high drain currents, the negative temperature coefficient of the drain current vs. gate voltage protects against thermal runaway.

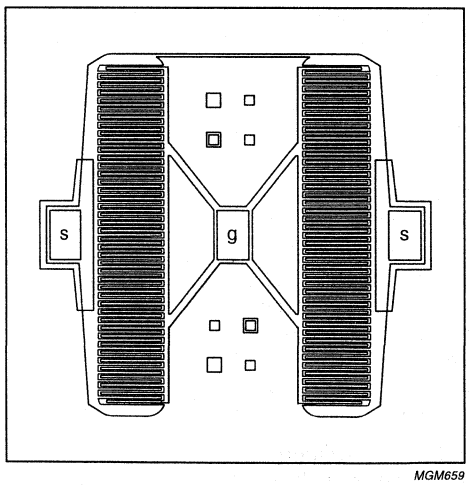


Fig.1-9 Interdigitated source and gate arrangement of a typical MOS transmitting transistor die. Die size: 1×1 mm^2.

1.1.2.3 *THE CHANNEL REGION*

As for bipolar devices, the process used to manufacture a MOS transistor is dependent on the intended maximum operating frequency. A key parameter is the length of the channel, l_{ch}, (gate) because it determines the cut-off frequency, f_T:

$$f_T = \frac{G_{fs}}{2\pi C_{is}} = \frac{V_{sat}}{4\pi l_{ch}}$$

where:

G_{fs} is the forward transconductance

C_{is} is the input capacitance

V_{sat} is the saturation velocity (for silicon: 10^7 cm/s)

and

l_{ch} is the channel (gate) length.

1.1.2.4 *COMPARISON OF VDMOS AND BIPOLAR TRANSISTORS*

Both Philips' bipolar and MOS types can provide excellent performance. At high frequencies (~1 GHz and above), bipolar transistors usually provide the best all-round performance. At lower frequencies, VDMOS devices can outperform bipolar types, e.g. on power gain, and will likely capture an increasing part of the present bipolar market as performance continues to improve.

Table 1-1 VDMOS and bipolar devices compared

ADVANTAGES OF VDMOS	DISADVANTAGES OF VDMOS
Simpler biasing circuit. This is primarily due to a MOS transistor's high input impedance, and the low and negative temperature coefficient at high drain currents.	**The gate is sensitive to electrostatic charges** so ESD protection measures must be taken.
Lower noise. This is especially important in duplex equipment and where many transceivers are operating near to each other and at similar frequencies.In one test, an improvement of 7 dB was measured at 75 MHz in similar wideband amplifiers.	**Higher output power 'slump'** (reduction of output power at high temperature). Note, this is primarily caused by decreasing transconductance.
Higher power gain (up to ~5 dB higher) than comparable bipolar types at lower frequencies. This is mainly due to the high transconductance and low feedback capacitance.	
Simple control of the output power. The output power can be controlled down to almost zero simply by reducing the DC gate-source voltage.	
Superior thermal stability owing to the negative temperature coefficient of the drain current at high levels, this is also why the current distribution over the whole active area of a VDMOS device is so good.	
Superior load mismatch tolerance - Another benefit of the superior thermal stability of a VDMOSFET.	
Lower high-order (7th and higher) intermodulation products due to the 'smoother' characteristics of MOS devices.	

1.1.3 *Lateral DMOS (LDMOS) transistor dies*

LDMOS technology is a relatively recent development. Unlike VDMOS which can be used up to about 1 GHz, LDMOS, like bipolar, is suitable for use at higher frequencies owing to its lower feedback capacitance and source inductance than VDMOS. However, depending on the particular performance and cost requirements, VDMOS, LDMOS or bipolar can provide the best solution.

1.1.3.1 THE SOURCE (SUBSTRATE MATERIAL)

Philips LDMOS transistors are all silicon n-channel enhancement types, (see Fig.1-11). The substrate is highly doped p-material, whereas the epitaxial layer is lightly doped p^--material.

1.1.3.2 THE DRAIN AND GATE

The configuration of drain and gate is fairly similar to the interdigitated emitter and base of a bipolar transistor, see Fig.1-10. Note however that *all regions, (gate, source and drain) are metallized on top of the die.* The gate and drain are connected to bonding pads, and the source is grounded to the substrate by means of a via-diffusion through the epi-layer. The benefit of this design is that a *single* metal interconnect can be used. Note, the top source metallization is solely for interconnecting the p^+ and n^+ regions; the transistor's source electrode is connected to the bottom (substrate) metallization.

As for a VDMOS device, the RF output power that an LDMOS device can deliver depends on the maximum drain current (I_{DSX}) which is directly proportional to the width of the gate (approximately equal to the 'channel width'). And, an equivalent to the emitter ballast resistors of a bipolar transistor is again not required, see Section 1.1.2.2.

1.1.3.3 THE CHANNEL REGION

As with VDMOS, a key parameter of an LDMOS transistor is the length of the channel, l_{ch} (gate) because it determines the cut-off frequency, f_T (defined as for VDMOS in Section 1.1.2.3).

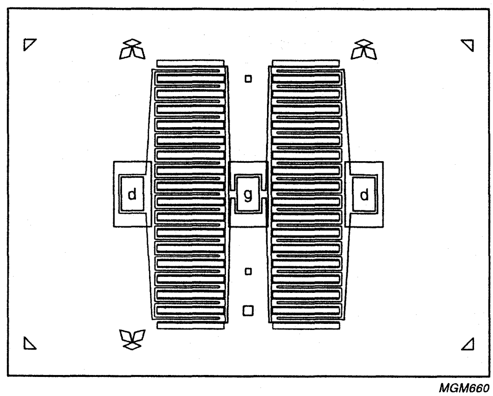


Fig.1-10 Interdigitated drain, source and gate arrangement of a typical LDMOS transmitting transistor die.
Die size: 1×0.8 mm^2.

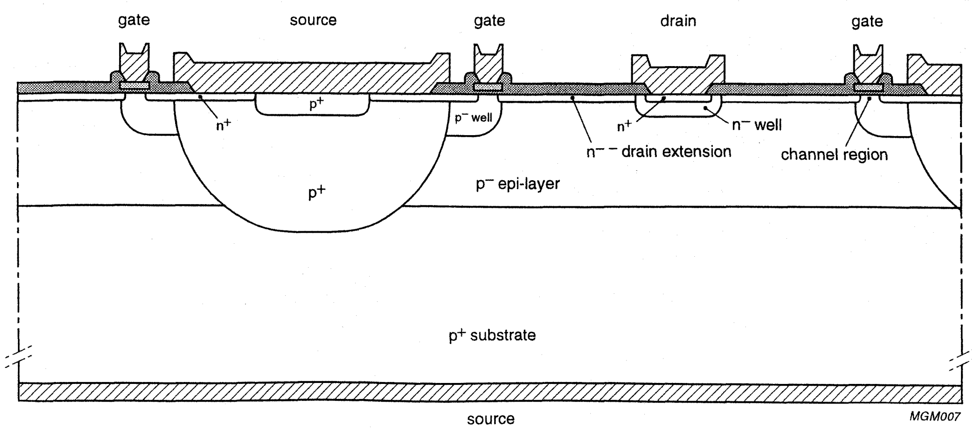


Fig.1-11 Cross-section of an LDMOS transmitting transistor. The *length* of the gate (the channel length) is in the plane of the paper; the channel *width* is into the plane of the paper.

1.1.3.4 *COMPARISON OF LDMOS AND BIPOLAR TRANSISTORS*

Both Philips' LDMOS and bipolar transistors can provide excellent performance in a variety of applications. Nevertheless, there are some differences. For example, the lateral structure of an LDMOS transistor means it has a very low feedback capacitance compared with a bipolar transistor. And as power gain is directly related to the feedback capacitance and source (or emitter) inductance, this means an LDMOS transistor has higher power gain. Furthermore, an LDMOS transistor has superior intermodulation distortion performance over a large dynamic range.

Table 1-2 LDMOS and bipolar devices compared

ADVANTAGES OF LDMOS	DISADVANTAGES OF LDMOS
Simpler biasing circuit. This is primarily due to a MOS transistor's high input impedance, and the low and negative temperature coefficient at high drain currents. **Higher power gain** than comparable bipolar types. This is due to the low source inductance and low feedback capacitance. **Simple control of the output power**. The output power can be controlled down to almost zero simply by reducing the DC gate-source voltage. **Superior thermal stability** owing to the negative temperature coefficient of the drain current at high levels. This is also why the current distribution over the whole active area of an LDMOS device is so good. **Superior load mismatch tolerance** - another benefit of the superior thermal stability of an LDMOSFET. **Lower high-order (7th and higher) intermodulation products** due to the 'smoother' characteristics of MOS devices.	**The gate is sensitive to electrostatic charges**, so ESD protection measures must be taken. **Higher output power 'slump'** (reduction of output power at high temperature). Note, this is primarily caused by decreasing transconductance.

1.2 Transistor equivalent circuit

At this point, it is useful to introduce a basic equivalent circuit of a bipolar RF transmitting transistor, and a few simple expressions that indicate the behaviour of power gain, input and load impedance under different conditions. This will assist the understanding of the following section on internal matching.

Figure 1-12 shows a simple equivalent circuit of an RF transistor with load circuit. Note, the emitter inductance, L_E, affects transistor performance significantly as we shall see presently.

1.2.1 Main elements

The collector-to-base feedback capacitance consists of two parts (see Fig.1-1, transistor cross-section):

- *An intrinsic part C_{BCi}:* the capacitance of the reverse biased collector-to-base junction in the regions below the emitter
- *An extrinsic part C_{BCe}:* the capacitance of the same junction beyond the emitter. C_{BCe} also includes parasitic capacitances introduced by the base metallization.

The sum of these capacitances, C_{BCt}, is published in data sheets as C_{re}:

$$C_{re} = C_{BCi} + C_{BCe}$$

R_B represents the series resistance of the base layer, and R_E is the emitter ballast resistance. C_{BE} represents the total forward biased base-emitter capacitance which is mainly determined by the diffusion capacitance, and which varies directly with the emitter current. This capacitance is normally shunted by a resistor, omitted here, since at high frequency operation, virtually all current flows into C_{BE}.

The collector is terminated by a load resistance R_L shunted by an inductance L_L which resonates with the total collector-to-base capacitance. Approximate expressions for these circuit elements are:

$$L_L = \frac{1}{\omega^2 C_{BC}} \text{ and } R_L = \frac{V_C^2}{2P_L}$$

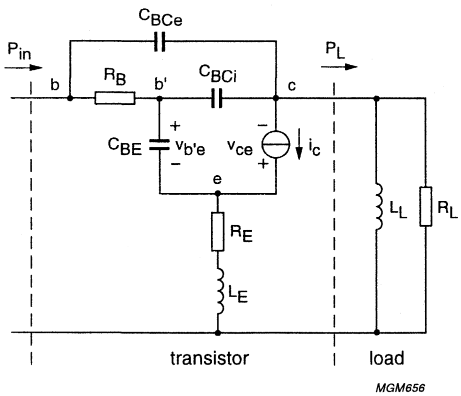
At high frequencies, the collector current, i_c, is proportional to the base-emitter current, i_{be}, and lags the latter by 90°:

$$i_c \approx i_{b'e}\left(\frac{\omega_T}{j\omega}\right)$$

Clearly, the high frequency common-emitter current gain, h_{fe}, is approximately ω_T/ω.

To simplify the following approximations, it has been assumed that:

- For maximum power, the collector circuit is in resonance, i.e. v_{ce} and i_c are in antiphase
- The base potential is very small compared to the collector voltage
- All collector parasitics are part of the load circuit.



b: Base.
c: Collector.
e: Emitter.

Fig.1-12 Simple equivalent circuit of a bipolar RF transmitting transistor.

1.2.2 *Input impedance*

With these assumptions, the input impedance, Z_{in}, can be approximated by:

$$Z_{in} = \left[\frac{1}{1+\omega_T C_{BCt} R_L}\right] \times$$

$$\left[(1+\omega_T C_{BCi} R_L)\, R_B + \omega_T L_E + R_E + j\omega L_E + \frac{1}{j\omega}\left(\frac{1}{C_{BE}} + R_E\omega_T\right)\right]$$

Note that emitter inductance effectively increases the total input resistance by $\omega_T L_E$. The emitter ballast resistance R_E appears as a series capacitance $1/R_E\omega_T$, decreasing the total input capacitance. Based on this expression, the total input impedance can be represented by a series RLC equivalent circuit, see Section 1.3.1.

1.2.3 *Power gain*

The power gain, Gp, can be approximated by:

$$G_p = \frac{P_L}{P_{in}} = \left(\frac{\omega_T}{\omega}\right)^2\left(\frac{1}{1+\omega_T C_{BCt} R_L}\right) \times$$

$$\left(\frac{R_L}{(1+\omega_T C_{BCi} R_L)\, R_B + R_E + \omega_T L_E}\right)$$

Note that emitter inductance L_E reduces power gain and is a key performance-determining factor in high-frequency transistors. It depends on bonding wire and package inductances. Other important parameters affecting power gain are R_E and these are determined by the active parts of the die design.

1.2.4 *Large-signal expressions*

The expressions given for Z_{in} and G_p relate to class-A amplifiers operating in the linear (i.e. small-signal) region. For large-signal operation, several elements become non-linear. The expressions can however still be used for a first-order approximation by substituting *average* values for the voltage and current dependent elements. In addition for class-B and class-C operation, the conduction angle, which affects the average value of ω_T, should be taken into account.

1.3 Internal matching

Impedance matching is required to optimize the performance of a transmitting transistor in the application for which it was designed. Internal matching raises impedances and improves wideband capability. To assist designers, many of Philips' transmitting transistors already incorporate internal matching circuitry, simplifying or reducing the external matching required.

1.3.1 Input matching

Figure 1-13 shows the equivalent circuit of the input impedance of a bipolar transmitting transistor without matching circuitry.

At high frequencies, the capacitor has very low reactance and can be neglected in most cases. In a high-power transistor, the resistor becomes very small, typically <1 Ω, as such a device can be considered as many small 'transistors' in parallel The inductor, which is normally 1 to 2 nH, has a rather high reactance in the UHF region, so the input Q becomes high, making wideband matching difficult if not impossible, while circuit losses increase significantly. To compensate for these effects, an additional capacitor is often fabricated 'inside' the transistor such that the transistor equivalent circuit is as shown in Fig.1-14.

This capacitor, together with the base and emitter inductances, forms a first matching section that raises the input impedance to a more acceptable level. The resonant frequency of the section is set to be somewhat above the maximum operating frequency for which the transistor is intended.

An additional advantage of this configuration is that it increases the power gain slightly at the high end of the frequency band, not only because of reduced circuit losses, but mainly because the capacitor is, in effect, connected to a tap on the emitter lead inductance, overcoming a major cause of reduced power gain at high frequencies (emitter lead inductance).

A MOS capacitor is used, and it can only be used in transistor packages with two emitter 'bridges': one, the normal elevated bridge; the other, an integrated bridge on the beryllia disc to which the capacitor is soldered. The maximum performance improvement is obtained with packages having *four* emitter connections (see Fig.1-15). Better still of course are packages with internal emitter grounding.

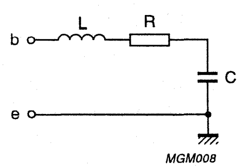


Fig.1-13 Equivalent circuit of the input impedance of a bipolar transmitting transistor. For high-frequency high-power operation, matching circuitry is required. b: base; e: emitter.

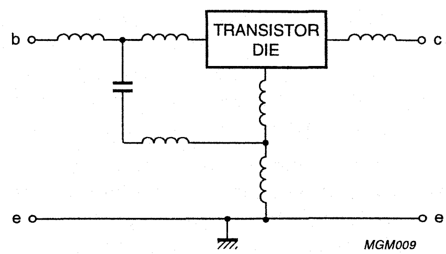


Fig.1-14 Equivalent circuit of a bipolar transmitting transistor with internal input matching. Adding an internal capacitor improves wideband matching.

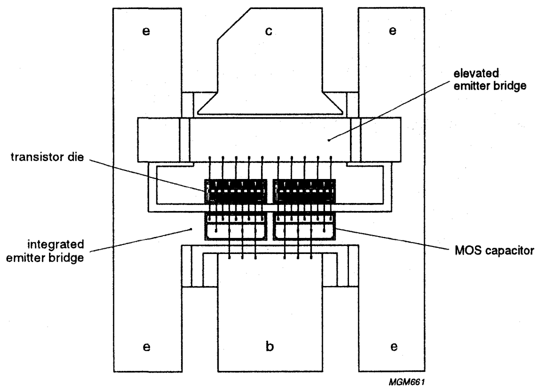


Fig.1-15 Position of the MOS input matching capacitor in a package with two emitter bridges, and four emitter connections.

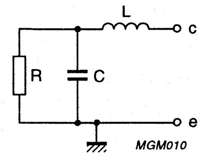


Fig.1-16 Large-signal equivalent circuit of the output of an RF power transistor.
L: collector and emitter lead inductance;
C: effective output capacitance;
R: optimum load resistance. Note, R is the load resistance that produces maximum output. It is not a physical resistor in a transistor and its value varies according to the application.

1.3.2 Output matching

At the output of a transistor, the situation is somewhat different, see Fig.1-16.

In wideband matching circuits, it is desirable to tune out (with inductive shunt) the capacitor C somewhere in the frequency band for which the transistor is intended. In practice, the best results are obtained when the resonant frequency is in the lower part of the band.

If an *external* shunt inductor were used for this purpose, the result would be a very low inductive tap, making further matching extremely difficult, especially at high powers and frequencies. A better solution would be to tune out the collector capacitance *inside the transistor package*. This is done in practice in balanced (push-pull) transistors by adding a metallized strip onto the beryllia or aluminium nitride disc. In single-ended devices, it is done by connecting one side (the other is grounded) of a MOS capacitor that provides isolation to the collector via bonding wires that form the required shunt inductance, see Fig.1-17.

A disadvantage of this approach in both cases is that such a transistor is unsuitable for use in frequency bands lower than the one for which it is intended. This limitation is outweighed however by the higher load impedance and lower Q-factor, resulting in lower losses in the matching circuit and improved wideband performance.

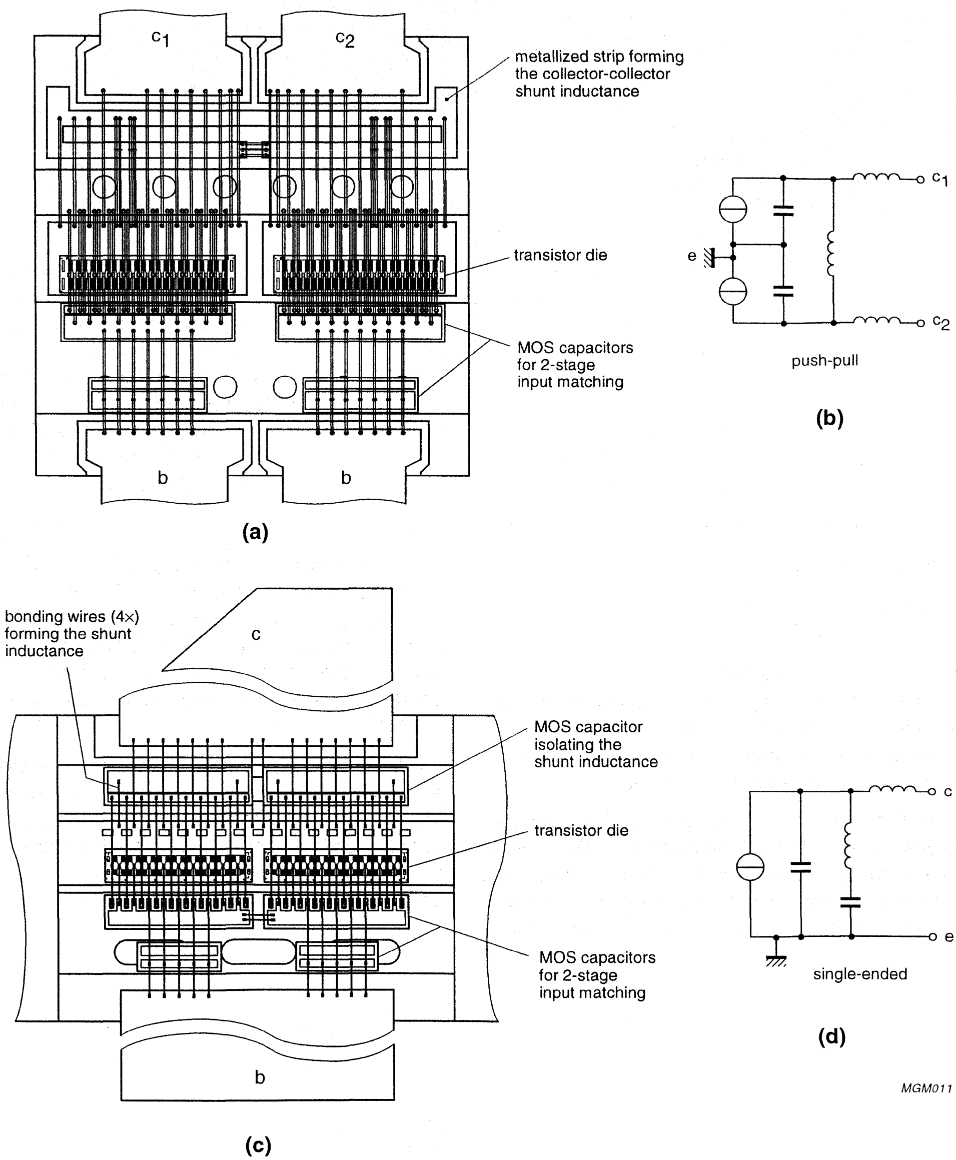


Fig.1-17 Bonding arrangement of (a) a BLV861 intended for use in push-pull configuration (b), and (c) bonding arrangement of a BLV2045 intended for single-ended configuration (d).

2 RF POWER TRANSISTOR CHARACTERISTICS

This section describes how to interpret and use the data published by Philips Semiconductors on its transmitting transistors.

2.1 Bipolar devices

2.1.1 Limiting values (Ratings)

As an example, consider the published data (Fig. 2-1) for the BLV59, a 30 W transistor intended for operation at up to 860 MHz from a supply voltage of 25 V, and used mainly in class-AB linear operation in TV transmitters.

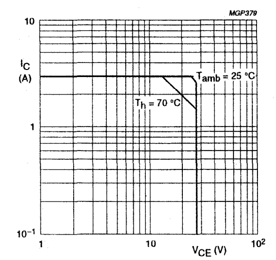
Philips Semiconductors — Product specification

UHF linear power transistor — BLV59

LIMITING VALUES

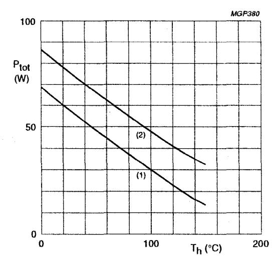
In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	50	V
V_{CEO}	collector-emitter voltage	open base	–	27	V
V_{EBO}	emitter-base voltage	open collector	–	3.5	V
I_C	collector current (DC)		–	3	A
$I_{C(AV)}$	average collector current		–	3	A
I_{CM}	peak collector current	f > 1 MHz	–	9	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; f > 1 MHz	–	70	W
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		–	200	°C



$R_{th\ mb\text{-}h}$ = 0.4 K/W.

Fig.2 DC SOAR.



(1) Continuous operation (f > 1 MHz).
(2) Short-time operation during mismatch (f > 1 MHz).

Fig.3 Power/temperature derating curves.

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Fig.2-1 Part of the BLV59 data sheet showing how device *ratings* are specified.

2.1.1.1 *DEFINITIONS*

V_{CBO} *The maximum collector-base voltage with open emitter,* which must never be exceeded in normal operation. If this voltage is exceeded slightly, the transistor will probably not be damaged immediately. However, it will certainly produce a lot of wideband noise if the peaks of the RF voltage reach the avalanche breakdown voltage.

For some transistors, V_{CES}, the maximum collector-emitter voltage with a short circuit between base and emitter is specified. V_{CES} is almost equal to V_{CBO}.

V_{CEO} *The maximum collector-emitter voltage with open base.* The supply voltage must always be lower than this voltage otherwise the base current becomes negative. And, as there is always some DC resistance between base and emitter, this can lead to reverse second breakdown.

For some transistors, V_{CER}, the maximum collector-emitter voltage with a small resistor e.g. 10 Ω, between base and emitter is specified. V_{CER} is slightly lower than V_{CBO} and V_{CES}. With higher resistances, this voltage can approach V_{CEO}.

The relation between the different collector breakdown voltages is illustrated in Fig.2-2.

V_{EBO} *The maximum emitter-base voltage with open collector.* When the transistor is used in class-C, the average base-emitter voltage is negative, and V_{EBO} can easily be exceeded. Life tests performed under such conditions have shown that parameters such as h_{FE} and leakage currents can deteriorate. Philips Semiconductors therefore does not advise class-C operation of bipolar transistors except when the negative base-emitter bias voltage is a few tenths of a volt.

I_C *The maximum collector DC current.* This is specified to protect the emitter bonding wires and the die metallization.

I_{CM} *The maximum instantaneous value of the collector current.* Characteristics such as h_{FE} and f_T deteriorate rapidly above this value, making operation at higher levels impractical.

P_{tot} *The maximum RF dissipation at a mounting base temperature of 25 °C.* This is given only to enable different devices to be compared. In practice, the mounting base temperature will always be higher than 25 °C.

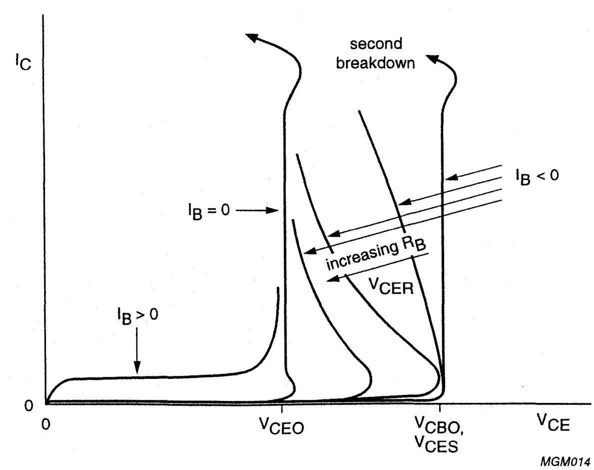


Fig.2-2 Definition of breakdown voltages.

T_{stg} *The maximum ($T_{stg\ max}$) and minimum ($T_{stg\ min}$) temperatures at which a device may be stored when not in operation.* These limits maximize storage life.

T_j *The maximum junction temperature in operation.* This is 200 °C for most silicon devices. Exceeding this value for long periods will shorten transistor life.

DC SOAR

The DC Safe Operating ARea.
This is a graph showing the maximum allowable DC collector current versus the collector-emitter DC voltage at a specified mounting base (and/or heatsink) temperature. This information is essential if a device is used in class-A. Note that the thermal resistance in DC operation is often higher (i.e. worse) than the resistance in RF operation. However, for a well-designed device, i.e. one with a built-in emitter resistance of sufficiently high value, the differences between the DC and RF SOAR are small.

Some transistors designed specifically for class-B operation have smaller built-in emitter resistances, so the allowable DC dissipation at high collector voltages is reduced to prevent forward second breakdown at these voltages. Figure 2-3 gives an example of such a DC SOAR.

Power/temperature derating curves versus heatsink temperature.
These curves give the maximum allowable RF dissipation under different conditions. A transistor's thermal resistance is not constant because the thermal resistivities of silicon, beryllia and aluminium nitride are temperature dependent, all increasing with temperature. Therefore, the thermal resistance of the transistor depends on the heatsink or mounting-base temperature and on the power dissipation.

The curve given for continuous operation (Curve I) is based on a junction temperature of 200 °C. The other curve (Curve II) is for short-term operation under mismatch conditions and is based on a maximum junction temperature of 270 to 280 °C. Clearly, the latter sort of operation reduces transistor life and should be restricted as much as possible.

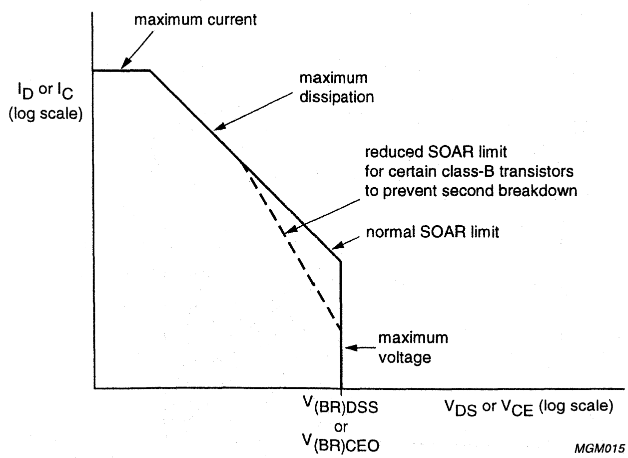


Fig.2-3 Example of a DC SOAR graph for a transistor designed specifically for class-B operation.

2.1.2 *Characteristics*

The BLV59 data sheet will again be used to illustrate how the main characteristics are presented in (see Fig.2-4)

2.1.2.1 *THERMAL CHARACTERISTICS*

Two thermal resistance values are given: from junction to mounting base, and from mounting base to heatsink. The former value is obtained from a well-defined, reproducible measurement taken under specified conditions and is guaranteed.

Philips Semiconductors — Product specification

UHF linear power transistor — BLV59

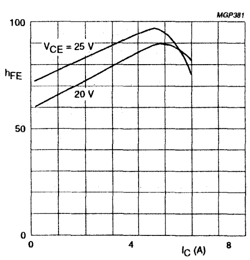
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C, P_{tot} = 50 W	2.3	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.4	K/W

CHARACTERISTICS

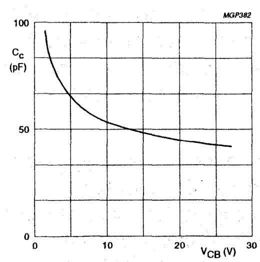
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 50 mA	50	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 100 mA	27	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 10 mA	3.5	–	–	V
I_{CES}	collector leakage current	V_{CE} = 27 V; V_{BE} = 0	–	–	10	mA
$E_{(SBR)}$	second breakdown energy	L = 25 mH; f = 50 Hz; R_{BE} = 10 Ω	4	–	–	mJ
h_{FE}	DC current gain	V_{CE} = 24 V; I_C = 2 A	15	–	–	
C_c	collector capacitance	V_{CB} = 25 V; I_E = i_e = 0; f = 1 MHz	–	44	–	pF
C_{re}	feedback capacitance	V_{CE} = 25 V; I_C = 0; f = 1 MHz	–	30	–	pF
C_{cf}	collector-flange capacitance		–	2	–	pF



T_j = 25 °C.

Fig.4 DC current gain as a function of collector current; typical values.



I_E = i_e = 0; f = 1 MHz.

Fig.5 Collector capacitance as a function of collector-base voltage; typical values

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Fig.2-4 Part of the BLV59 data sheet showing how device *characteristics* are specified.

2.1.2.2 *OTHER CHARACTERISTICS*

Every transistor is subjected to a series of DC measurements to guarantee performance to specification. These measurements include the breakdown voltages mentioned earlier which are tested at specified currents, and the collector leakage current, in this example, I_{CES}, specified at a collector voltage of about half the breakdown voltage. Sometimes, other leakage currents such as I_{CEO} and I_{EBO} are specified.

h_{FE} *The DC current gain*
This is the ratio of collector and base current at specified V_{CE} and I_C. A minimum value is always given; a maximum sometimes. Matched pairs of some transistor types are available for push-pull operation.

$E_{(SBR)}$ *The (reverse) second breakdown energy*
This is measured with a coil of 25 mH in the collector lead of the transistor. First, the collector current is adjusted such that:

$$I_C = \sqrt{\frac{2E_{(SBR)}}{L}}$$

where $E_{(SBR)}$ is the specified second breakdown energy.

The current is then suddenly interrupted, causing the collector voltage to rise to the avalanche voltage and to stay there until all the energy of the coil ($LI_C^2/2$) is dissipated by the transistor. If the collector voltage falls before a pre-set time that represents ideal transistor behaviour, the device is deemed unable to withstand the specified energy and fails the test.

A transistor's performance in the $E_{(SBR)}$ test gives a good indication of its RF mismatch performance. Moreover, since this test can be performed much quicker than a mismatch test and has no effect on transistor life, 100% testing of $E_{(SBR)}$ is used in production instead of mismatch-testing. Samples from production are of course subjected to real mismatch testing (see Section 2.1.3.3, Ruggedness) to establish quality levels.

Several other characteristics (typical values) such as capacitances and sometimes f_T and $V_{CE\,sat}$ are given:

C_c *The total collector or output capacitance.* This is the sum of C_{cb} and C_{ce} measured at 1 MHz.

C_{re} *The feedback capacitance, i.e. C_{cb}, also measured at 1 MHz.* Both capacitances are measured at the standard supply voltage for each transistor type.

f_T *The transition frequency.* This is the frequency at which the RF value of the common-emitter current gain, h_{fe}, has fallen to one, see Fig.2-5, and is a useful performance indicator when comparing transistors. It is obtained in one measurement taken with the transistor output short-circuited. Above a certain frequency, the RF current gain, h_{fe} begins to fall off at 6 dB/octave. The measuring frequency, f_m, is chosen well above this frequency and then:
$f_T = h_{fe}f_m$.

Note: no f_T information is published for the BLV59, because this transistor has a built-in matching capacitor at its input which would make the measurement meaningless.

$V_{CE\,sat}$ *The collector-emitter saturation voltage* gives an impression of the total resistance in the collector-emitter circuit. It is measured at an I_C/I_B ratio less than the specified minimum h_{FE} to ensure the transistor is saturated.

Finally, some graphs such as h_{FE} versus I_C, C_c versus V_{CB}, and in some cases f_T versus I_C are given.

All characteristics are published at T_j = 25 °C and (with the exception of the capacitances) are obtained from pulsed measurements using pulses of short duration compared to the thermal time constant of the die.

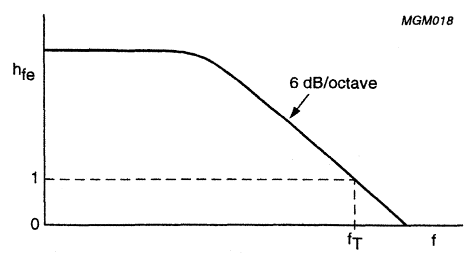


Fig.2-5 RF current gain, h_{fe} as a function of frequency. f_T is the transition frequency.

2.1.3 *Application information*

For each transistor type, a narrow-band test circuit is designed for the highest frequency of operation. The circuit is aligned for maximum power transfer and minimum input reflection. Important parameters such as power gain and collector efficiency (see Sections 2.1.3.1 and 2.1.3.2) are measured for each transistor from production.

To assist circuit designers, Philips Semiconductors publishes the circuit diagram and board lay-out of these test circuits (and the measured performance) in its data sheets, see Figs 2-6 and 2-7.

Philips Semiconductors — Product specification

UHF linear power transistor — BLV59

APPLICATION INFORMATION

RF performance up to T_h = 25 °C in a common emitter class-AB circuit; $R_{th\ mb\text{-}h}$ = 0.4 K/W.

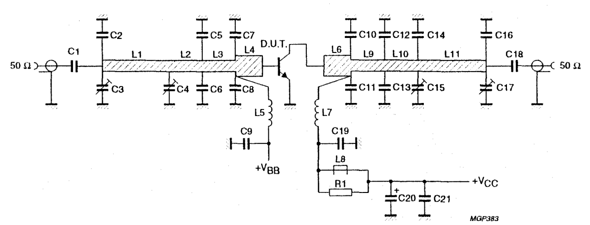
MODE OF OPERATION	f (MHz)	V_{CE} (V)	$I_{C(ZS)}$ (mA)	G_p (dB)	P_L (W)	η_C (%)	ΔG_p (dB)(1)
CW, class-AB	860	25	60	>7 typ. 8.5	30	>50 typ. 55	<1 typ. 0.2

Note

1. Assuming a 3rd order amplitude transfer characteristic, 1 dB gain compression corresponds with 30% sync input/25% sync output compression in television service (negative modulation, C.C.I.R. system).

Ruggedness in class-AB operation

The BLV59 is capable of withstanding a load mismatch corresponding to VSWR = 10 through all phases at rated load power under the following conditions: V_{CE} = 25 V; f = 860 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W; $I_{C(ZS)}$ = 60 mA.



Temperature compensated bias (R_i < 0.1 Ω).

Fig.6 Class-AB test circuit at 860 MHz.

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Fig.2-6 Part of the BLV59 data sheet showing the Class-AB test circuit for the BLV59 at f = 860 MHz. Fig.2-7 shows the board and component layout. Though omitted here, component values, descriptions and manufacturers as well as board specifications and assembly instructions are given in the data sheets for each test circuit.

2.1.3.1 POWER GAIN

The power gain is defined as:

$$G_P = 10 \log\left(\frac{P_L}{P_S}\right) \text{ dB}$$

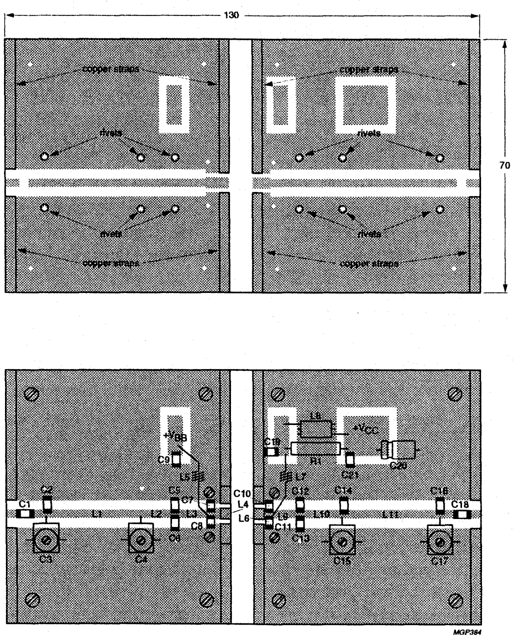
where:

P_L is the output power in the 50 Ω load

P_S is the forward power delivered by the 50 Ω source.

Philips Semiconductors | Product specification

UHF linear power transistor | BLV59



Dimensions in mm.

The components are situated on one side of the copper-clad PTFE-glass board, the other side is unetched and serves as a ground plane. Earth connections are made by fixing screws, hollow rivets and copper straps around the board and under the bases to provide a direct contact between the copper on the component side and the ground plane.

Fig.7 Printed-circuit board and component layout for 860 MHz class-AB test circuit.

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Fig.2-7 Board and component layout of the circuit shown in Fig.2-6.

2.1.3.2 *COLLECTOR EFFICIENCY*

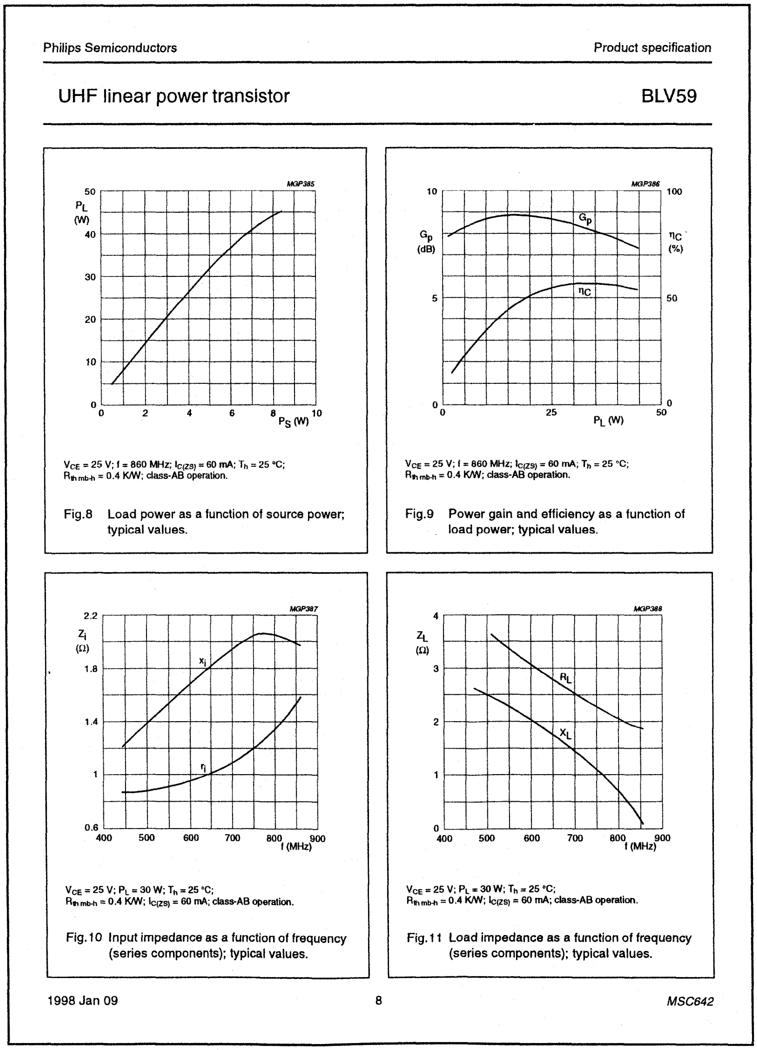
The collector efficiency is defined as:

$$\eta_c = \frac{P_L}{V_{CE} I_C} \times 100\%$$

where V_{CE} and I_C are the collector-emitter DC voltage and collector DC current respectively.

For the BLV59, the gain compression at maximum power (30 W) is also measured. The published values (all types) are all guaranteed.

Graphs are always given of load power versus source power and of power gain and efficiency versus load power (all typical values), see Fig.2-8.



Philips Semiconductors — Product specification

UHF linear power transistor — BLV59

V_{CE} = 25 V; f = 860 MHz; $I_{C(ZS)}$ = 60 mA; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W; class-AB operation.

Fig.8 Load power as a function of source power; typical values.

V_{CE} = 25 V; f = 860 MHz; $I_{C(ZS)}$ = 60 mA; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W; class-AB operation.

Fig.9 Power gain and efficiency as a function of load power; typical values.

V_{CE} = 25 V; P_L = 30 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W; $I_{C(ZS)}$ = 60 mA; class-AB operation.

Fig.10 Input impedance as a function of frequency (series components); typical values.

V_{CE} = 25 V; P_L = 30 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W; $I_{C(ZS)}$ = 60 mA; class-AB operation.

Fig.11 Load impedance as a function of frequency (series components); typical values.

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Fig.2-8 Part of the BLV59 data sheet showing the performance (Figs.8 and 9) measured in the test circuit at a specified frequency (here 860 MHz).

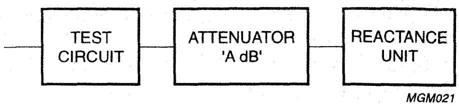


Fig.2-9 Circuit for measuring load mismatch tolerance.

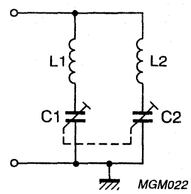


Fig.2-10 LC reactance circuit for mismatch measurements at low frequencies.

2.1.3.3 RUGGEDNESS

Transistors are also tested for their ability to withstand output mismatching without any measurable degradation of performance (ruggedness). This is done by replacing the 50 Ω load impedance of the test circuit by an attenuator and reactance unit as shown in Fig.2-9.

The attenuator is dimensioned such that the VSWR required by the test is obtained according to:

$$A = 10\log\left(\frac{s+1}{s-1}\right)\ \text{dB}$$

where A is the attenuation and s is the VSWR.

The reactance unit is required to vary the phase of the reflection coefficient and has to be able to provide reactances from $-\infty$ to $+\infty$, including zero at the test frequency (usually the transistors maximum intended operating frequency). At very high frequencies, this can be done by means of a variable-length coaxial stub, variable over at least half a wavelength. At low frequencies, an LC circuit as shown in Fig.2-10 is used.

In this circuit, inductors L_1 and L_2 must be screened from each other. C_1 and C_2 is a ganged capacitor, and $C_1 = C_2$. Suitable component values are:

$X_{L1} = +j50\ \Omega$; $X_{L2} = +j200\ \Omega$

$X_{C1} = X_{C2} = -j200\ \Omega$ to $-j50\ \Omega$.

If C_1 and C_2 are set to their minimum value, the first series resonance (of L_2 and C_2) occurs, see Fig.2-11.

By increasing the capacitance of C_1 and C_2, the reactance can be varied from zero to $+\infty$ at which a parallel resonance occurs. Increasing the capacitances further changes the reactance from $-\infty$ to zero at which the second series resonance (of L_1 and C_1) occurs.

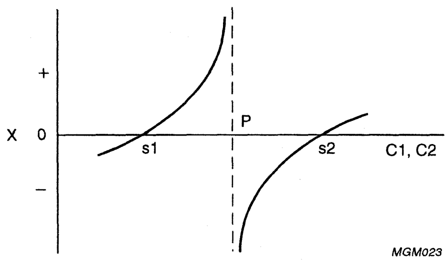


Fig.2-11 Reactance of the reactance unit as a function of C_1 and C_2 ($C_1 = C_2$). s1, s2: first and second series resonances.

2.1.3.4 GAIN AND IMPEDANCE INFORMATION

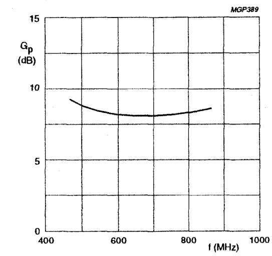
To facilitate the design of both narrowband and wideband amplifiers, graphs of input impedance, optimum load impedance and power gain over a wide range of frequencies are published in Philips' data sheets, see Fig.2-8 (Figs 10 and 11) and Fig.2-12. The published data are valid for the specified supply voltage and output power; when the conditions in your application are different, please contact Philips Semiconductors for additional information.

Philips Semiconductors

Product specification

UHF linear power transistor

BLV59



V_{CE} = 25 V; P_L = 30 W; T_h = 25 °C;
$R_{th\,mb\text{-}h}$ = 0.4 K/W; $I_{C(ZS)}$ = 60 mA; class-AB operation.

Fig.12 Power gain as a function of load power; typical values.

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Fig.2-12 Part of the BLV59 data sheet showing additional information to assist in the design of narrow and wideband amplifiers. See also Fig.2-8.

2.2 MOS devices

2.2.1 Limiting values (Ratings)

As an example, consider the published data (Fig.2-13) for the BLF544, a silicon n-channel enhancement mode vertical DMOS transistor intended for wideband operation in the VHF/UHF range. At 500 MHz and a supply voltage of 28 V, the BLF544 has a specified output power of 20 W.

Philips Semiconductors — Product specification

UHF power MOS transistor — BLF544

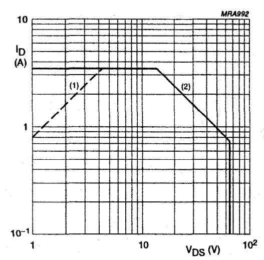
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	3.5	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C	–	48	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

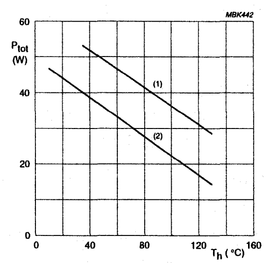
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	3.7	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	0.4	K/W



(1) Current is this area may be limited by R_{DSon}.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.3 Power/temperature derating curves.

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Fig.2-13 Part of the BLF544 data sheet showing how the device *ratings* of a MOS transistor are specified.

2.2.1.1 DEFINITIONS

Since many of the ratings of a MOS transmitting transistor are the same or very similar to those of a bipolar device, we shall discuss only the main differences, namely:

V_{DS} *Drain-source voltage*
This is equivalent to V_{CBO} for a bipolar transistor. A quantity like V_{CEO} does not exist for MOS devices.

V_{GS} *Gate-source voltage.*
This rating must be carefully adhered to. Even very small amounts of energy are able to destroy a MOS device. Static charges in particular are dangerous in this respect; ESD protection measures are essential when handling MOS transistors.

I_D *Drain current.*
This is equivalent to I_C for a bipolar transistor.

All other ratings in Fig.2-13 have the same meaning as those for bipolar transistors. Unlike bipolars however, there is no difference between the power dissipation for DC and RF operation. In the DC SOAR, there is an extra drain current limitation at low drain voltages due to $R_{DS\,(on)}$.

2.2.2 Characteristics

As the example of Fig.2-14 shows, the published data contains some well-known parameters such as breakdown voltage and leakage currents and, in addition:

$V_{GS(th)}$ *The gate voltage at which drain current starts to flow.*
As there is quite a large spread on this parameter, matched pairs of some transistor types are available for push-pull operation ($V_{GS(th)}$ matched to within <100 mV).

g_{fs} *The forward transconductance.*
This is the slope of the I_D versus V_{GS} characteristic at a specified I_D. This parameter is important for the power gain of a transistor.

$R_{DS\,(on)}$ *The total resistance in the drain-source circuit at a high, positive V_{GS}.*
$R_{DS\,(on)}$ is the main parameter that determines the drain efficiency.

C_{is} *The input capacitance when the output is short-circuited.*
This means that $C_{is} = C_{gs} + C_{gd}$ where C_{gs} and C_{gd} are the gate-source and gate-drain capacitances respectively.

C_{os} *The output capacitance when the input is short-circuited.*
This means that $C_{os} = C_{ds} + C_{gd}$ where C_{ds} and C_{gd} are the drain-source and gate-drain capacitances respectively.

C_{rs} *The feedback capacitance.*
This is the same as C_{gd}.

I_{DSX} *The maximum drain current that the device can deliver.*
Above I_{DSX}, the transconductance is too low for practical use.

Besides the above, some graphs are given such as I_D versus V_{GS}. As this characteristic is temperature dependent, its temperature coefficient (useful when designing bias units) is given in a separate graph (see Fig.2-14).

$R_{DS(on)}$ is also dependent on junction temperature and this is shown in a graph (see Fig.2-15) Finally, the capacitances are given as functions of the drain voltage (also shown in Fig.2-15). Note, C_{is} is the sum of the gate-source capacitance and the gate-drain capacitance (equal to C_{rs}), and subtracting the latter from C_{is} shows that the gate-source capacitance is almost constant.

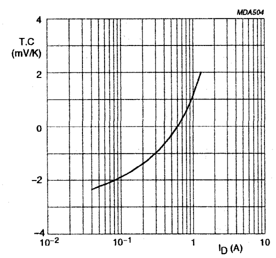
Philips Semiconductors — Product specification

UHF power MOS transistor — BLF544

CHARACTERISTICS

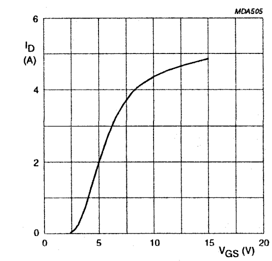
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	1	mA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	μA
V_{GSth}	gate-source threshold voltage	I_D = 40 mA; V_{DS} = 10 V	1	–	4	V
ΔV_{GSth}	gate-source voltage difference of matched pairs	I_D = 40 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 1.2 A; V_{DS} = 10 V	600	900	–	mS
R_{DSon}	drain-source on-state resistance	I_D = 1.2 A; V_{GS} = 10 V	–	0.85	1.25	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	4.8	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	32	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	24	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	6.4	–	pF



V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values.



V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage; typical values.

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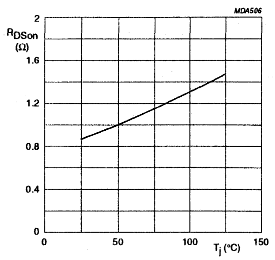
Fig.2-14 Part of the BLF544 data sheet showing how the device *characteristics* of a MOS transistor are specified.

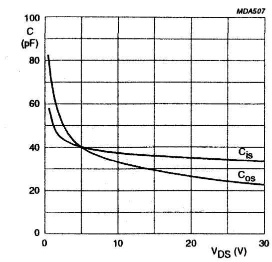
Philips Semiconductors | Product specification

UHF power MOS transistor | BLF544



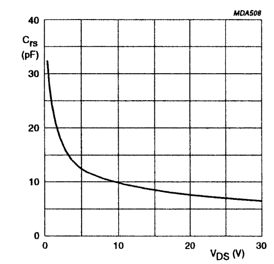
I_D = 1.2 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage; typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage; typical values.

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Fig.2-15 Part of the BLF544 data sheet showing the $R_{DS(on)}$ and capacitance graphs.

2.2.3 *Application information*

The published application information for MOS transistors is so similar to that for bipolar devices (see Section 2.1.3), that no further comment is needed here.

2.3 Reliability

Reliability is a measure of the ability of a device to perform its intended function over its useful lifetime under stated conditions. It is thus a measure of the quality remaining after some time and after exposure to certain operating stresses. Like other measures of quality, reliability is a probability. The failure rates of many semiconductors follow the well-known bath-tub curve, (see Fig.2-16).

2.3.1 *Failure rate*

The instantaneous failure rate is the sum of three components:

Early failures (infant mortalities)
These are failures of devices that initially meet the specification, but which fail due to minor latent defects exposed during the first hours of operation. Such failures are common to the fabrication processes of all semiconductor manufacturers. They can be isolated by subjecting all devices to a burn-in period.

Random failures
This is the dominant failure mode during the main period of life. Failures may occur randomly for no apparent reason. The failure rate is virtually constant during this period, the only one therefore where it is useful to specify a failure rate.

Wear-out failures
These are the increasing number of failures that occur as physical and chemical degradation processes accelerate until no working components remain.

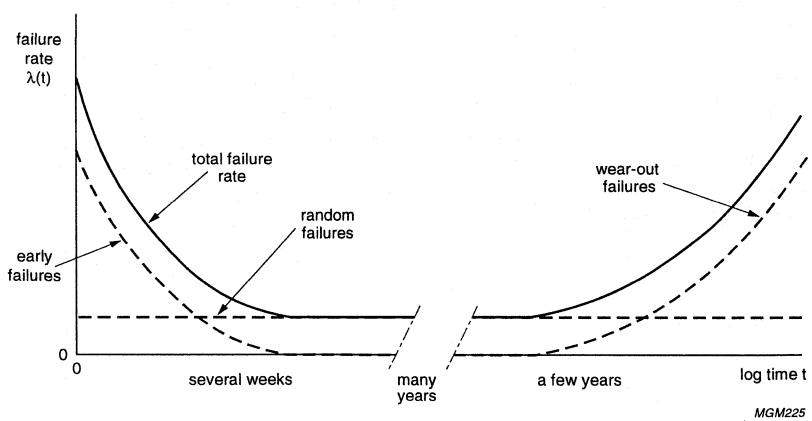

Fig.2-16 The familiar bath-tub curve of failure rate as a function of time. Note, time is given on a log scale - the period of constant failure rate is soon reached.

2.3.2 *Mean-Time-To-Failure (MTTF)*

During the constant failure rate period, the reliability is:
$R(t) = e^{-\lambda t}$
where:
R(t) is the probability of no failures up to time t, and
λ is the failure rate.

The MTTF is the time after which R(t) has fallen to 37% (1/e), that is, MTTF = $1/\lambda$. A device that has operated up to the MTTF therefore has a probability of survival of 0.37.

2.3.3 *Median-Time-To-Failure (MTF or $t_{50\%}$)*

In many instances, the cumulative failures of semiconductor devices follow a lognormal distribution. The time at which 50% of the components have failed due to wearout is called the median-time-to-failure. Note that knowledge of MTF is of little value to equipment designers; much more important, and useful, is the likely time to failure of, for example, the first 0.1% ($t_{0.1\%}$).

2.3.4 *Bonding wires, metallization and barrier layers*

Philips' modern range of RF transmitting transistors with gold bonding wires, gold metallization and a TiPt barrier layer (to prevent gold-silicon alloy formation) are extremely reliable especially at high junction temperatures. The use of barrier layers has enabled the potential reliability of all-gold designs to be fully exploited, and has overcome the shortcomings of all-aluminium designs such as electromigration, aluminium diffusion and thermal fatigue, and the 'purple plague' of the now-obsolete gold-aluminium hybrids.

A two-layer structure formed by depositing a platinum barrier layer on top of a titanium adhesive layer (the latter deposited on the silicon die) has proved to be highly effective at preventing alloy formation. Moreover, as the electromigration of gold is about one tenth that of aluminium, the current density in the metallization is no longer the limiting factor. And, the MTF of 'gold' transistors with barrier layers is theoretically 10^6 to 10^7 hours at a junction temperature of 200 °C. Accelerated life tests have shown that the lifetime mentioned can indeed be reached.

Published MTFs
Note, when comparing the published MTFs of different manufacturers, remember that different manufacturers base their MTFs on different failure mechanisms. Philips, for instance, includes the diffusion of gold into the die silicon, which indicates the quality of the platinum barrier layer, as a failure mechanism. Some manufacturers use electromigration measurements which can *suggest* reliability superior to that obtained using the former, more exacting, criterion.

2.3.5 *Power temperature-derating*

Finally, it is important to bear in mind the effect of derating. Suppose that an RF amplifier circuit has been designed such that the maximum junction temperature of the output transistor is 200 °C at maximum supply voltage and ambient temperature. This means that for most of the time, under normal operating conditions, the junction temperature will be lower, and the life of the transistor will be longer - more than double (2.4×) per 10 °C reduction in junction temperature.

3 POWER AMPLIFIER DESIGN

3.1 Classes of operation and biasing

3.1.1 Class-A

Class-A operation is characterized by a constant DC collector (or drain) voltage and current. This class of operation is required for linear amplifiers with severe linearity requirements including:

- Drivers in SSB transmitters where a 2-tone 3rd-order intermodulation of at least –40 dB is required
- Drivers in TV transmitters where the contribution to the gain compression must be very low, i.e. not more than a few tenths of a dB
- All stages of TV transposers. These are tested with a 3-tone signal and the 3rd-order intermodulation products must be below –55 to –60 dB. The driver stages should only deliver a small contribution to the overall intermodulation, so they have to operate at even lower efficiency than the final stage (as this is the only way to reduce distortion in class-A).

Though the theoretical maximum efficiency of a class-A amplifier is 50%, because of linearity requirements, the efficiency in the first two applications listed above will be no more than about 25%. And in TV transposers, the efficiency is only about 15% for the final stage and even less for the driver stages.

The transistor power gain in a class-A amplifier is about 3 to 4 dB higher than that of the same transistor operating in class-B. This is because the conduction period of the drain current in class-A is 360° and in class-B only 180° (electrical degrees). Therefore, the effective trans-conductance in class-B is only half that in class-A.

3.1.1.1 DISTORTION

SSB modulation is mainly used in the HF range: 1.5 to 30 MHz. When testing transistors for this application, Philips uses a standard test frequency of 28 MHz. Owing to its variable amplitude, an SSB signal is sensitive to distortion.

3.1.1.1.1 2-TONE INTERMODULATION DISTORTION TEST

3rd and 5th-order products

This is the most common distortion test. In this test, two equal-amplitude tones 1 kHz apart are applied to the input of the amplifier under test. Practical amplifiers will never be completely linear, and the most important distortion products they produce are the 3rd and 5th order ones, because these are in or very near to the pass-band.

NOTE TO SECTION 3

For clarity in equations, identifiers such as R1, +jB2, –jX3 in drawings are written as R_1, $+jB_2$, $-jX_3$ in the body text.

If the frequencies of the two input tones are denoted by p and q, the 3rd-order products are at frequencies of 2p–q and 2q–p, see Fig.3-1. The 5th-order products which usually have smaller amplitudes are at 3p–2q and 3q–2p. Note, the two intermodulation products of the same order don't necessarily have equal amplitudes. This can be due to non-ideal decoupling of the supply voltages, i.e. decoupling that is insufficiently effective at all the frequencies involved. Philips publishes the largest value in data sheets.

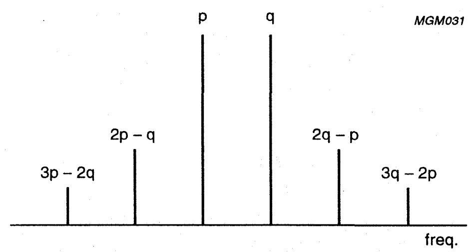

Fig.3-1 Position of the main intermodulation distortion products in the 2-tone test where p and q are the input tones.

Power relationships

If the tones at p and q are each of 10 W, then the combination has an *average (calorific)* power of 20 W. The two tones can however combine in phase or out of phase, producing an RF signal of variable amplitude. When the two tones are in phase, the voltage amplitude is twice that of one tone, so the power is four times that of one tone (in this example: 40 W). This maximum power is called the peak envelope power (PEP) and is commonly published in data sheets. When the two tones are in anti-phase, their combined amplitude is zero. In the ideal case, i.e. with no distortion, the envelope of the combined signal consists of half sine waves, see Fig.3-2.

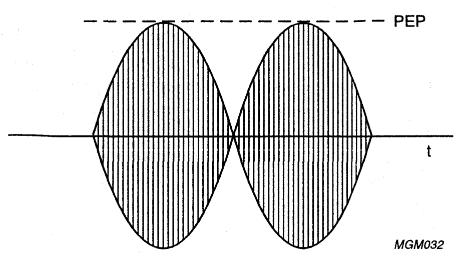

Fig.3-2 Two-tone signal showing the peak envelope power.

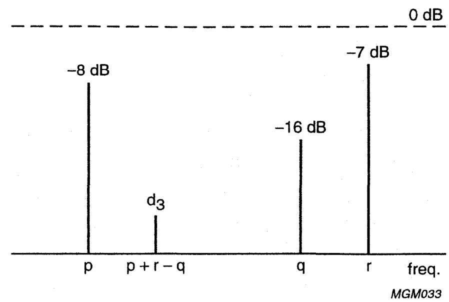

Fig.3-3 Three-tone test. The 3rd-order intermodulation product, d_3, is at p+r−q.

In class-A applications, distortion products are nearly always specified relative to the amplitude of one of the input test tones. As a general guideline, in the linear region of a class-A amplifier, every 1 dB reduction of output power reduces 3rd-order intermodulation distortion by 2 dB.

3.1.1.1.2 3-TONE TEST FOR TV TRANSPOSER APPLICATIONS

In a TV transposer, vision and sound are amplified together, so the distortion requirements are more severe, and it is usual to measure intermodulation using a 3-tone signal. The most popular test (DIN 45004B, para.6.3: 3-tone uses tones of −8 dB, −16 dB and −7 dB with respect to a 0 dB reference power level called the peak sync power. The first tone (−8 dB) represents the vision carrier, the second (−16 dB) a sideband, e.g. the colour carrier, and the third (−7 dB) the sound carrier. This combination of tones has a real peak power which is very close to the 0 dB level, namely: +0.02844 dB or +0.66%.

Another important relationship is the ratio of the average power to the 0 dB level. This ratio is 0.3831, so the 0 dB level is found by multiplying the calorific power by 2.61.

In the 3-tone test, the frequency of the −7 dB tone is 5.5 MHz higher than that of the −8 dB tone, while the frequency of the −16 dB tone is varied between the other two to produce the most intermodulation. If the frequencies of the tones are denoted by p, q and r respectively, we are primarily interested in the 3rd-order intermodulation product p+r−q which is inside the passband and which, in addition, usually has the largest amplitude, see Fig.3-3.

The test requirement for this product for a *complete* transposer is −51 dB with respect to the 0 dB reference level. This implies that the requirements for final stages are more severe (typically −55 dB) while those for driver stages more severe still (typically −60 dB).

In another 3-tone test method, the amplitude of the audio carrier is reduced from −7 dB to −10 dB. This has several effects:

- The actual peak power is only 76.2% of the 0 dB level
- The calorific power is 28.36% of the 0 dB level
- The intermodulation requirements are more severe. Because one of the tones is reduced by 3 dB, the intermodulation product at f_{p+r-q} is also reduced by 3 dB provided the amplifier is operating in the linear region.

3.1.1.1.3 RELATIONSHIP BETWEEN 2- AND 3-TONE TEST RESULTS

Theoretically, the first-mentioned 3-tone test and the 2-tone test measurement of SSB amplifiers are related. When (but only when) the PEP of the 2-tone test and the 0 dB level of the 3-tone test are equal, there is always a 13 dB difference in the intermodulation distortion. For example, if, an intermodulation of −40 dB is measured in the 2-tone test, −53 dB will be measured in the 3-tone test. Further, the 2-tone intermodulation should be measured relative to the two equal-amplitude tones and the 3-tone intermodulation relative to the 0 dB level.

Class-A amplifiers for TV transposers and transmitters behave in a similar way to those for SSB driver stages. So, reducing the output power by 1 dB reduces 3rd-order intermodulation by 2 dB.

3.1.1.2 BIASING

For MOS transistors, biasing is very simple. The temperature coefficient of the I_D versus V_{GS} curve is almost zero at the optimum operating point so an adjustable resistive divider is sufficient. For bipolar transistors, the situation is more complicated because of the temperature dependency of h_{FE} and V_{BE}.

In an audio amplifier, it is usual to stabilize the operating point by means of an emitter resistor and a base potentiometer. In an RF amplifier, however, it is preferable to ground the emitter to obtain maximum power gain as illustrated in Fig.3-4.

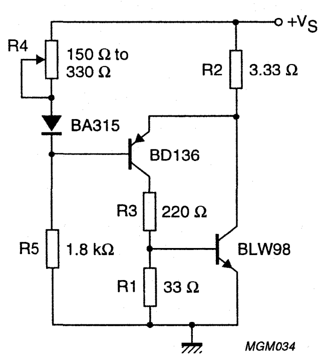

Fig.3-4 Class-A biasing circuit with grounded emitter for maximum power gain.

3.1.1.2.1 DESIGN EXAMPLE

In this example, a bias circuit must be designed such that the BLW98 RF transistor operates at V_{CE} = 25 V and I_C = 850 mA. The auxiliary transistor is a small PNP audio power transistor: BD136. Owing to the large negative feedback in the final circuit (Fig.3-4), the operating point of the BLW98 is extremely well stabilized for variations in ambient temperature and for the h_{FE} spread of the BLW98.

For instance, if h_{FE} rises due to an increase in ambient temperature, the collector voltage of the BLW98 will fall slightly, causing a decrease in the collector current of the BD136 and therefore in the base current of the BLW98.

The BA315 diode is used to compensate the temperature coefficient of the V_{BE} of the BD136. The variable resistor in series with this diode serves to adjust the I_C of the BLW98 accurately at the desired value.

3.1.1.2.2 CALCULATION OF COMPONENT VALUES

BD136 collector current

The supply voltage is chosen 2 to 3 V higher than the V_{CE} of the BLW98, e.g. 28 V (to provide sufficient negative feedback). The h_{FE} of the BLW98 can vary from 15 to about 100. To reduce the I_C variation of the BD136, the BLW98 is pre-loaded with a resistor between base and emitter (R_1 in Fig.3-4). The I_B of the BLW98 can vary from 8.5 to 57 mA while the required V_{BE} for an I_C of 850 mA is about 0.98 V. If 30 mA flows through R_1, the required resistance is: 0.98/0.03 ~ 33 Ω.

The I_C of the BD136 can now range from 38.5 to 87 mA with an average value of 51 mA. The BD136 has a typical h_{FE} of 100, so its I_B is approximately 0.5 mA and its average emitter current is 51.5 mA. The current through the collector resistor, R_2, of the BLW98 is then: 0.85 + 0.0515 = 0.9015 A. For a voltage drop of 3 V (28 – 25 V), a 3.33 Ω resistor (3/0.9015) rated at a rather high 2.7 W (3 × 0.9015) is required.

Protection resistor

To protect the BLW98 and to reduce the dissipation in the BD136, a resistor, R_3, is included between the collector of the BD136 and the base of the BLW98. The value of R_3 must be calculated on the basis of the minimum h_{FE} of the BLW98, and thus on the maximum I_C of the BD136 of 87 mA. As the V_{BE} of the BLW98 is about 1 V and the $V_{CE(sat)}$ of the BD136 is less than 1 V, the maximum voltage drop across R_3 must be less than 23 V. This means a maximum value of: 23/0.087 = 264 Ω, say 220 Ω, and the maximum dissipation in R_3 is $0.087^2 \times 220 = 1.67$ W.

Base potentiometer

Finally, the BD136 base potentiometer components (R_4, R_5 and the BA315) have to be determined. The potentiometer current must be high compared with the I_B of the BD136 (say 10 to 20 I_B); 13 mA is suitable and corresponds with the test circuit in the data sheet. As the V_{BE} of the BD136 is about 0.7 V and the voltage drop across the BA315 diode is 0.8 V, there is a drop of 2.9 V across the variable resistor, so a nominal resistance of 2.9/0.013 = 223 Ω is required. A range of 150 to 330 Ω provides sufficient adjustment for practical use. Across resistor R_5, there is a voltage drop of 24.3 V and a current of 13.5 mA, so a resistance of 24.3/0.0135 = 1.8 kΩ is required.

Note, unlike some types of bias circuit, this type does not suffer from parasitic oscillations due to high loop gain.

3.1.2 Class-AB

Class-AB operation is characterized by a constant collector voltage and (unlike class-A) a quiescent collector current that increases with drive power. The distortion behaviour is also different to that of class-A. Class-AB operation is used for linear amplifiers with less severe requirements including:

- Final stages of SSB transmitters where a 2-tone *3rd*-order intermodulation of about −30 dB is required
- Final stages of TV transmitters where a gain compression of max. 1 dB is required
- Final stages of base stations for cellular radio.

Maximum efficiency is obtained at maximum power, and although the theoretical maximum efficiency of a class-AB amplifier is 78.5%, in practice it is always lower because:

- There are resistive losses both in the transistor and in the output matching circuit
- The collector AC voltage cannot be driven to its maximum value because of distortion requirements
- There is a small quiescent current (for a bipolar transistor, about 2% of the collector current at maximum power and, for a MOSFET, about 12% of the drain current at maximum power).

For HF and VHF amplifiers, in a 2-tone situation, the average efficiency is about 40% which corresponds to an efficiency of 60 to 65% at maximum power (PEP situation). At higher frequencies, the efficiencies are somewhat lower. The power gain of a class-AB amplifier is between those of class-A and class-B amplifiers.

3.1.2.1 DISTORTION

Unlike a class-A amplifier where intermodulation improves as the power is reduced, for a class-AB amplifier, the distortion is as shown in Fig.3-5.

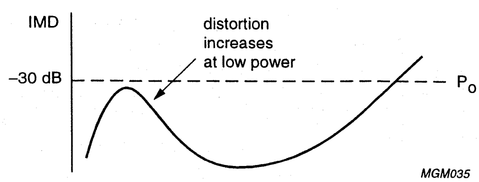

Fig.3-5 Intermodulation distortion as a function of output power for a class-AB amplifier.

The increasing distortion at low powers is due to ‘cross-over’ distortion, i.e., distortion during the transition from class-A to class-B operation.

3.1.2.1.1 EFFECT OF LOAD IMPEDANCE

An important factor affecting distortion is the load impedance. The optimum value at the fundamental frequency is always specified in Philips’ transistor data sheets for the frequency range of interest. The load reactance at the second harmonic is also important. Often, this is solely the output capacitance of the transistor. The collector or drain current contains a substantial second harmonic component which due to the presence of the load reactance causes a second harmonic output voltage component. A relatively small component can be tolerated. However, if it is above say 10% of the voltage at the fundamental frequency, the amplifier will saturate at a lower power than intended, so the allowable distortion is reached at lower power.

This can be solved by adding an external capacitor between collector (or drain) and earth. Though this will reduce gain and efficiency somewhat, it will reduce intermodulation significantly. A good practical rule is that the reactance of the parallel combination of internal and external capacitance at the second harmonic should be about 2.2 times the load resistance at the fundamental frequency. For wideband amplifiers, there is another solution which can be found in application reports, e.g. *“NCO8703”.*

3.1.2.2 BIASING

For MOS transistors, biasing is rather easy. In most cases, a resistive voltage divider is sufficient. If necessary, a diode or an NTC thermistor can be included in the lower branch to compensate for the negative t.c. of the gate voltage.

For bipolar transistors, a more sophisticated circuit is required. The circuit has to deliver a constant voltage of about 0.7 V (adjustable over a restricted range) and should have very low internal resistance. The latter is required to accommodate a wide range of ‘load’ currents (i.e. base drive currents for the RF transistor), whilst maintaining a nearly constant output voltage. Other desired properties are temperature compensation and the lowest possible current consumption. Figure 3-6 shows a circuit meeting these requirements.

The bias circuit has large negative feedback. If the load current increases, the output voltage drops slightly, decreasing the collector current of the BD135 whose collector voltage increases to counteract the drop in output voltage.

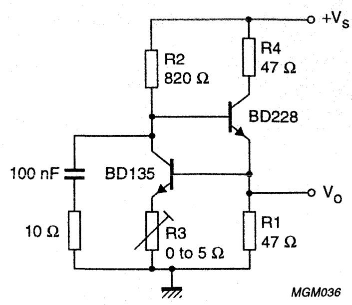

Fig.3-6 Bias circuit for a class-AB bipolar transistor amplifier.

3.1.2.2.1 DESIGN EXAMPLE

Calculation of component values

BD228 BASE AND COLLECTOR CURRENT

In this example, it is assumed that the bias circuit is for an amplifier delivering an output power of 100 W at a supply voltage of 28 V. So, if the minimum amplifier efficiency is 50%, the required DC input power is 200 W, corresponding to a collector current of 7.14 A. If the transistors used have a minimum h_{FE} of 15, the maximum base current can be 0.48 A. Such an amplifier could be the final stage of an SSB transmitter where the output power and therefore also the base current vary from almost zero to 0.48 A. In the bias circuit, a pre-loading resistor, R_1, is used to reduce the base current variations. To draw 15 mA at 0.7 V, R_1 must be 0.7/0.015 = 47 Ω. The maximum emitter current of the BD228 will then be nearly 0.5 A. From the published h_{FE} data for this type, the base current is 15 mA maximum.

The current through the collector resistor, R_2, of the BD135 is chosen to be twice this value, i.e. 30 mA, to restrict the variations in the collector current of the BD135. The V_{BE} of the BD228 is about 0.8 V, so the voltage across R_2 is 26.5 V, giving a value of: 26.5/0.03 = 883 Ω (nearest preferred value: 820 Ω, 1 W.)

OUTPUT VOLTAGE

At first sight, the choice of a BD135 in this circuit seems a bit overspecified for a transistor that has to draw only 30 mA. Yet this has been done deliberately because then the V_{BE} required by the BD135 is low (smaller than the bias voltage to be delivered to the RF amplifier.) The difference is corrected by the variable resistor, R_3, in the emitter of the BD135. The output voltage of the bias circuit, and thus the quiescent current of the RF amplifier, can now be adjusted. With a resistor of 5 Ω max., the output voltage can be adjusted by at least 100 mV, sufficient for this application.

PROTECTION RESISTOR

To protect the BD228 against the consequences of a short-circuit of the output voltage, it is advisable to include a resistor, R_4, in the collector lead. As the BD228 has a $V_{CE(sat)}$ of 0.8 V max., a voltage drop of 26.5 V across R_4 is allowed at the maximum collector current of 0.5 A. The maximum value of this resistor is therefore 26.5/0.5 = 53 Ω (nearest preferred value: 47 Ω.) Note that R_4 must be rated at 12 W ($I^2R = 0.5^2 \times 47 = 11.75$).

PERFORMANCE

The internal resistance of this bias circuit is exceptionally small. Values of less than 0.1 Ω have been measured, so the output voltage varies by less than 50 mV from zero to full load. The value of the output voltage is mainly determined by the V_{BE} of the BD135, which has a well-known temperature dependence (about −2 mV/°C), providing reasonable matching with the required V_{BE} of RF transistors without any special measures.

This type of bias circuit can develop parasitic oscillations near 1 MHz with highly capacitive loads (such as the supply decoupling capacitors in the RF circuit). This can be prevented by an RC combination between the collector of the BD135 and ground. Good values are 10 Ω and 100 nF.

3.1.3 Class-B

This class of operation can be used for all RF power amplifiers without linearity requirements, e.g. in portable and mobile radios, base stations (except those for the 900 MHz band) and FM broadcast transmitters.

For bipolar transistors, no biasing is required, i.e. $V_{BE} = 0$, while MOSFETS are used with very small quiescent drain current, say 2 to 3% of the current at full power. This can be provided in the same way as for class-AB amplifiers.

The collector (or drain) efficiency is about 70% at VHF, while the power gain depends on the frequency of operation.

3.1.4 Class-C

This class of operation is *not recommended for bipolar transistors,* because it shortens transistor life, see also Section 2.1.1: V_{EBO} rating. An exception can be made for a very small negative bias (<100 mV) which can be generated with a small resistor between base and emitter.

MOSFETS are more tolerant in this respect and can be adjusted at $V_{GS} = 0$, causing only a few dB reduction of power gain. This is not a problem in most cases because the gain is rather high. The main advantage is a higher drain efficiency. A good example is the BLF278 which at 108 MHz in class-B gives 70% efficiency at 22 dB gain, and in class-C, 80% efficiency at 18 dB gain.

3.1.5 Class-E

This class of operation is discussed in more detail in application report *"COE82101"*. With an optimum choice of component values for the output matching network of the transistor, collector or drain efficiencies of 85% can be reached. However, the use of class-E is restricted as beyond 60 to 70 MHz, efficiency falls significantly.

3.1.6 Influence of driver stages on intermodulation

Most linear amplifiers (i.e. class-A and class-AB) consist of a cascade of two or more amplifier stages. The overall distortion is mainly caused by the final stage because the driver stages are generally designed to have a lower distortion. In fact, attention to the design of the driver stage will pay dividends in overall performance as the following analysis illustrates.

The total distortion of a multi-stage amplifier, d_{tot}, can be determined from:

$$d_{tot} = 20\log\left(10^{d_1/20} + 10^{d_2/20} + ...\right)$$

where d_1, d_2 etc. are the intermodulation products of each stage in dB.

With two stages, e.g. driver plus a final stage, it is useful to know by how many dB the overall distortion worsens for a given difference in distortion between driver and final stage (assuming the driver distortion is the smaller). This relationship is described by:

$$B = 20\log\left(1 + 10^{-A/20}\right)$$

where:
A is the absolute difference in distortion between driver and final stage, and
B is the increase in distortion in the output of the amplifier.

This relationship is summarized in Table 3-1 for a few values. Clearly, if a large increase in distortion is unacceptable, the driver stage has to be substantially better than the final stage.

Table 3-1 Effect of driver distortion upon overall distortion

A Amount by which driver IMD is superior to final stage IMD (dB)	**B** Increase in IMD of output amp. (dB)
0	6.0
5	3.9
10	2.4
15	1.4
20	0.8

3.2 Matching

3.2.1 Narrow-band (test) circuits

NARROW-BAND MATCHING CIRCUITS

- *Section 3.2.1.1:* describes the principles of impedance matching
- *Section 3.2.1.2:* describes two types of adjustable network, and how to handle high power levels
- *Section 3.2.1.3:* deals with UHF versions of the networks of the previous section using striplines
- *Section 3.2.1.4:* discusses the double networks required for very-low transistor impedances
- *Section 3.2.1.5:* is on π-networks where the trimmers are grounded on one side to avoid 'hand effects'. VHF and UHF versions are given as well as the modifications for low-impedance transistors.

3.2.1.1 GENERAL REQUIREMENTS

Every transistor amplifier needs to be impedance matched both at its input and output. In test circuits, the 50 Ω signal source must be matched to the complex input impedance of the transistor. At the output, the reverse is needed, namely, the 50 Ω load resistance must be transformed to the optimum complex load impedance of the transistor.

In multistage amplifiers, networks are required in addition, to provide direct matching between two complex impedances. The most important requirement for all matching networks is that power losses must be minimized. In addition, especially for output networks, the voltage and current loading of the components must be taken into account.

Most matching networks have to be tunable, ideally with a large tuning range and with smooth, continuous control. Unfortunately, these are conflicting requirements so a compromise must be made.

In general, there are no severe requirements on the bandwidth of a matching network. However, it can be advantageous not to make this bandwidth too small, thereby improving the smoothness of the alignment and reducing losses.

The objective of matching is to maximize power transfer. This requires that the source and load impedances are complex conjugates, i.e. they have equal resistance components, and equal reactance components but of opposite sign.

The simplest form of matching between a source with a real (i.e. resistive) internal impedance and a different load resistance can be made using two reactive elements, see Fig.3-7.

In Fig.3-7, A and B have low-pass characteristics and are most commonly used because of their suppression of harmonic components. C and D have high-pass characteristics and, although used less frequently, have advantages in specific cases such as interstage networks.

The higher resistance is denoted by R_h and the lower by R_l. R_h always has a parallel reactance (X_p) and R_l a series one with opposite sign (X_s).

The component values can be easily calculated from:

$$\frac{X_s}{R_l} = Q = \frac{R_h}{X_p} \qquad (1)$$

and

$$\frac{R_h}{R_l} = Q^2 + 1 \qquad (2)$$

where Q is the *loaded* Q-factor which has to be small compared with the *unloaded* Q-factor of the components.

Note: Equations (1) and (2) are used on many occasions in subsequent sections to determine component values in networks.

Up to now, we have only considered matching two different value *resistances*. In practice, at least one of the impedances is complex, and in such cases, one of the reactances, namely the one closest to the complex impedance, has to be modified.

Suppose that in Fig.3-7, circuit A is used for the input matching of a transistor. If the transistor's input impedance is capacitive, X_S has to be increased by the absolute value of the transistor's input reactance as Fig.3-8 shows. If the input impedance is inductive, the reverse is needed: X_S has to be reduced by this amount. Note, if in the latter case the input reactance of the transistor is higher than the calculated X_S, the new X_S becomes negative, meaning a capacitor has to be used instead of an inductor.

Similar considerations hold for the other configurations.

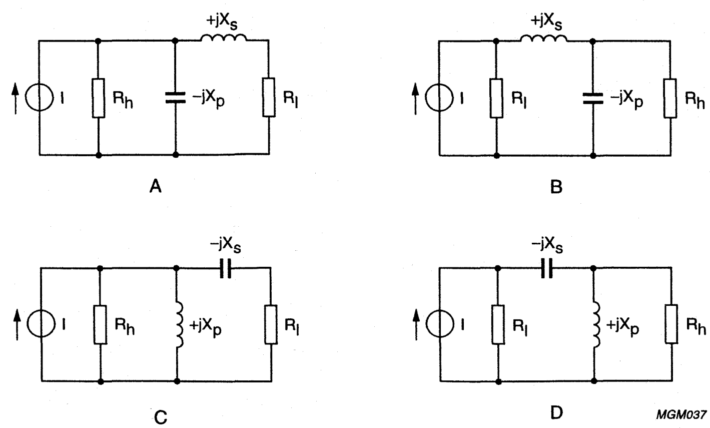

Fig.3-7 Four examples of matching a resistive source and load using two reactive elements.

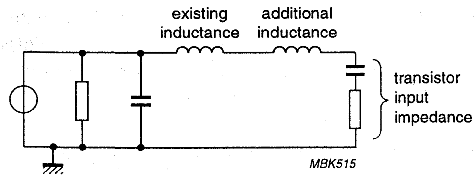

Fig.3-8 Adding a series inductance to the input matching circuit A of Fig.3-7 to compensate for the capacitive part of a transistor's input impedance.

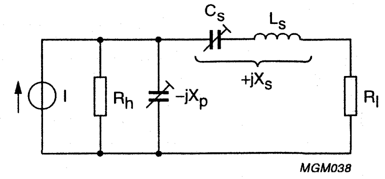

Fig.3-9 Adjustable matching network (based on circuit A of Fig.3-7) suitable for test circuits. A similar network can be made based on circuit B of Fig.3-7.

3.2.1.2 ADJUSTABLE L AND T NETWORKS[(1)]

Owing to their limited control options, the networks described in the previous section are not really suitable for use in test circuits. This limitation can be overcome in two ways by simple circuit modifications.

3.2.1.2.1 NETWORK 1

Starting from circuits A (high-to-low transformation) and B (low-to-high transformation) of Fig.3-7, X_p is made (partly) variable by using a trimmer (optionally with a fixed capacitor in parallel to lower the trimmer current and for smoother control). In addition, a variable capacitor is connected in series with X_s such that the combination remains inductive. (C_s can again be the parallel combination of a trimmer and a fixed capacitor). This means the inductance has to be increased to keep the combination's reactance at the calculated value of X_s, see Fig.3-9.

For the modified network, the new Q-factor for L_s is

$$Q' = \frac{\omega L_s}{R_l}$$

And since L_s has increased, Q' is higher than the Q defined in the previous section, meaning the circuit losses are higher and the bandwidth is lower. Therefore, these effects must be reduced as much as possible by restricting the increase in L_s.

3.2.1.2.2 NETWORK 2

A variant of network 1 is shown in Fig.3-10. This circuit uses smaller capacitances than the circuit of Fig.3-9. And though the harmonic suppression is worse, this can usually be tolerated in input networks.

The calculation of component values is done in two stages. To assist understanding, it is best to imagine this circuit as two cascaded sections (D plus A from Fig.3-7), see Fig.3-11. The first section transforms R_h to a higher value at point A, and the second transforms this value down to R_l. To restrict the losses and reduction of bandwidth, it is advisable to choose the equivalent parallel resistance at point A no higher than necessary. When making the calculation, note that the combined reactance of L_p' and C_p' is always negative (C_p' dominates), so the combination can be realized by a (variable) capacitor.

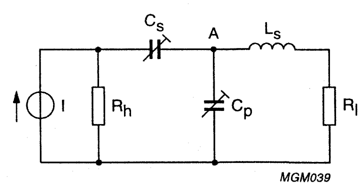

Fig.3-10 Variant of the matching network shown in Fig.3-9.

(1) Note: Many of the networks in Section 3.2 are 'reversible'.

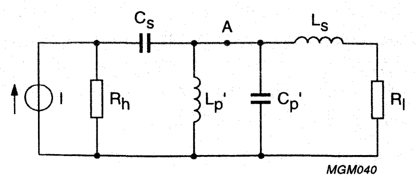

Fig.3-11 The matching network of Fig.3-10 represented as two cascaded sections to simplify calculation.

Another possibility is a combination of networks 1 and 2. This is sometimes used in output networks that must handle relatively high power, see Fig.3-12.

The purpose of C_{p1} is to drain some, say half, of the RF current to ground so that the current through C_s and C_{p2} becomes proportionally smaller, allowing components of a lower rating to be used.

The equivalent parallel resistance at point A should be 2 to 3 times R_h which determines the value of L_s (from equations (1) and (2), the resistance ratio determines the Q, and $X_s = QR_l$). Next, choose a value for C_{p1} that is about half that required to transform R_l to the resistance at point A.

Looking from point A to the left (but including C_{p1}), we see an inductive impedance: R + jX, where $R > R_l$. The remaining part of the calculation is then the same as for network 1.

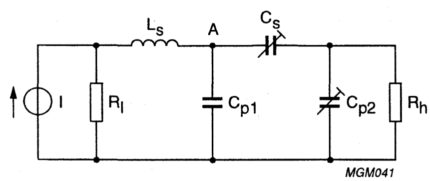

Fig.3-12 Matching network formed by combining those shown in Figs.3-9 and 3-10.

With these and the following networks, it is often needed to transform an impedance from series to parallel components or vice versa. For such transformations, the equations given in the previous section for calculating L-networks can be used with R_l as the series resistance component and R_h as the parallel resistance component.

3.2.1.3 UHF NETWORKS

Above 300 MHz, it is not very practical to work with coils, so transmission lines in the form of striplines are preferred, see Fig.3-13. As well as having series inductance, striplines have parallel capacitance which transforms the real part of the load impedance, calling for a modified calculation.

Figure 3-13 is very similar to the right-hand part of the circuit shown in Fig.3-10. The (low) load impedance is known, but note that its imaginary part can be positive or negative depending on the transistor. And R_{ip} is chosen in the same manner as the resistance at point A in network 2, Section 3.2.1.2.

Next, choose the characteristic resistance of the stripline to satisfy the condition:

$$R_c > \sqrt{R_{ls}R_{ip}}$$

The exact value of R_c is set by practical considerations as both very narrow and very broad striplines are undesirable.

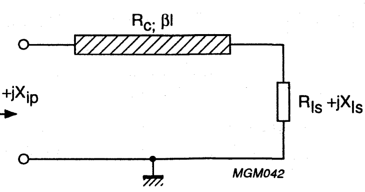

Fig.3-13 Representation of a stripline used in UHF matching networks.

It's now possible to calculate the electrical length (βl) and the parallel input reactance (X_{ip}) from the following two equations:

$$\tan \beta l = \frac{-b + \sqrt{b^2 - 4ac}}{2a}$$

where:

$a = R_c^2 - R_{ls}R_{ip}$

$b = 2R_c X_{ls}$

$c = R_{ls}^2 + X_{ls}^2 - R_{ls}R_{ip}$

and:

$$X_{ip} = \frac{R_{ls}R_{ip}}{X_{ls} + \tan \beta l \left(R_c - \dfrac{R_{ls}R_{ip}}{R_c} \right)}$$

The values of the (variable) capacitors are calculated as described in Section 3.2.1.2.

3.2.1.4 DOUBLE NETWORKS

In some cases, the input and/or load impedance of the transistor is so low that a direct transformation, as just described in Section 3.2.1.3, leads to very high values of the loaded Q-factor with all its negative consequences. It is then better to add an extra (fixed) section as shown in Figs 3-14 and 3-15.

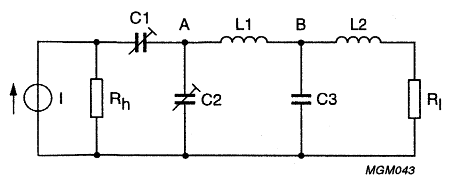

Fig.3-14 Adding a fixed section to the network of Fig.3-10 avoids high loaded Q-factors.

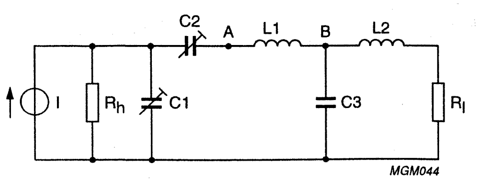

Fig.3-15 Circuit with the fixed section added to the alternative network of Fig.3-9.

Suppose that $R_h = 50\ \Omega$ and $R_l = 1\ \Omega$. A suitable value for the equivalent parallel resistance at point A is then 100 to 150 Ω (i.e. more than 50 Ω, but not so big in view of circuit losses and bandwidth). At point B, a value which is the geometric mean of that at point A (say 125 Ω) and R_l is required, namely $\sqrt{(125 \times 1)} = 11.2\ \Omega$.

Without the double network, the loaded Q is:
$\sqrt{(125 - 1)} = 11.1$

and with the double network, it is :
$\sqrt{(11.2 - 1)} = 3.2$ which is a significant improvement.

This double network variant also has advantages for output networks. Furthermore, by replacing some or all of the coils by striplines, it can be used at higher frequencies.

3.2.1.5 PI-NETWORKS

3.2.1.5.1 FOR THE VHF RANGE

The networks considered up to now have used both parallel and series capacitors. This can be undesirable because of the so-called 'hand-effect' (the influence of an operator's capacitance) when adjusting a variable capacitor with an RF signal on both sides of it. This effect is present even when an insulated adjuster is used. An alternative method of impedance matching which uses only parallel capacitors overcomes this problem, see Fig.3-16.

If R_l is the low transistor output impedance and R_h the 50 Ω load resistance, then we start by transforming R_l up to about 50 Ω by the fixed section L_1-C_1. This fixed section is followed by a Pi-network C_2-L_2-C_3 which can transform the impedance either up or down as required, and the Pi-network component values are calculated as follows (see Fig.3-17).

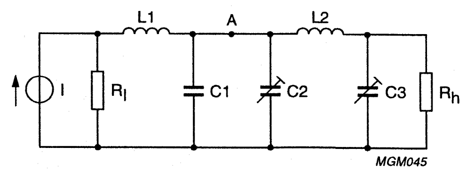

Fig.3-16 Impedance matching circuit using only *parallel* capacitors.
This arrangement in which only one side of the capacitor is 'hot' allows manual tuning on the grounded side of the capacitor, avoiding the 'hand-effect'.

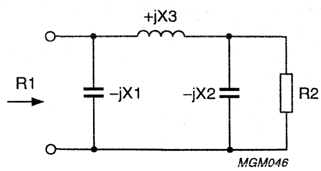

Fig.3-17 Pi-network circuit for the calculation when both R_1 and R_2 have fixed values.

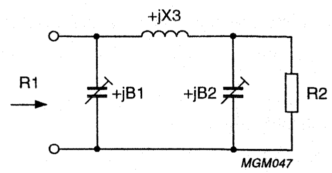

Fig.3-18 Pi-network circuit for the calculation with adjustable input resistance, R_1. R_2 is fixed, e.g. 50 Ω.

For the condition: $X_3 \le \sqrt{R_1 R_2}$,

$$X_1 = \frac{R_1 X_3}{R_1 + \sqrt{R_1 R_2 - X_3^2}}$$

and

$$X_2 = \frac{R_2 X_3}{R_2 + \sqrt{R_1 R_2 - X_3^2}}$$

In most cases however, we want to adjust the input resistance by varying X_1 and X_2, for example, to suit different transistors and for maximum power transfer. Figure 3-18 shows a suitable network in which, for mathematical convenience, susceptances ($B = \omega C$) have been used instead of reactances.

The value required for X_3 is determined by the minimum value of R_1:

$$X_3 = \sqrt{R_{1\,min} R_2}$$

$$B_{1\,min} = B_{2\,min} = \frac{1}{X_3}$$

$$\Delta B_1 = \frac{1}{2R_{1\,min}}$$

and

$$\Delta B_2 = \frac{\sqrt{\frac{R_{1\,max}}{R_{1\,min}} - 1}}{R_2}$$

So both capacitors have the same minimum value but generally a different control range (Δ).

The losses in this type of Pi-network are in general somewhat higher than those in the networks discussed earlier. The losses increase as the difference between R_1 (avg.) and R_2 increases and as the control range increases since in both cases the loaded Q of the components increases.

The losses can be kept within reasonable limits if the average value of R_1 is within a factor of 2 (up or down) of R_2 (i.e. $R_2/2 < R_1 < 2R_2$). For the control range of R_1, a factor of 4 (total) is generally suitable, providing a control factor of 2 (up and down) from the nominal value.

3.2.1.5.2 FOR THE UHF RANGE

The network just described can also be made in a stripline version, see Fig.3-19.

The characteristic resistance of the stripline must satisfy the condition:

$$R_C > \sqrt{R_{1\,min} R_2}$$

Then the other quantities become:

$$\tan \beta l = \frac{1}{\sqrt{\frac{R_c^2}{R_{1\,min} R_2} - 1}}$$

$$B_{1\,min} = B_{2\,min} = \frac{1}{R_c \tan \beta l}$$

$$\Delta B_1 = \frac{1}{2R_{1\,min}}$$

$$\Delta B_2 = \frac{\sqrt{\frac{R_{1\,max}}{R_{1\,min}} - 1}}{R_2}$$

So clearly this stripline network has much in common with the previous one.

3.2.1.5.3 PI-NETWORK MODIFICATIONS FOR LOW-IMPEDANCE TRANSISTORS

If the transistor impedance is very low (say <5 Ω) as occurs in high power situations, there are two options:

1. Make the average value of R_1 lower than R_2, e.g. half of R_2
2. Use two pre-matching sections instead of one. If this is done, make the impedance between the two sections equal to the geometric mean of the transistor impedance and the average input resistance of the Pi-network.

3.2.2 Wideband circuits

WIDEBAND HF MATCHING CIRCUITS OVERVIEW

HF range *(Section 3.2.2.1)*

– Describes the procedures for input/output matching of MOS and bipolar transistors. Most attention is paid to MOS devices as they are usually the preferred choice for HF applications.

– *Section 3.2.2.1.1* describes some output compensation circuits. Output compensation aims to maintain the ideal load impedance over the frequency band of interest to obtain the highest efficiency and lowest distortion. This section explains:

  * How to compensate a transistor's output capacitance with one or two elements - the latter giving superior results
  * How to compensate parallel inductances such as RF chokes and/or transformer inductance to improve performance at the lower end of the band, and the selection of compensation (coupling) capacitor(s).

– *Section 3.2.2.1.2* deals with the design of input networks to obtain low input VSWR, and high, flat power gain over the whole frequency band.

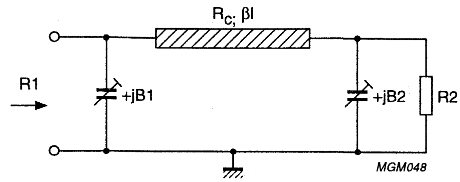

Fig.3-19 Stripline version of the Pi-network of Fig.3-18.

3.2.2.1 THE HF RANGE

This frequency range covers 1.6 to 28 MHz. Most transmitters in this range work with single sideband modulation and wideband power amplifiers. The impedance transformation in these amplifiers can be done either by transmission line type transformers or by compensated conventional transformers (extensively described in application reports *"ECO6907"* and *"ECO7213"*).

In addition, a number of compensation techniques can be used at both output and input. For the former, this is done to obtain maximum output power and efficiency over the whole frequency band; for the latter, it's done to obtain maximum and flat power gain and good impedance matching over the band.

3.2.2.1.1 COMPENSATION AT THE OUTPUT

Compensation of output capacitance

Take as an example the BLF177 MOS transistor. From the published data sheet, this has an output capacitance of 190 pF which rises at full power by about 15% to 220 pF. The capacitor reactance at 28 MHz is about four times the load resistance of 6.25 Ω. Without compensation, the output VSWR is 1.28 which is rather high. To reduce this VSWR, one or two external components can be used. Compensation with one element is shown in Fig.3-20. Two elements will of course give a better result than one, and is described later.

These compensation examples make use of Chebyshev filter theory where it is usual to express the values of the filter elements normalized to a characteristic resistance (source and/or load resistance) of 1 Ω and to a cut-off (angular) frequency, ω, of 1 rad/s. For a low-pass filter, 1 rad/s is the maximum angular frequency, and for a high-pass filter the minimum. Normalized quantities are denoted by g_k where k is a filter-element identifier (Ref.1).

Single-element compensation

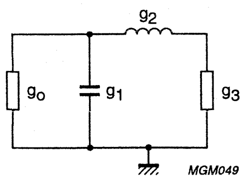

Fig.3-20 Output capacitance compensation using one element.
g_o: optimum load resistance;
g_1: output capacitance of device.

In the circuit of Fig.3-20, the filter elements are:

g_o: the optimum load resistance (known);

g_1: the output capacitance of the device (known);

g_3: the real load resistance, and

g_2: the compensating element inductance.

In normalized form, we can express these quantities as:

$$g_1 = \frac{\sqrt{2}}{\gamma}$$

$$g_2 = \frac{\sqrt{2}\gamma}{1+\gamma^2}$$

$$g_3 = \frac{g_0\gamma^2}{1+\gamma^2}$$

where γ is an intermediate quantity (mathematically related to the maximum VSWR in the pass-band) used to simplify the calculations.

From the above, it follows that:

$$g_2 = \frac{2g_1}{g_1^2+2}$$

In general, $g_1 << 1$, so $\gamma >> 1$ and as a result, $g_3 \sim g_o$.

(De)normalization can be done using:

$g_o = R$

$g_1 = \omega CR$

$g_2 = \omega L/R$

where: ω is the *maximum* angular frequency, and the maximum VSWR is g_o/g_3.

In the example with the BLF177:

$g_1 = 1/4$

$g_2 = 0.2424$ (normalized value), so L = 8.61 nH.

Therefore, the VSWR is 1.031 - a substantial improvement. And though not necessary in this case, it can be made better still as required in driver stages for which compensation with two elements, see Fig.3-21, is preferred.

Two-element compensation

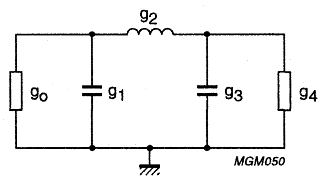

Fig.3-21 Output capacitance compensation using two elements.

The calculation is similar to that just described, so in normalized form:

$g_o = g_4$

$$g_1 = g_3 = \frac{1}{\gamma}$$

$$g_2 = \frac{2\gamma}{\gamma^2+\frac{3}{4}}$$

From this, it follows that:

$$g_2 = \frac{8g_1}{3g_1^2+4}$$

Normalization and denormalization is done using:

$g_0 = g_4 = R$

$g_1 = g_3 = \omega CR$

$g_2 = \omega L/R$

where ω is again the *maximum* angular frequency.

The maximum VSWR is calculated as follows. For the calculation, it is necessary to introduce a term k where:

$k = \gamma + \sqrt{(\gamma^2 + 1)}$

Then:

$$\mathrm{VSWR} = \left(\frac{k^3 + 1}{k^3 - 1}\right)^2$$

In the example with the BLF177:

$g_1 = 1/4$

$\gamma = 4$

$g_2 = 0.4776$ (so L = 17 nH)

Therefore, the VSWR = 1.007.

This is principally the same as the HF compensation of a conventional transformer. The only difference is that in the latter case the stray inductance is known and the compensation capacitors have to be calculated.

Compensation of parallel inductances

COMPENSATING ONE PARALLEL INDUCTANCE

It is also worthwhile compensating for the parallel inductances of the RF choke and output transformer found in most amplifiers as their reactances at 1.6 MHz are often about four times the load resistance. In most cases, compensation is provided by the coupling capacitor(s).

There are also simpler situations where either the RF choke or the impedance transformer is missing. We will start with this case and the equivalent circuit is given in Fig.3-22.

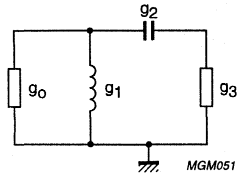

Fig.3-22 Compensation of an RF choke.

This circuit looks much the same as the HF compensation scheme, with the L and the C interchanged. Mathematically, there is also much in common - only the normalized values have to be inverted. So, for the reactive elements:

$$g_1 = \frac{\gamma}{\sqrt{2}}$$

$$g_2 = \frac{1 + \gamma^2}{\sqrt{2}\gamma}$$

$$g_3 = \frac{g_0 \gamma^2}{1 + \gamma^2}$$

From these, it follows that:

$$g_2 = \frac{1 + 2g_1^{\ 2}}{2g_1}$$

In general, g_1 and γ are >>1, so $g_3 \sim g_0$.

Normalization and denormalization are done using:

$g_0 = R$

$g_1 = \omega L/R$

$g_2 = \omega CR$

where ω is the *minimum* angular frequency, and the maximum VSWR is again g_0/g_3.

COMPENSATING TWO PARALLEL INDUCTANCES

If we have to compensate two parallel inductances of approximately equal value, the equivalent circuit is as shown in Fig.3-23.

Inverting the normalized values for the reactive elements gives:

$g_0 = g_4$

$g_1 = g_3 = \gamma$

$$g_2 = \frac{\gamma^2 + \frac{3}{4}}{2\gamma}$$

From these, it follows that:

$$g_2 = \frac{4g_1^{\ 2} + 3}{8g_1}$$

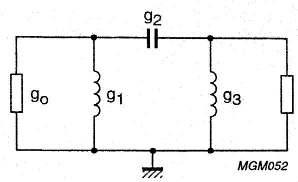

Fig.3-23 Compensation of an RF choke and impedance transformer.

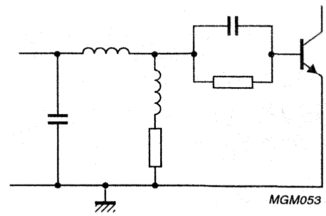

Fig.3-24 Compensation circuit of a bipolar transistor input. An example is given in report *"AN98030"*.

Normalization and denormalization is done using:

$g_0 = g_4 = R$

$g_1 = g_3 = \omega L/R$

$g_2 = \omega CR$

where ω is the *minimum* angular frequency and the maximum VSWR is determined in the same way as in the HF situation. So, if $k = \gamma + \sqrt{(\gamma^2 + 1)}$ as defined earlier:

$$VSWR = \left(\frac{k^3+1}{k^3-1}\right)^2$$

In the example with a BLF177:

$g_1 = 4$

$\gamma = 4$

$g_2 = 2.094$

Therefore, the VSWR = 1.007

For R = 6.25 Ω and f = 1.6 MHz, we get C = 33 nF.

3.2.2.1.2 COMPENSATION AT THE INPUT

For bipolar transistors, the variations in power gain and input impedance can be compensated with an R-L-C network as decribed in application report *"AN98030"*, and shown in Fig.3-24. The network was designed using a circuit analysis program with an optimization facility.

For MOS transistors, the behaviour of the input impedance is quite different. The main problem here is providing a constant voltage across a rather high input capacitance (for the BLF177: about 745 pF) over the frequency range. At the same time, we want good matching at the input *and* the highest power gain.

Simply connecting a resistor across the transistor input does not produce good results. Better solutions, the simplest of which is described here (see Fig.3-25), are required. The more advanced ones will be discussed later where their superior performance is really needed.

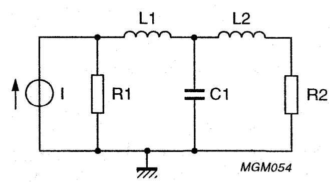

Fig.3-25 Circuit providing simple input compensation of a MOS transistor.

In Fig.3-25, the (transformed) driving generator is represented by the combination I-R_1, and the input capacitance of the transistor by C_1. The compensation components are: L_1, L_2 and R_2. R_2 should approximately equal R_1. In addition, the voltage across C_1 should not differ much from that across R_1. As the required voltage across C_1 is a given quantity, we shall design a circuit with the highest possible value of R_1 to obtain the lowest possible drive power.

Computer optimization programs can be used to investigate what happens when the product R_1C_1 is increased. The aims of optimization are to:

- Minimize the input VSWR over the frequency band, and
- Minimize the variation of the voltage across C_1 over the same band.

Table 3-2 gives the normalized results from such a program.

Table 3-2 Effect of varying ωC_1R_1 in the compensation circuit of Fig.3-25

ωC_1R_1	$\omega L_1/R_1$	$\omega L_2/R_1$	R_2/R_1	$VSWR_{max}$	ΔG(dB)
0.8	0.437	0.305	0.961	1.21	0.19
1.0	0.515	0.388	0.939	1.34	0.31
1.2	0.571	0.473	0.908	1.51	0.44
1.4	0.619	0.568	0.867	1.74	0.64

ω is the maximum angular frequency, and ΔG the maximum deviation from the average gain.

From Table 3-2, clearly, a good practical choice is $\omega C_1R_1 = 1.0$. For the BLF177, this means that R_1 can be 7.6 Ω maximum. For ease of transformation, we chose 6.25 Ω.

The input impedance of the transistor is not of course a pure capacitance. It also has some series resistance and inductance, so reoptimization is necessary to take account of the real input impedance and power gain of the transistor as a function of frequency.

For driver stages operating at a low power level, negative feedback is sometimes used: an emitter resistor and a collector-base resistor for bipolar devices (with in some cases an inductance in series with the latter to reduce feedback at the high end of the frequency band).

Similarly, for MOS transistors, a resistor is connected between drain and gate. A resistor is not required in the source lead however. The advantage of this feedback method is lower intermodulation distortion. The feedback must not be too large however as such a resistor consumes part (albeit a small part) of the output power.

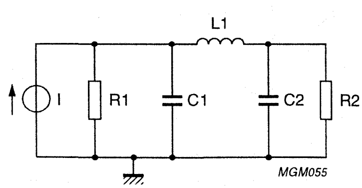

Fig.3-26 Equivalent circuit of output compensation for the lower VHF range.

3.2.2.2 *THE LOWER VHF RANGE*

WIDEBAND VHF MATCHING CIRCUITS OVERVIEW

Lower VHF range *(Section 3.2.2.2)*

- Though the same circuit configurations used for HF can be used in this range, the higher maximum frequency requires modified component values.
- *Section 3.2.2.2.1* describes two circuits that compensate for output capacitance.
- *Section 3.2.2.2.2* describes two input networks using more compensation elements than the HF version for higher power gain.

Upper VHF range *(Section 3.2.2.3)*

- Describes impedance matching (input and output) for this range using low-pass L-sections, with an optional high-pass section.
- *Section 3.2.2.3.1* describes a single low-pass section, sufficient for low impedance ratios and/or moderate bandwidths. To meet more stringent requirements, two or three sections are required. *Section 3.2.2.3.2* outlines several approaches, some suitable for interstage networks.
- Finally, the effect of non-ideal network components is discussed.

Some military communications transmitters operate in this range. The lowest frequencies used are 25 to 30 MHz and the highest 90 to 110 MHz.

Power amplifiers for this range are similar to those for the HF range. However, impedance matching can only be done with transmission line transformers as described in application report *"ECO7703"*. In addition, more complex methods are required for RF compensation at both output and input.

3.2.2.2.1 COMPENSATION AT THE OUTPUT

The output compensation systems described in Section 3.2.2.1.1 provide adequate results in the HF range. For the lower VHF range, somewhat better results can be obtained simply by modifying the component values. The equivalent circuit is shown in Fig.3-26.

First, let $R_1 = R_2$; C_2 does not however have to equal C_1. Computer optimization for lower VHF yields the results shown in Table 3-3.

The practical limit of usefulness is at $\omega C_1R_1 = 1.0$. If we use this condition with the Chebyshev system described earlier, then the maximum VSWR would be 1.33 instead of 1.29.

Table 3-3 Computer optimization results of the compensation circuit of Fig.3-26 for the lower VHF range

ωC_1R_1	ωC_2R_1	$\omega L_1/R_1$	$VSWR_{max}$
0.6	0.549	0.914	1.08
0.8	0.693	1.04	1.17
1.0	0.827	1.10	1.29
1.2	0.965	1.12	1.44

ω is the maximum angular frequency. $R_1 = R_2$.

With this compensation, we can go one step further by dropping the requirement that R_2 has to equal R_1. Doing this and optimizing again yields the results shown in Table 3-4.

As Table 3-4 shows, for $\omega C_1R_1 = 1.0$, the maximum VSWR is improved to 1.25, and the corresponding value of R_2 is now smaller than R_1. Whether this is an advantage or not is difficult to say as it is dependent on the desired combination of supply voltage and output power as well as on the possible transformer ratios.

Table 3-4 Computer optimization results of the compensation circuit of Fig.3-26 for the lower VHF range. $R_1 \neq R_2$

ωC_1R_1	ωC_2R_1	$\omega L_1/R_1$	R_2/R_1	$VSWR_{max}$
0.6	0.468	0.818	0.939	1.08
0.8	0.615	0.922	0.897	1.16
1.0	0.738	0.943	0.838	1.25
1.2	0.886	0.943	0.783	1.36

ω is the maximum angular frequency, and $R_1 \neq R_2$.

3.2.2.2.2 INPUT NETWORKS

For bipolar transistors, it should be possible to use the same type of compensation network used for the HF range in the lower VHF range. However, we shall restrict our considerations to input networks for use with MOS devices.

The problem is the same as for the HF range (maintaining a constant voltage across a capacitance over a wide frequency range, see Section 3.2.2.1.2), but with a substantially higher maximum frequency. So, a more efficient compensation network is needed, requiring more components. The first of two examples is shown in Fig.3-27.

C_2 represents the input capacitance of the transistor. The results obtained by computer optimization are shown in Table 3-5.

Compared with the network described earlier (Fig.3-25 and Table 3-2), there is substantial improvement because ωR_1C_2 can certainly be increased up to 1.6, compared with 1.0 for the simpler network, providing higher gain for a given bandwidth.

A second circuit configuration producing as good or even superior results is shown in Fig.3-28. Here, the input capacitance of the transistor is represented by C_1. Computer optimization yields the results summarized in Table 3-6.

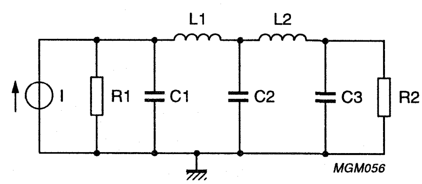

Fig.3-27 Example of an improved compensation circuit for the lower VHF range.

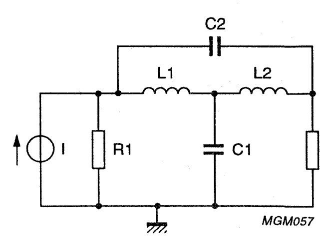

Fig.3-28 Second example of an improved compensation circuit for the lower VHF range.

Table 3-5 Computer optimization results of the compensation circuit of Fig.3-27

ωR_1C_2	ωR_1C_1	ωR_1C_3	$\omega L_1/R_1$	$\omega L_2/R_1$	R_2/R_1	$VSWR_{max}$	ΔG (dB)
1.0	0.460	0.501	0.870	0.836	1.02	1.10	0.10
1.2	0.602	0.496	1.02	0.836	1.00	1.14	0.15
1.4	0.751	0.485	1.11	0.836	0.977	1.21	0.20
1.6	0.887	0.476	1.15	0.845	0.955	1.31	0.28
1.8	0.993	0.482	1.15	0.870	0.934	1.42	0.38

ω is the maximum angular frequency and ΔG the maximum deviation from the average gain.

Table 3-6 Computer optimization results of the compensation circuit of Fig.3-28

ωC_1R_1	ωC_2R_1	$\omega L_1/R_1$	$\omega L_2/R_1$	R_2/R_1	$VSWR_{max}$	ΔG (dB)
1.0	0.591	0.392	0.336	0.977	1.12	0.11
1.2	0.597	0.447	0.396	0.972	1.15	0.13
1.4	0.604	0.504	0.462	0.966	1.19	0.16
1.6	0.584	0.584	0.536	0.961	1.21	0.18
1.8	0.584	0.662	0.611	0.955	1.23	0.20
2.0	0.574	0.794	0.733	0.934	1.21	0.36

ω is the maximum angular frequency and ΔG the maximum deviation from the average gain.

Comparing these results with those of the previous case, we see that the product ωC_1R_1 can be increased to 1.8 and possibly to 2.0. So, this configuration, even though it uses one component fewer, is better. Experience shows that circuits using inductive coupling between L_1 and L_2 do not improve the VSWR and gain variation performance.

As mentioned earlier, the input impedance of a MOS transistor can be represented by a capacitance, inductance and resistance in series. At high power levels in particular, the resistance cannot be neglected.

As a guideline, reoptimization is necessary when the values of input VSWR and gain variation are inferior to those in Tables 3-2, 3-5 and 3-6.

3.2.2.3 THE UPPER VHF RANGE

To get an idea of the impedance levels in this frequency range, consider a BLF225 MOS transistor able to deliver 30 W at 175 MHz from a 12.5 V supply voltage (Note, bipolar devices for the same range have similar impedance levels).

Suppose that the BLF225 is used in a mobile radio transmitter for the range 132 to 174 MHz. The optimum load impedance is about 2.5 Ω with a rather small reactive component. At the transistor input, there is an effective capacitance of 215 pF in series with a resistance of 3.2 Ω and a small inductance of 0.21 nH.

In the literature, most networks for wideband impedance matching are based on pure resistances. So, we have to start by making the impedance at the input approximately real. In theory, this can be done with either a parallel or a series inductance. Though the former should be preferable as it provides a higher impedance, unfortunately, a small inductance in parallel with the input of a transistor can cause large parasitic oscillations. Therefore, we have to use a series inductance, giving a tuned circuit with a loaded Q-factor of 1.53 in the middle of the frequency band. The relative width of this band ($\Delta f/f_0$) is 27 to 28% . If the product of loaded Q-factor and relative bandwidth is much less than 1, as in this case, the matching will not be affected significantly.

The remaining task is to match resistances of 3.2 Ω and 2.5 Ω to a 50 Ω source and load over the range 132 to 174 MHz. The most popular type of network for this purpose comes from G.L. Matthaei (Ref.2) where the matching is obtained from one or more low-pass L-sections (the more sections, the lower the VSWR in the pass-band).

The essence of this method is that there are several frequencies in the pass-band at which exact matching occurs. The number of exact matches is equal to the number of sections.

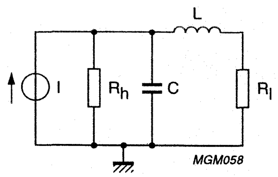

Fig.3-29 Single-section matching network for the upper VHF range.

3.2.2.3.1 SINGLE-SECTION MATCHING

First consider when there is just one section, Fig.3-29. R_h is the higher of the two resistances and R_l the lower. Exact matching takes place at:

$$f_0 = \sqrt{\frac{1}{2}\left(f_l^2 + f_h^2\right)}$$

where f_l is the lower limit of the band and f_h the upper one.

L and C can be calculated in the same way as described in Section 3.2.1.1. The maximum VSWR in the pass-band follows from the input impedance at one of the band limits.

The results of the calculation for the output, where 2.5 Ω must be matched to 50 Ω, are:

f_0 = 154.4 MHz

L = 11.23 nH

C = 89.84 pF

VSWR = 2.974.

The VSWR calculation is rather complex and is best done using a circuit analysis program. The high VSWR obtained here indicates that one section is not sufficient. Therefore, we shall now consider some possibilities with two sections.

3.2.2.3.2 TWO-SECTION MATCHING

Two low-pass sections

If both sections are low-pass, the situation is as shown in Fig.3-30.

Exact matching takes place at f_1 and f_2 ($f_2 > f_1$) and:

$$f_1 = \frac{1}{2}\sqrt{(2+\sqrt{2})\,f_l^2 + (2-\sqrt{2})\,f_h^2} \text{ and}$$

$$f_2 = \frac{1}{2}\sqrt{(2-\sqrt{2})\,f_l^2 + (2+\sqrt{2})\,f_h^2}$$

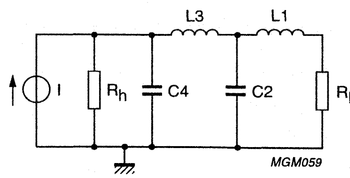

Fig.3-30 Two-section matching network for the upper VHF range.

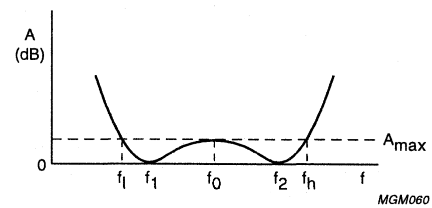

Fig.3-31 Pass-band characteristic of the two-section matching circuit of Fig.3-30.

There is maximum attenuation at the band limits, but also at:

$$f_0 = \sqrt{\frac{1}{2}\left(f_l^2 + f_h^2\right)}$$

The pass-band characteristic is shown in Fig.3-31.

To determine the values of the components, we need to define an auxiliary quantity M where:

$$M = L_1C_2 = \frac{\sqrt{1 - \frac{R_h}{R_l}}}{\omega_1\omega_2}$$

in which $\omega_1 = 2\pi f_1$
and $\omega_2 = 2\pi f_2$.

Then, for the circuit of Fig.3-30:

$$L_1 = \sqrt{\frac{-p}{2} + \sqrt{\frac{p^2}{4} - q}}$$

where:

$p = -R_l \{MR_h(\omega_1^2M - 2) + (R_h - R_l)/\omega_1^2\}$, and

$q = -M^2R_l^3R_h$

And, for the other components:

$C_2 = M/L_1$

$L_3 = C_2R_lR_h$

$C_4 = L_1/(R_lR_h)$.

To calculate the maximum VSWR in the pass-band, the procedure used for single-section matching must again be followed.

For this example, where we need to match from 2.5 to 50 Ω in the frequency range 132 to 174 MHz, we obtain:

$f_1 = 138.9$ MHz	$C_2 = 197.4$ pF
$f_2 = 168.5$ MHz	$L_3 = 24.67$ nH
$L_1 = 5.343$ nH	$C_4 = 42.74$ pF

The maximum VSWR (from the circuit analysis program) in the pass-band is now 1.173, which is a far better result than with one section (2.974).

Though the calculation procedure described above is rather complicated, direct use of the Matthaei method (Ref.2) is not simple either because:

- Interpolation is required both for impedance ratio and relative bandwidth
- Denormalization must be used, and
- Insertion loss must be converted to VSWR.

One low-pass and one high-pass section

Another method of wideband impedance matching is described by U. Fleischmann. (Refs 3, 4 and 5). In this method, two L-sections are used: one low-pass, the other high-pass. Both sequences are possible, and the resulting pass-band characteristic is almost equal to that of the previous case with two sections. To simplify calculation, we need to define several quantities:

$$f_0 = \sqrt{f_l f_h}$$

where f_l and f_h are the lower and upper limits of the frequency band respectively.

$$d = \frac{f_h - f_l}{f_0}$$

$$m = \frac{R_h}{R_l}$$

$$\varepsilon = \frac{-d^2\sqrt{m}}{4} + \sqrt{\left(\frac{d^2\sqrt{m}}{4}\right)^2 + \left(\frac{d^2+2}{2}\right)}, \text{ and}$$

$k = \varepsilon\sqrt{m}$.

Now we are able to calculate the normalized component values, first for when the low-pass section is adjacent to the lower resistance, R_l, see Fig.3-32.

LOW-PASS SECTION NEAR R_l

In this case:

$$g_1 = \frac{1}{k}\sqrt{\frac{k-1}{m}}$$

$$g_2 = \sqrt{m(k-1)}$$

$$g_3 = \sqrt{\frac{m}{k-1}}$$

$$g_4 = \frac{k}{\sqrt{m(k-1)}}$$

Denormalization can be done for each element using:

$g = \omega_0 L/R_h$ and

$g = \omega_0 CR_h$

where $\omega_0 = 2\pi f_0$

Then, the maximum VSWR in the pass-band becomes:

$VSWR = 1/\varepsilon^2$

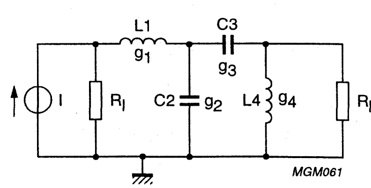

Fig.3-32 Two-section matching network using two L-sections.

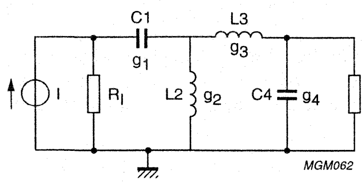

Fig.3-33 Two-section matching network using two L-sections (section sequence reversed compared with that in Fig.3-32).

LOW-PASS SECTION NEAR R_H

If the sequence of the sections is now reversed, the situation is as in Fig.3-33.

In this case, the normalized element values have to be inverted, so:

$$g_1 = k\sqrt{\frac{m}{k-1}}$$

$$g_2 = \frac{1}{\sqrt{m(k-1)}}$$

$$g_3 = \sqrt{\frac{k-1}{m}}$$

$$g_4 = \frac{1}{k}\sqrt{m(k-1)}$$

Denormalization is done as in the previous case, and the maximum VSWR remains the same ($1/\varepsilon^2$).

To match 2.5 to 50 Ω over 132 to 174 MHz, (see Section 3.2.2.3.2), the calculation gives the following results:

1st case (circuit as in Fig.3-32):

$L_1 = 5.005$ nH ; $C_2 = 167.7$ pF

$C_3 = 52.6$ pF ; $L_4 = 27.54$ nH

2nd case (circuit as in Fig.3-33):

$C_1 = 220.3$ pF ; $L_2 = 6.575$ nH

$L_3 = 20.97$ nH ; $C_4 = 40.04$ pF.

VSWR (both cases) = 1.14

The results are slightly better than those obtained with two low-pass sections. Other advantages are:

- Easier calculation
- Useful for interstage networks.

A disadvantage is the reduced suppression of harmonics.

Effect of real ('imperfect') components on the calculations

When implementing these wideband networks, keep in mind that capacitors, even surface-mount (chip) capacitors, are not ideal components. A chip capacitor, for example, has a series inductance of about 1 nH. In the example with two low-pass sections, a capacitance of 197 pF was required. If two capacitors in parallel are used, their combined inductance is 0.5 nH. As a consequence, we have to reduce the capacitance to C' where:

$$C' = \frac{C}{\omega^2 LC + 1}$$

Note, ω is the average angular frequency of the band, so in the example:

$$C' = \frac{197}{1.09} = 181 \text{ pF}$$

3.2.2.4 THE LOWER UHF RANGE

For the lower UHF range, the methods used in the upper VHF range can again be employed. However, it is not always very practical to use discrete inductances because of the very low values required, and these should then be replaced by striplines.

Note that a stripline is not a pure series inductance; it has parallel capacitance which must be taken into account in any network design. In addition, a particular inductance can be obtained with striplines of different characteristic resistance, R_c. Wherever, possible, use striplines with relatively high R_c as they generally have lower parallel capacitances.

If a transmission line is shorter than 1/8th of a wavelength, a good approximation is the LC equivalent circuit shown in Fig.3-34 where:

$L = R_c l/v$

$C = l/R_c v$

where $v = 3\text{x}10^8/\sqrt{\varepsilon_r}$. ($\varepsilon_r$ being the *effective* relative dielectric constant of the print board).

What was said about the parasitic inductance of real capacitors at VHF frequencies is of course even more relevant at UHF frequencies.

WIDEBAND UHF MATCHING CIRCUITS OVERVIEW

Lower UHF range *(Section 3.2.2.4)*

- In this range, the techniques used in the upper VHF range can again be used. The main difference is the more frequent use of striplines. In Section 3.2.2.4, the equivalence between striplines and LC-networks is given.

Upper UHF range *(Section 3.2.2.5)*

- This section outlines the considerations for very wide bandwidths (about 1 octave).
- *Section 3.2.2.5.1* covers the use of band-pass networks for the output circuit. These are based on an equivalent low-pass circuit and contain one or two Norton transformations (inductive and capacitive) including T and Pi equivalents.
- Input networks for this range are usually designed for the highest possible flat power gain, and often have a poor input VSWR at the lower end of the range. To improve performance, two identical amplifiers can be combined with 3 dB 90° hybrid couplers as outlined in *Section 3.2.2.5.2.* Constructing couplers for less-demanding applications is also described, as is the design procedure for the input matching network.

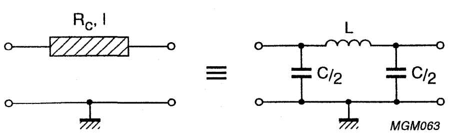

Fig.3-34 LC equivalent circuit of a transmission line shorter than 1/8th of a wavelength.

3.2.2.5 THE UPPER UHF RANGE

Here, we shall consider wideband circuits for TV bands IV and V, covering 470 to 860 MHz, i.e. a bandwidth of 390 MHz.

In Section 3.2.2.3 (Upper VHF range), we described how to match two widely different resistances over a wide range of frequencies. For two pure resistances, matching is always possible, though more sections are required as the resistance ratio and/or the relative bandwidth increases.

Now consider when one or both impedances have a large reactive component - a parallel-RC combination, or a series-RL circuit. In both cases, a time constant, τ, is involved: $\tau = RC$ or L/R.

According to Bode (see also Refs 6 and 7), there is a limit to the reflection coefficient, r, which can be achieved in the pass-band. This limit depends on the time constant and the required (absolute) bandwidth, even when the number of elements in the matching network is made arbitrarily high and is:

$$\int_0^{\infty} \ln\left|\frac{1}{r}\right| d\omega = \frac{\pi}{\tau}$$

If we assume that r is constant in the pass-band, and equal to one in the stop-bands, this relation can be simplified to:

$$2\pi B\tau = \pi / \ln\left|\frac{1}{r}\right|$$

where B is the absolute bandwidth.

This relationship is shown in Fig.3-35.

According to Bode, the area below the curve is given by the time constant. If r is less than 1 in the stop-bands, and varies in the pass-band, then the maximum value of r in the pass-band will be higher than the theoretical value.

For example, suppose the maximum acceptable VSWR in the pass-band is 1.25, then r = 0.111. For the ideal case, this gives: $2\pi B\tau = 1.43$; in practice, $2\pi B\tau$ will rarely exceed 1.0, and then only by a very small amount.

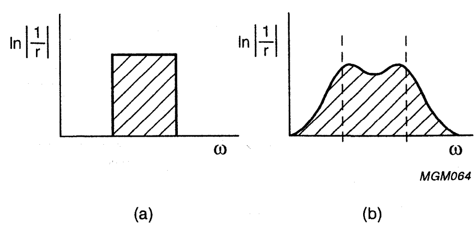

Fig.3-35 (a) Ideal and (b) practical plot of $\ln\left|\frac{1}{r}\right|$ as a function of ω (i.e. 2π times the frequency).

3.2.2.5.1 OUTPUT NETWORKS

As an example, take the BLW98, a class-A TV-transposer transistor for bands IV/V (bandwidth, B = 390 MHz). At V_{CE} = 25 V and I_C = 0.85 A, a BLW98 is able to deliver about 4 W peak sync power with a 3-tone intermodulation distortion of −60 dB. Under these conditions, the effective output capacitance, C_C, is ~20 pF, and the optimum load resistance in class-A operation is ~20 Ω. So the time constant, τ, of the transistor output is ~400 ps, and $2\pi B\tau$ then becomes 0.98, meaning that the required bandwidth can just be realized without serious concessions in output power and IMD in parts of the frequency band.

The equivalent output circuit of a transistor without internal output matching is shown in Fig.3-36.

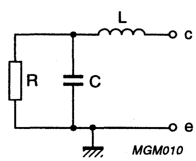

Fig.3-36 Equivalent circuit of the output of a transistor without internal output matching.

The values of R, C and L can be derived from the published curves for optimum load impedance versus frequency. Here, computer programs for circuit analysis with an optimization facility can be very helpful. A good approximation however can also be made using the following:

R: In class-A amplifiers, $R = NV_{CE}/I_C$ where N = 0.65 to 0.80. In other classes, $R = V_C^2/(2P_o)$ but note that for linear class-AB amplifiers, V_C must be chosen 10 to 15% below the supply voltage.

C: In the HF and VHF range, $C = NC_C$ where N = 1.10 to 1.15. In the UHF range (especially in the upper part), higher efficiency and gain can be obtained when the output capacitance is not completely tuned out. In practice, an amount $\Delta C = 0.5/(\omega_m R)$ may be subtracted where ω_m is the maximum angular frequency of the band.

L: This is approximately $L_c + L_e/2$ (about 1 to 2 nH in practice) where L_c and L_e are respectively the collector and emitter self-inductance.

The next step is to choose the configuration of the matching network. Where a large bandwidth is required, as in this example, it can be a big advantage to make the collector RF choke part of the matching network. This can be arranged in two ways. The simplest is where the collector RF choke tunes out the imaginary part of the output impedance in the middle of the band. A better and theoretically more correct method is to apply a Norton transformation as shown in Fig.3-37.

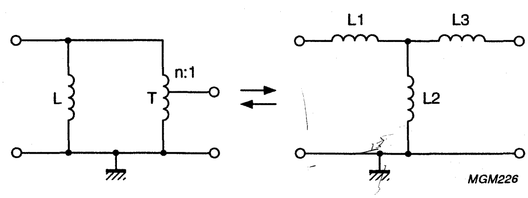

Fig.3-37 Norton transformation.

T is an ideal transformer which transforms the voltage down by a factor n (n > 1). 'Ideal' means the transformer has no parallel and no stray inductance, i.e. there is 100% coupling between the windings.

The other quantities are:

$$L_1 = L\left(1 - \frac{1}{n}\right)$$

$$L_2 = \frac{L}{n}$$

$$L_3 = \frac{-L(n-1)}{n^2}$$

Note, L_3 is negative but this is subsequently 'absorbed' in the remainder of the network. $L_1 \geq L$ in the equivalent output circuit (Fig.3-36) of the transistor.

Combining Figs 3-36 and 3-37 yields Fig.3-38. So, the transistor output impedance becomes a parallel connection of R', C' and L' where:

$$R' = \frac{R}{n^2}$$

$$C' = Cn^2$$

$$L' = \frac{L}{n^2}$$

Now we can arrange that the LC-parallel circuit resonates in the middle of the frequency band. Furthermore, we can vary R' within certain limits.

At the 50 Ω side, the same kind of transformation in reverse can be made if required. In this case, a capacitive transformation is also possible, see Fig.3-39 where:

$$C_1 = \frac{-n^2C}{n-1}$$

$$C_2 = nC$$

$$C_3 = \frac{nC}{n-1}$$

Here, C_1 is negative and so it has also to be absorbed in the remainder of the network.

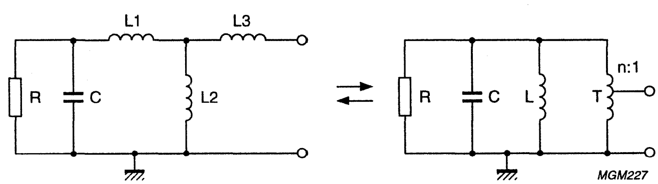

Fig.3-38 Norton transformation at transistor output.

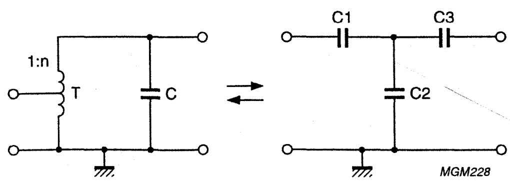

Fig.3-39 Alternative transformation at 50 Ω load side.

Sometimes a Pi-equivalent is needed instead of a T-equivalent. This can be obtained as indicated in Fig.3-40 for the capacitive case where:

$$B_{12} = \frac{B}{n}$$

$$B_{20} = B\left(1 - \frac{1}{n}\right)$$

$$B_{10} = \frac{-B\,(n-1)}{n^2}$$

This transformation also has an inductive equivalent in which $B = -1/\omega L$ instead of ωC.

Now we return to Fig.3-38 to complete the impedance matching. Several methods are possible:

- The Matthaei method as described in Section 3.2.2.3.2
- The Fleischmann method as described in Section 3.2.2.3.2
- A band-pass network as depicted in Fig.3-41.

The network of Fig.3-41 can only be used if R_1 does not differ too much from R_3, say $2R_3 \geq R_1 \geq R_3/2$. If so, we can apply the Norton transformation (just discussed) at the input and, if necessary, also at the output.

This band-pass network has been derived from an equivalent low-pass Chebyshev filter as shown in Fig.3-42.

Components with the same identifiers (in Figs 3-41 and 3-42) have the same values. Components L_1, C_2 and L_3, added in the band-pass network, resonate with the parallel or series-connected components at the geometric mean frequency of the passband, f_0:

$$f_0 = \sqrt{f_1 f_2}$$

where f_1 and f_2 are the lower and upper limits of the pass-band respectively.

L_1 resonates with C_1; C_2 resonates with L_2, and L_3 resonates with C_3

In Fig.3-42, without a Norton transformation:

$R_1 = R_3$

$C_1 = C_3$.

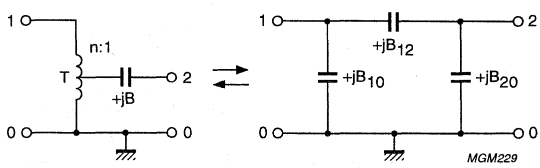

Fig.3-40 Norton transformation with Pi equivalent.

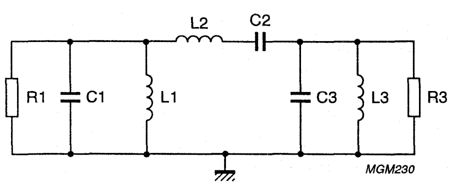

Fig.3-41 Band-pass network for output matching.

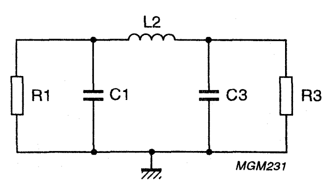

Fig.3-42 Low-pass network equivalent to Fig.3-41.

By combining some equations from the two-element compensation of Section 3.2.2.1.1, we can express L_2 as:

$$L_2 = \frac{8R_1^{\ 2}C_1}{3(\omega C_1 R_1)^2 + 4}$$

where ω is 2π times the required bandwidth. The maximum VSWR of this network can be calculated in the same way as in Section 3.2.2.1.1 where:

$$\gamma = \frac{1}{\omega R_1 C_1}$$

and

$$k = \gamma + \sqrt{\gamma^2 + 1}$$

from which

$$\mathrm{VSWR} = \left(\frac{k^3+1}{k^3-1}\right)^2$$

Since the Norton transformation does not change the product R_1C_1, this product is the same as that of the equivalent circuit of the transistor output (Fig.3-36). A circuit like that of Fig.3-41, plus transformations, has been made for the BLW32 with R = 82 Ω and C = 4.2 pF. With a bandwidth of 390 MHz this gives:

$\omega RC = 0.8439$

$\gamma = 1.185$

$k = 2.735$

VSWR = 1.216.

This is very acceptable performance. In practice. the inductances are replaced by striplines as described in Section 3.2.2.4. Re-optimization is then required and the final VSWR will be somewhat higher because of the capacitance of the striplines and the inductance of the SMD chip capacitors. See also application report *"ECO7806"*.

If the Matthaei or Fleischmann method is used instead of the one above, note that:

- For TV band IV/V, three sections (instead of two) may be necessary
- Besides several low-pass elements, sufficient high-pass elements are used. The former are the series inductances and parallel capacitances; the latter are the parallel inductances and series capacitances.

This is necessary to meet, as far as possible, the conditions for the lowest possible reflection coefficient in the pass-band according to the Bode integral. So, three low-pass sections are not as good as two low-pass plus one high-pass section.

3.2.2.5.2 INPUT NETWORKS

What is desired at the input is a network that gives good impedance matching over the entire frequency band while compensating for the variations in transistor gain with frequency. The overall gain (transistor plus network) should be roughly equal to the transistor gain at the highest frequency of the band.

For low powers, as in driver stages, this can be realized with a network containing one or two resistors. For high powers, there are better solutions, namely:

1. Make a network giving good impedance matching over the frequency band, and compensate the gain variation somewhere else in the amplifier chain or,
2. Make a network giving an (almost) exact match at the highest frequency of the pass-band and increasing mismatch at lower frequencies such that the increasing gain of the transistor is compensated in the best possible way.

The second approach is much easier to realize because the loaded Q-factors in the network may be higher than with the first approach.

Assuming a gain variation of the transistor of 6 dB per octave, the input VSWR at the lowest frequency of TV bands IV and V will be 11.3 if the second method is followed. Clearly, the preceding amplifier stage cannot function normally under these conditions. Fortunately, there is a simple solution to this problem - make two identical amplifier stages according to this principle and combine them with 3 dB, 90° hybrid couplers as shown in Fig.3-43.

The first hybrid coupler splits the drive power delivered at port 1 into two equal parts at ports 2 and 3, and introduces a 90° phase shift between the two signals. If ports 2 and 3 are loaded with 50 Ω, the output at port 4 is zero.

The most important property of a 90° hybrid coupler is that equal amounts of mismatch at ports 2 and 3 do not influence the matching at port 1; any reflected power goes to port 4. The mismatch at ports 2 and 3 must however be equal in amplitude and phase.

At the second coupler, the opposite happens. For two input signals of equal amplitude and 90° phase difference, the output is the sum of the powers while the power at port 4 is again zero. If the powers are not equal or the phase difference deviates from 90°, then the power difference appears on port 4.

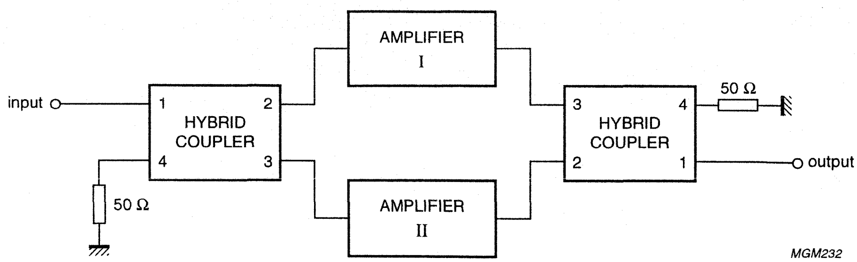

Fig.3-43 Input/output network using two identical amplifiers and 90° hybrid couplers to lower VSWR.

This sort of hybrid coupler with a full octave bandwidth and continuous power handling of 200 W is available from Anaren, USA.

Another American company, Sage, delivers the Wireline. This is a special semi-rigid coaxial cable with two inner conductors. A hybrid coupler is formed from a 1/4 λ cable for the middle of the frequency band. Note, the wavelength in this cable is about two-thirds that in free space. The Wireline is available in several thicknesses to suit different power requirements. For high powers, another product with a square cross-section is available (Wirepack).

If the bandwidth requirements are less severe, 90° hybrid couplers can be made from striplines as shown in Fig.3-44. Here, four striplines of 1/4 λ and characteristic resistances of 50 and 35.4 Ω are used. In a practical implementation, it is usual to:

- Replace the striplines by LC equivalents see Fig.3-45, or
- Make the hybrid coupler with shortened striplines, and add compensation (multilayer SMD) capacitors, see Fig.3-46.

In Fig.3-46, let tan βl = t then:

$$R'_c = R_c\sqrt{\frac{1+t^2}{t^2}}$$

$$X_c = R_c\sqrt{1+t^2}$$

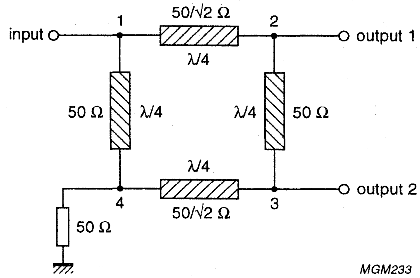

Fig.3-44 90° hybrid coupler based on striplines.

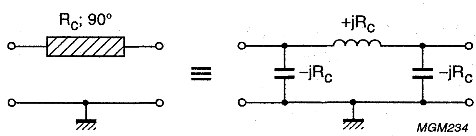

Fig.3-45 LC equivalent of a stripline.

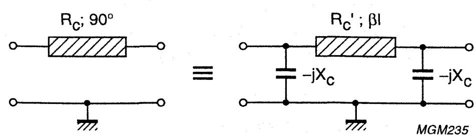

Fig.3-46 Shorter stripline equivalent using compensation capacitors.

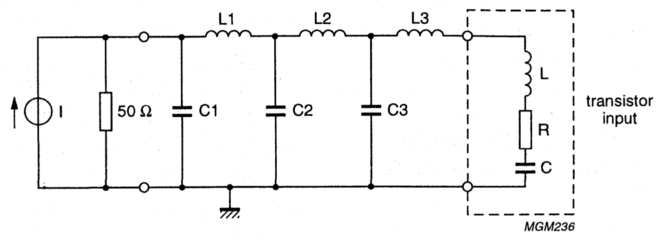

Fig.3-47 Typical input matching network.

Procedure for designing an input matching network

When calculating input matching networks, it is useful to know the RLC series-equivalent of the transistor input impedance. A first estimate can be made on the basis of the published graph of input impedance versus frequency. More accurate estimates can be obtained with the aid of a circuit analysis computer program.

To design an input matching network meeting the conditions mentioned earlier, use the following procedure, see Fig.3-47.

The last section (L_3-C_3) is designed for the highest frequency of the band. For bipolar transistors, the value of C is so high that it has no practical influence. The best value for the loaded Q-factor in this case is then about 4, and the resistance R is transformed up by a factor $Q^2 + 1$, so about 17 times.

For MOS transistors, a lower loaded Q-factor is required because of the relatively smaller value of C. A good value for Q is 2 to 3. The resistance R is then transformed up by a factor of 5 to 10, resulting in a sufficiently flat power gain.

The remaining sections, L_1-C_1 and L_2-C_2, can be calculated using the Matthaei method for the entire frequency band starting from the value found for R (Q^2 + 1) and the 50 Ω of the generator.

In the example above, the remaining part of the matching used two sections. In some cases, one is sufficient, but this depends on the value of R. The lower this is the more sections are required.

3.2.3 *Interstage networks*

Impedance matching networks between successive stages can be designed in the same way as discussed in the previous sections. For narrow-band amplifiers, this can be done directly (i.e. with no intermediate 50 Ω impedance level). However, for wideband amplifiers it is very useful to choose an intermediate impedance of 50 Ω to facilitate the alignment of the amplifier. The best way to align the output part of the network is by means of a dummy load. We shall return to this later in Section 3.5.1.

3.3 Guidelines for choosing print boards and components

3.3.1 *Print board materials*

Two main print board materials are used for constructing test circuits and practical RF power amplifiers: epoxy fibreglass and Teflon fibreglass.

3.3.1.1 EPOXY FIBREGLASS

The relative dielectric constant (ε_r) of this material can vary between 4 and 5; the average, 4.5, is suitable for most calculations. The material is available in several thicknesses, the most popular being: 1/16 inch (~1.6 mm) and 1/32 inch (~0.8 mm). The copper thickness commonly used is called 1 oz. which corresponds to a thickness of ~38 μm.

The dielectric loss factor of epoxy fibreglass is rather poor (tan δ = 0.030 to 0.035). This means a capacitor formed from part of the board itself has an unloaded Q-factor of only about 30, limiting this type of board to HF and VHF circuits. The board can however be used for interconnecting components and making low-impedance striplines.

Sometimes, even an interconnection area can cause problems. Take for instance point A in the circuits of Section 3.2.1.2. Suppose that the area of this connection is 1 cm^2 and the board thickness is 1.6 mm, then the capacitance will be about 3.35 pF. At 175 MHz and a Q_o of 30, the parallel resistance will therefore be 8150 Ω.

If the transistor operates at a supply voltage of 28 V say, and the coil in the matching network has a loaded Q of 5, the voltage at point A is 140 V maximum and the power loss in this connection area is approximately 1.2 W. This is already on the high side and, when the supply voltage and/or the loaded Q are higher, it can be considerably more. A good remedy in such a case is to remove the copper on the bottom side of the board beneath the connection area, and also to remove some heatsink material in the same region.

3.3.1.2 TEFLON FIBREGLASS

Another popular material is Rogers RT/duroid with an ε_r of 2.2. This material can be obtained in the same dielectric and copper thicknesses as epoxy fibreglass. The losses are considerably lower (tan δ = 0.001 to 0.002), making it very suitable for UHF circuits with striplines.

Tables 3-7 and 3-8 show the relationship between the characteristic resistance of stripline, R_c, and its width, w, for 1/16 inch and 1/32 inch board thicknesses. The table data have been generated by computer program based on information in Ref.8. The quantity SQRT ε_r is the line shortening factor by which the stripline length with air as a dielectric must be divided to obtain the line length on the print board. In addition, the inductance and capacitance per mm line length are given.

Table 3-7 Some characteristics of 1/16" (1.575 mm) Teflon fibreglass (Rogers RT-duroid)

W (mm)	**R_c** (Ω)	**SQRT** ε_r	**L/l** (nH/mm)	**C/l** (pF/mm)
4.746	50.00	1.367	0.22783	0.09113
1.000	113.23	1.313	0.49574	0.03866
1.500	95.47	1.325	0.42157	0.04625
2.000	83.15	1.334	0.36970	0.05348
2.500	73.90	1.342	0.33054	0.06052
3.000	66.64	1.349	0.29960	0.06745
3.500	60.77	1.355	0.27439	0.07431
4.000	55.90	1.360	0.25341	0.08110
4.500	51.79	1.365	0.23562	0.08785
5.000	48.28	1.369	0.22034	0.09454
5.500	45.23	1.373	0.20705	0.10120
6.000	42.57	1.377	0.19538	0.10782

ε_r = 2.200; H = 1.575 mm; Th = 0.0350 mm.

Table 3-8 Some characteristics of 1/32" (0.787 mm) Teflon fibreglass (Rogers RT-duroid)

W (mm)	**R_c** (Ω)	**SQRT** ε_r	**L/l** (nH/mm)	**C/l** (pF/mm)
2.352	50.00	1.364	0.22739	0.09095
1.000	82.31	1.330	0.36492	0.05386
1.500	66.12	1.346	0.29656	0.06783
2.000	55.53	1.357	0.25127	0.08148
2.500	48.00	1.367	0.21874	0.09493
3.000	42.36	1.375	0.19413	0.10820
3.500	37.95	1.382	0.17480	0.12135
4.000	34.42	1.388	0.15917	0.13439
4.500	31.51	1.393	0.14626	0.14733
5.000	29.07	1.397	0.13538	0.16021
5.500	26.99	1.401	0.12608	0.17302
6.000	25.21	1.405	0.11804	0.18578

ε_r = 2.200; H = 0.787 mm; Th = 0.0350 mm.

The main function of a stripline in a circuit is to provide a particular inductance. As a narrow, short line can have the same inductance as a wide, long one, see Tables 3-7 and 3-8, a choice has to be made based on power handling. The reactive power, i.e. the volt-ampere product, that the line is required to handle must be taken into account, i.e.:

$$P\beta l\,(s + 1/s)$$

where:

- P is the power transferred
- βl is the electrical line length in radians
- s is the voltage standing wave ratio.

Dividing this product by the unloaded Q-factor of the line, (usually 200 - 400) gives the power lost in the line.

A collector or drain RF choke can also be made in the form of a stripline. The reactance of a line RF 'short circuited' at one end is:

$$X = R_c \tan(\beta l).$$

And, the volt-ampere product of such a line is:

$$V^2\beta l/\{R_c \sin^2(\beta l)\}$$

where:

- V is the RMS value of the RF voltage at the end not 'short-circuited'
- βl is again the electrical line length in radians.

3.3.2 *Choice of components*

3.3.2.1 INDUCTORS

Depending on the value of the inductance required, inductors can be made in the form of a length of wire or a coil having one or more turns:

- straight wire

  The inductance of a straight wire is:

  $L = 0.46\, l \log(1.47\, l/d)$ nH.

  where l is the length of the wire and d the diameter, both in mm.

- single turn coil

  The inductance of a single turn of wire is:

  $L = 1.44D \log(1.08\, D/d)$ nH.

  where:

  D is the diameter (wire centre to wire centre) of the turn and d the wire diameter, both in mm.

- multi-turn coil

  The inductance of a coil with more than one turn wound in a single layer is:

  $L = n^2D^2/\{1.013\,(l + 0.45D)\}$ nH

  where:

  n is the number of turns

  D is the diameter (wire centre to wire centre) of the coil in mm

  l is the length of the winding in mm.

  The accuracy of the last formula is better than 1% provided $l > 0.45D$.

The formulae above indicate that the same inductance can be realized in different ways. An important point is the choice of the wire diameter. And, as a guideline, it is recommended to limit the current density to 2 to 3 A/mm^2. Although this guideline stems from the design of AF transformers and chokes where the windings are packed tightly together, it is relevant for inductances used at RF, as the series resistance due to skin-effect at high frequencies will be considerably greater.

Another point to consider for single layer coils is the ratio of the length of the winding to the diameter of the coil. The best ratio is 1 to 2 to get a high unloaded Q-factor. Providing some spacing between the turns will improve this Q-factor, and the recommenced spacing is equal to the wire diameter.

3.3.2.2 FIXED CAPACITORS

The most important properties of a capacitor for use in matching networks at high frequencies are:

- Maximum operating voltage
- Unloaded Q-factor
- Series inductance
- Size (in relation to dissipation)
- Temperature coefficient.

Nowadays, ceramic multilayer SMD capacitors (chip capacitors) are widely used, these having largely superseded leaded cylindrical and rectangular ceramic types. The Philips multilayer range contains Class 1, NPO types in different sizes and with maximum operating voltages up to 500 V (Ref.9). Class 1 means a relatively low ε_r and tan δ. NPO denotes a low temperature coefficient. Whilst these capacitors are suitable for many applications, a capacitor meeting more stringent specifications may be required in some applications.

The series inductance of most chip capacitors is about 1 nH. The VA-product that a chip can handle can be estimated as follows. Suppose a (small) chip can dissipate 300 mW and the unloaded Q-factor is 300, then the VA-product is the product of these two quantities:

$VI = 0.3 \times 300 = 90$ VA

If a specific application requires a higher VA-product, a parallel and/or series combination of chips can be used.

3.3.2.3 TRIMMERS

For VHF and UHF circuits, there are some excellent trimmers with Teflon isolation in Philips' product program (e.g. the 809 series, Ref.9). These have maximum operating voltages of 200 to 300 V, a maximum operating temperature of 125 °C and a guaranteed unloaded Q-factor between 400 and 670 at 100 MHz. They can be used up to about 1 GHz (their series inductance is 5 to 8 nH). At higher frequencies, products such as 'Gigahertz Trimmer Capacitors' from Tekelec (Johansson) are suitable. These have a self-resonant frequency well above the frequency of operation.

The power handling of these trimmers is much higher than that of chip capacitors. Some reserve is desirable because of the higher series inductance of trimmers. Parallel connection with chip capacitors is recommended to optimize the size of the control range.

3.4 Amplifier configurations

Most RF power amplifiers are 'single-ended', i.e. they have one power transistor. Sometimes, however, there are good reasons for using amplifiers having two or more transistors, as for example described in Section 3.2.2.5.2. In such cases, there are several ways to interconnect the transistors, the most popular employing:

- Hybrid couplers (90° phase difference)
- Parallel connection (0° phase difference), or
- Push-pull or balanced connection (180° phase difference).

3.4.1 Hybrid couplers

The use of hybrid couplers has already been described in the wider discussion of input networks in Section 3.2.2.5.2 just referred to. There, two single-ended stages were combined using 3 dB, 90° hybrid couplers to provide impedance matching *and* a flat power gain over a wide band of frequencies. The reader is referred back to that section for further details.

3.4.2 Parallel connection

3.4.2.1 VHF AND UHF RANGES

Sometimes, in base stations for mobile radio, output powers higher than those that can be delivered by a single transistor are required. The simplest solution is then to connect two transistors in parallel. However, because the transistor impedances can be very low, it is not recommended that this be done directly (i.e. by connecting gate-to-gate and drain-to-drain). A better method is shown in Fig.3-48.

Adjacent the transistors, separate matching sections are used; elsewhere, the sections are common to both transistors.

Resistors R_1 and R_2 are included to prevent push-pull oscillations, and perform the function of a hybrid coupler. Although this circuit does not fully isolate the transistors, it does prevent oscillations. For the best performance, R_1 should be twice the equivalent parallel input resistance and R_2 twice the load resistance of one transistor.

In Fig.3-48, only the RF components are shown. DC components such as RF chokes, coupling and decoupling capacitors still have to be added.

3.4.2.2 HF RANGE

Another form of parallel connection is often used in high-power amplifiers for the HF range. An extensive description of such a system is given in application report *"AN98032"*. The combining transformer (transmission line type) used is also described in report number *"ECO6907"*.

3.4.3 Push-pull (balanced) connection

To obtain more power than that obtainable from a single transistor, two transistors can be operated in push-pull mode (i.e. with 180° phase difference). To assist designers, several dual transistors already configured for push-pull are available from Philips. MOS and bipolar types for VHF and UHF operation are available.

The main advantage of push-pull is the good suppression of even-order harmonics and intermodulation products, simplifying the design of harmonic filters. It is therefore used extensively in HF SSB transmitters, as well as in FM broadcast and TV bands III, IV and V.

In the HF range, baluns (balanced to unbalanced transformers) can usually be combined with the required impedance transformation. This is done with transmission line or conventional transformers with ferrite cores as described in application reports *"ECO6907"* and *"ECO7213"*.

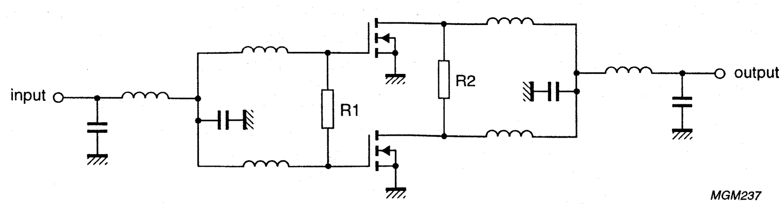

Fig.3-48 Two-transistor power amplifer with matching sections. This arrangement is also suitable for bipolar transistors.

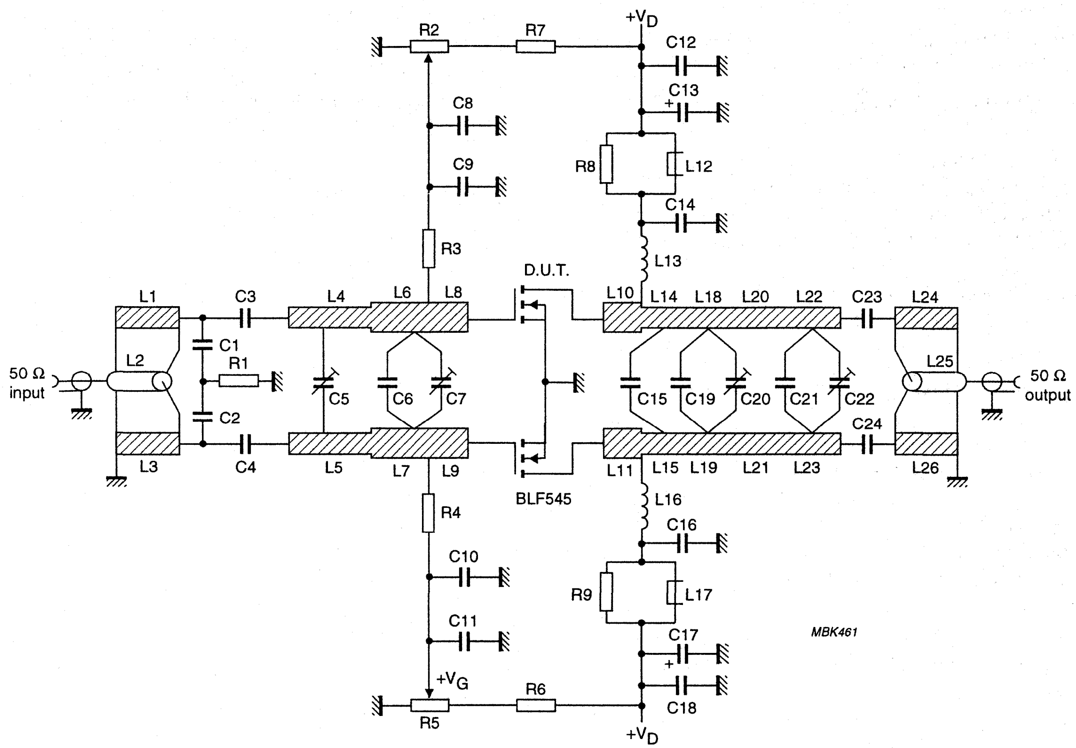

Fig.3-49 BLF545 test circuit. Full details of components are given in the BLF545 data sheet.

In the VHF and UHF ranges, another kind of balun is often used. Take, for example, the 500 MHz test circuit of the BLF545 (Fig.3-49). Although this is a narrow-band circuit, the balun used is a wideband type with a bandwidth of approximately one octave. Note that owing to the operating frequency, extensive use is made of striplines.

The baluns are both at the input (L_1, L_2 and L_3) and at the output (L_{24}, L_{25} and L_{26}). The input balun splits the signal on a 50 Ω basis (asymmetrical) into two signals in antiphase, each of half the input power. At the output, the reverse takes place.

A very convenient way of realizing this is by means of a semi-rigid coax cable with a characteristic resistance of 50 Ω. Looking at the output balun in Fig.3-49, we see that this is L_{25} and that its outer conductor is grounded at the output side while at the input side of this cable, both the inner and outer conductors are floating.

The best isolation will be obtained if the cable length (inner and outer conductors) is 1/4 λ for the centre of the frequency band (500 MHz). A disadvantage however is the impractical length of the cable.

A better solution is to use a cable length of about 1/8 λ soldered on top of a print track of the same length. The track width must of course be somewhat larger than the cable diameter so the two can be soldered together.

The signal that reaches the outer conductor of the cable via C_{24} is now shunted by a short stripline with an R_c of about 48 Ω and 1/8 λ long. The reactance of this stripline is then:

$$X_p = R_c \tan \beta l = 48 \tan 45° = 48\ \Omega$$

To restore the symmetry, we have to shunt the other signal, reaching the inner conductor of the cable via C_{23} with a stripline of the same dimensions, as shown in Fig.3-50.

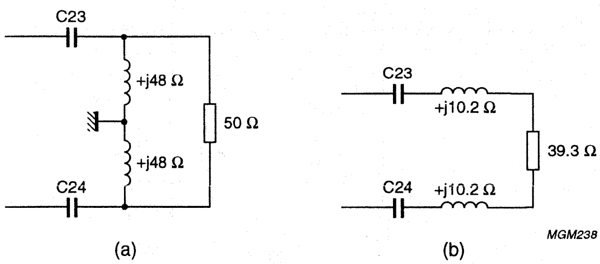

Fig.3-50 (a) Modified output baluns using 1/8 λ stripline; (b) Transformed circuit of (a) using the parallel-to-series transformation described in Section 3.2.1.1.

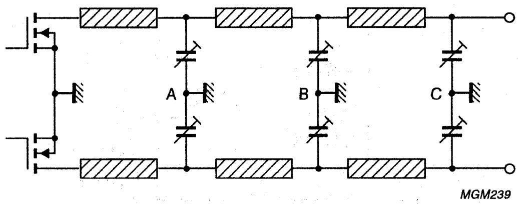

Fig.3-51 Output matching of a push-pull amplifier.

The last step is to choose the reactances of the capacitors C_{23} and C_{24} which have to be equal to the series-equivalent inductive reactances.

The result is that we have transformed the asymmetrical load resistance of 50 Ω to a symmetrical and real load resistance with a somewhat lower value. The latter is not a real problem as in many cases the transistor load impedance is lower still, so the balun forms part of the matching network.

In principle, the matching can be made for each section of the push-pull transistor separately as in Fig.3-51. However, it is not necessary to ground points A, B and C, so two capacitors in series can then be replaced by one of half the value, simplifying the circuit.

If the transistor operates in push-pull mode, it sees at its input the correct source impedance and at its output the correct load impedance. When analysing such a circuit in the parallel mode, it appears that in most cases the abovementioned conditions are not met at all. Both the input and the output circuits are practically unloaded so a parallel mode of oscillation (as opposed to the normal push-pull oscillation) can easily occur at a frequency far below the operating frequency. A good remedy is to introduce damping at the input and/or the output for this parallel mode which has no influence on the push-pull operation. An example is the combination C_1-C_2-R_1 in the BLF545 test circuit (Fig.3-49).

Another possibility is to shift the resonant frequency in the parallel mode by a large amount. This can be done for example at the input by not soldering the coax cable L_2 on L_1 but by loading it with a ferrite tube or several beads.

L_2 can also be wound on a ferrite toroid. The tracks L_1 and L_3 then become superfluous and the values of capacitors C_3 and C_4 must be increased as they now have only the function of coupling capacitors. Suitable grades of ferrite are 4B and 4C. If a toroid is used, the inductance of the outer conductor of L_2 will be increased considerably. And although this inductance has a relatively large loss factor in the VHF/UHF range, if the impedance is high enough then the gain loss is rather small. An example of this method can be found in the 108 MHz test circuit of the BLF278 (see *"Data Handbook SC19a"*).

Returning to the BLF545 circuit at 500 MHz, we see the input balun compensated differently to the output one. L_1 and L_3 are tuned by the parallel capacitors C_1 and C_2, so there will be no transformation of the source resistance.

A good example of a wideband push-pull power amplifier using the baluns described above can be found in Application note *"AN98014"*. This amplifier delivers 150 W in TV-band IV/V and uses a BLV862 transistor.

3.5 Miscellaneous

3.5.1 Alignment of RF power amplifiers

In most cases, test circuits are aligned for maximum power gain and minimum input reflection. Sometimes a situation of very high power gain and moderate efficiency arises. This indicates that the circuit is very close to instability. Often, this is because the output network has been aligned in such a way that the transistor is loaded inductively, introducing (via the feedback capacitance) a negative resistance component at the input.

Though extra damping at the input lowers the gain and improves stability, it often does not raise efficiency. In such cases, it is better to align the output network with a dummy load. This procedure is also recommended for linear amplifiers such as those in SSB transmitters and in TV transposers and transmitters where the main aim is to minimize distortion. A dummy load for a 4-lead transistor with a stud or flange envelope can be made using a small piece of printed-circuit board as shown in Fig.3-52.

Between the collector and emitter connections of a bipolar transistor (or between the drain and source connections of a MOS transistor), an SMD resistor and an SMD multilayer capacitor of the correct value are connected in parallel. Together, these components form the complex conjugate value of the optimum load impedance of the transistor. Note, the values of resistor and capacitor for the dummy load can be determined using the guidelines given in Section 3.2.2.5.1.

The dummy load is placed in the circuit instead of the transistor. At the 50 Ω output, a signal generator is connected via a directional coupler to measure the reflection coefficient.

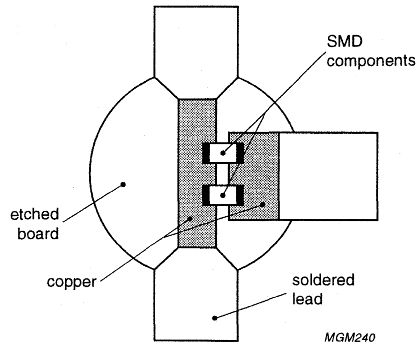

Fig.3-52 Dummy load made using printed-circuit board and SMD components. Though the dimensions are not critical, it is convenient to mimic those of a transistor to form a drop-in transistor replacement during alignment.

The output network is adjusted for zero reflection. After this procedure the network, loaded with 50 Ω, will provide the correct load impedance to the transistor and further alignment is not advised.

For push-pull transistors, the same method can be followed, but with two identical loads on one piece of printed-circuit board.

For wideband amplifiers too, this method is highly recommended. The signal generator has to be of the swept-frequency type, e.g. an R & S Polyskop or HP network analyzer.

For input networks of wideband amplifiers (see Fig.3-53) another method must be followed.

In this amplifier, capacitors C_1 and C_4 are partly variable (they are the parallel connection of a chip capacitor and a trimmer), while C_2 and C_3 are fixed (chip capacitors). The inductances L_2 and L_3 are relatively small and are therefore executed as striplines.

When aligning the output network by means of a dummy load, C_4 can first be varied to get the reflection over the whole frequency band within the required limits. If this is not sufficiently successful, C_3 can be varied in steps until the desired result is obtained. In most cases the results are then satisfactory; sometimes, L_4 must also be involved in this process.

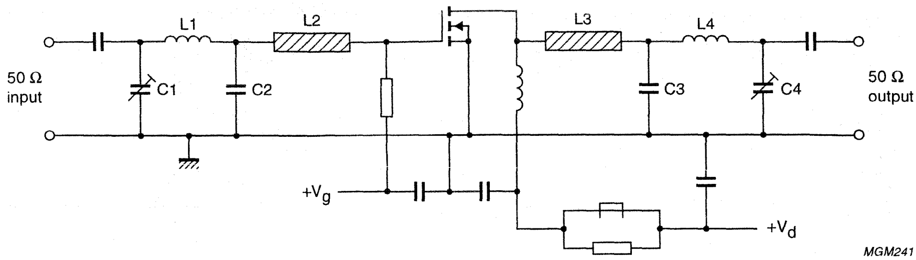

Fig.3-53 Typical wideband amplifier.

To align the input network, the transistor is put into the circuit, the 50 Ω load resistance is connected and the normal supply voltage applied. The bias voltage is adjusted in such a way that the transistor operates in class-A with a dissipation close to the desired output power, see data sheet for suitable values. Subsequently, the input network is aligned for minimum reflection over the desired frequency band. Compared with the output network this must be done in reverse order, namely C_1 first and when this is not sufficient also C_2, and in the last resort L_1.

This class-A alignment of the input network, done with small input signals, brings us very close to the final result. The last fine tuning of this network can then take place in the intended class of operation and with normal bias and RF drive powers for the required output power.

3.5.2 Suppression of parasitic oscillations

Oscillations at or near the frequency of operation can occur both with bipolar and MOS transistors especially in the lower VHF region. A suitable damping resistor between base and emitter (or between gate and source) will stop this type of oscillation.

Another type of oscillation occurs mainly with bipolar transistors although under certain circumstances with MOS devices too. This oscillation has to do with the biasing method. The collector or drain RF choke has a much higher inductance than the tuning elements and together with the total capacitance from collector or drain to earth it forms a resonant circuit at a frequency far below the operating one.

Sometimes a similar situation exists at the input side especially with bipolar transistors. If these circuits are not well damped, parasitic oscillation at relatively low frequency can start due to the always present feedback capacitance.

The best remedy is a combination of components giving strong damping at low frequencies and very little damping at the frequency of operation. Generally speaking, transistors should be loaded at both their input and output with a low, mainly resistive impedance. This can be provided at the input side with the circuit of Fig.3-54(a) and at the output side with the circuit of Fig.3-54(b) or (c).

In all these circuits, L_1 is a relatively small inductance with a high Q-factor and a reactance at the operating frequency of 3 to 7 times the equivalent parallel resistance at that point. L_2 is a much higher inductance with a low Q-factor, e.g. a choke with a ferrite core (3B being a good material). The inductance can be 6 to 8 μH.

R is a small resistor, say 10 Ω. C1 is a decoupling capacitor for the operating frequency, i.e. a low value ceramic type with high Q-factor. C_2 is a much higher capacitance, e.g. 100 nF which can have a low Q-factor.

Sometimes the supply voltage is decoupled with an extra capacitor which can be a low value electrolytic type (not drawn).

Another form of parasitic oscillation is parametric oscillation caused by the non-linear-properties of the collector capacitance. If this capacitor is fully driven by the RF voltage, it can develop a negative resistance at one half and even one third of the RF frequency, leading to instability when the collector or drain RF choke has a very low value.

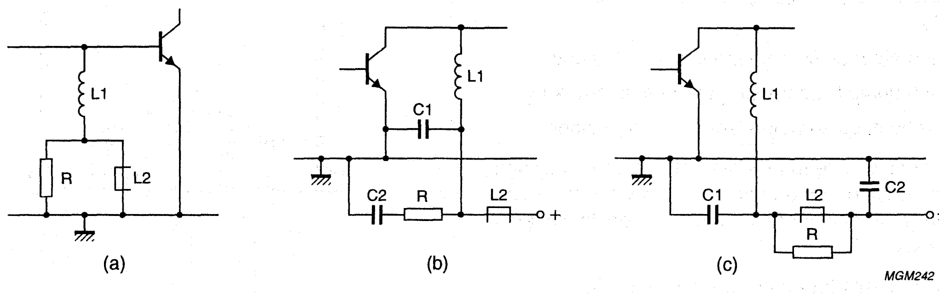

Fig.3-54 Circuit parts to suppress parasitic oscillations (a) at the input; (b) and (c) at the output.

Also possible is a parametric oscillation known as conversion oscillation. This can happen when the collector or drain circuit contains two resonant circuits where the sum of the resonant frequencies equals the frequency of operation. The lower one is then formed by the RF choke and the total effective parallel capacitance while the other is the slightly detuned output matching circuit.
This detuning can arise during tuning or by a small antenna mismatch.

Mathematically it can be shown that the power of this oscillation is divided into the ratio of the resonant frequencies of the tuned circuits. Fortunately, the measures necessary to stop this oscillation are the same as those previously mentioned.

4 RF AND MICROWAVE TRANSISTOR PACKAGES

The packages of electronic devices are, in general, designed to:

- Protect the electronics from mechanical damage
- Ensure adequate heat transfer to the ambient, and
- Provide robust, solderable electrical terminations.

For RF and microwave transistors however, the package itself forms an important part of the total electronic circuit, and this places additional requirements upon its electrical characteristics.

These requirements together with the available technologies have influenced RF transistor package design over the years. As a result, there are a variety of packages on the market today. The design and characteristics of the main package types are outlined in the following sections. Information on specific packages is given in data handbooks SC18: Discrete Semiconductor Packages, and SC19a: RF & Microwave Power Transistors, RF Power Modules and Circulators/Isolators.

4.1 Basics of RF and microwave transistor packages

In general, two (the base/gate and emitter/source) of the three electrical contacts of a transistor die are on the top of the die, and are connected to the external package terminations by bonding wires. The underside of the die is the third contact (the collector/drain) and connection is usually made to this contact by bonding the die to an electrical conductor which also serves as a heatsink.

4.2 Metal-can packages

Included here for historical completeness, metal-can packages used to house bipolar transistors are rapidly being replaced by newer, superior alternatives.

In a metal-can package (e.g. TO-39 (SOT5)), the transistor die is attached to a small, thin metal plate (usually round). All the external electrical terminations are wire leads. The collector lead is connected to the plate; the emitter and base leads are fed through the plate and isolated from it by a glass seal.

The package is sealed with a metal cap welded onto the plate. This design combined with stringent well-controlled manufacture provide a hermetic package.

The power that a metal-can package can handle however is very limited, because heat is mainly removed from the die by radiation. And, while mounting the package directly onto a heatsink in a circuit lowers the packages thermal

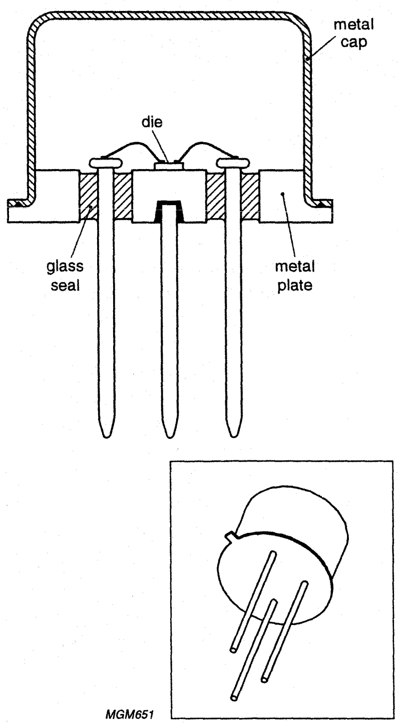

Fig.4-1 Metal-can package construction.

resistance, it means the collector is connected to the heatsink, whereas most applications require a common-emitter or common-base configuration. The solution to this drawback was found with the introduction of ceramic packages.

4.3 Ceramic packages with a copper stud or flange

In a ceramic package, the transistor die is soldered on a metallized ceramic heat-spreader located on top of a stud or flange used to mount the transistor and to conduct heat away from the die. The function of the somewhat inappropriately named heat-spreader is to electrically isolate the bottom of the die from the stud or flange, allowing the transistor package to be mounted directly to a heatsink.

The electrical terminations are formed by brazing several, usually flat, leads to the heat-spreader, with wire bonding from the leads to the two contacts on top of the die. Beryllia (BeO) used to be the most-commonly used heat-spreader material since it combines good thermal conductivity (250 W/mK) with good electrical isolation. A disadvantage of BeO is that it is toxic. So, in line with Philips' policy to eliminate toxic and environmentally harmful substances from its products, packages with aluminiumnitride (AlN) heat-spreaders have been developed - the slightly lower thermal conductivity of AlN being compensated for by using thinner ceramic.

The first ceramic packages incorporated a copper stud or flange brazed to the bottom of the heat-spreader. Since there is considerable mismatch between the thermal coefficients of expansion (TCE) of copper and beryllia, the contact area must be limited to prevent the heat-spreader from cracking. Larger (higher power) packages (e.g. SOT121 and SOT171) were therefore designed using a copper pedestal to which the heat-spreader was attached (brazed) with the die on top. The pedestal allows a larger heat-spreader (and hence die) to be used whilst maintaining the metal-to-ceramic contact area well below the practical limit. Even with this design, however, the size of the heat-spreader is limited as only the region directly above the pedestal has a low thermal resistance, and thus conducts heat effectively. Those areas of a transistor die and heat-spreader extending beyond the top of the pedestal have a higher thermal resistance. Nevertheless, since such packages can be mounted directly onto a heatsink in the application, the power handling, though still restricted, is much better than that of the standard design.

This type of package (with or without pedestal) is sealed by epoxy-glueing a ceramic cap to the top of the package. Though forming a high-quality reliable seal, epoxy resin does not provide a hermetic barrier. To ensure that the package is completely sealed and that there are no pinholes in the epoxy, the packages are tested for gross leaks. Note that all epoxy glues start to degrade at temperatures close to 300 °C and, for long-term stability, standard ceramic packages should not be exposed to temperatures above about 150 °C. Short exposure to higher temperatures is allowed (e.g. during reflow soldering). In addition, during fluxing and cleaning, minimize exposure to liquids, for example by dipping.

Though not strictly hermetic, all of Philips' standard ceramic packages contain glass-passivated transistor dies. Effectively isolating the die from its surroundings, glass passivation contributes to extremely high levels of transistor reliability.

4.4 Ceramic packages with special flange materials

As indicated above, the size of ceramic packages with copper flanges is limited by the different TCEs of copper and ceramic. This limitation was overcome by replacing the copper by a material with a much lower TCE. Nowadays, two materials are commonly used which combine a much lower TCE with a still acceptable thermal conductance:

- A tungsten-copper alloy (e.g. SOT262), and
- A copper-molybdenum-copper sandwich (e.g. SOT468).

These materials allow the contact area between flange and ceramic to be much larger while the ceramic can be even thinner without increased risk of cracking. Since these materials are at present very expensive, packages with a copper flange remain in widespread use. For improved RF grounding at high frequencies, flanged packages with through-plated holes in the ceramic have been developed.

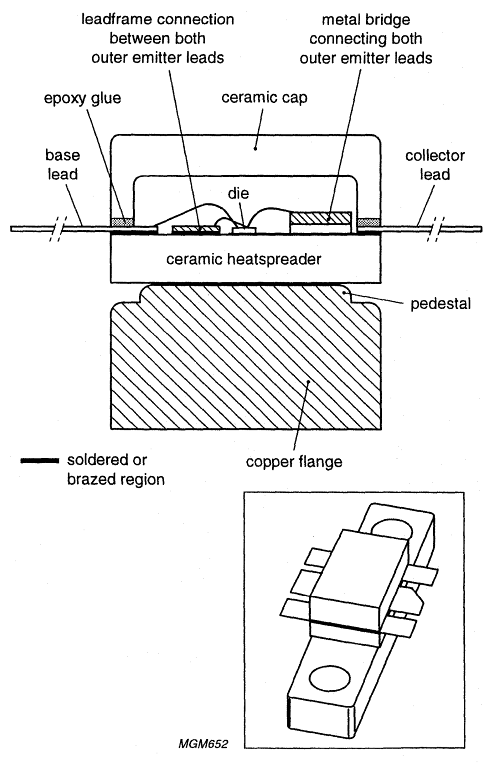

Fig.4-2 Construction of a typical ceramic package with flange.

4.5 Hermetic ceramic packages

A hermetic transistor package provides the highest levels of reliability in extremely harsh environments as required in aerospace and military applications for example.

Ceramic packages can be made hermetic, however a special design is required. The leads are no longer brazed directly onto the heat-spreader as in a standard ceramic package but are brazed onto a two-layer alumina frame (i.e. consisting of two frames sintered together). The bottom frame is larger than the top one, thus forming inner and outer ledges (electrically connected by metallization on the bottom frame) The external leads are brazed to the outer ledge, while the inner ledge is used to make a connection to the transistor die by wire-bonding. The top side of the second frame is flat and completely metallized to enable a metal or ceramic cap to be soldered to it.

4.6 LDMOST packages

Whereas the abovementioned packages are suitable for bipolar and VDMOS transistors, packages for the LDMOS transistors are somewhat different. This is because the bottom of an LDMOST die is the source, not the drain (collector) as in a standard MOS (bipolar) transistor. This is a major advantage as it is no longer necessary to electrically isolate the die from the heatsink in the application - the die is mounted directly on the flange. The flange material therefore must have a good thermal conductivity and a TCE close to that of silicon. Two materials in current use are a tungsten-copper alloy flange, and the copper-molybdenum-copper sandwich mentioned earlier. In order to electrically isolate the drain and gate leads from the flange, an alumina frame is brazed onto the flange, with the leads brazed on top of this frame. The package is completed by a ceramic cap sealed with epoxy.

Offering superb electrical and thermal performance, and ease of heatsinking, Philips' LDMOS packages are an attractive solution in an increasing number of applications.

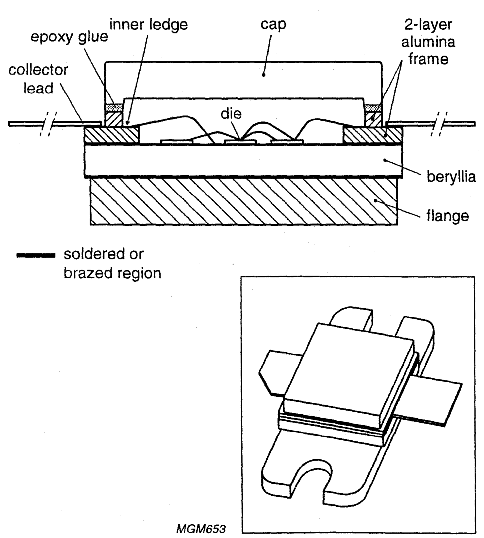

Fig.4-3 Typical hermetic package construction (Package: SOT422A).

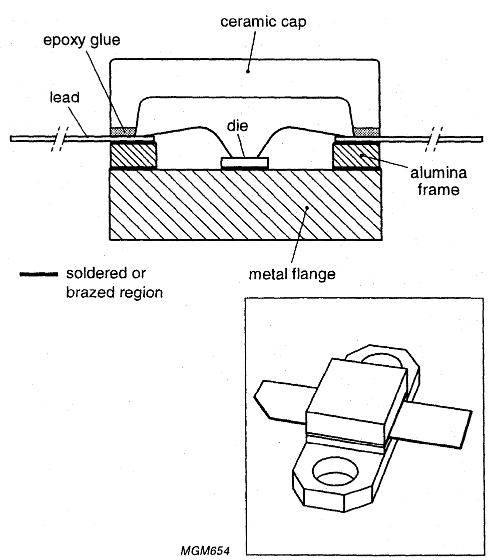

Fig.4-4 Typical LDMOST package construction (Package: SOT467).

4.7 Flangeless and SMD packages

In order to reduce the board space required by transistors, packages without a flange have been introduced (e.g. SOT333). Eliminating the flange however also eliminates the mounting holes, so other mounting methods have to be used. These include clamping or even reflow soldering. Eliminating the flange is in general only possible with packages for bipolar devices in which the dies are mounted on a ceramic heat-spreader. However, for Philips' SOT391B package, eliminating the flange alone was not an option as this package has through-plated holes in the heat-spreader. Without a flange, the package could not be sealed adequately. The solution is to braze a thin copper plate to the back of the package. This has two advantages. First, the holes are sealed, and second, the lead height of the package can be optimized to suit standard printed board materials.

With LDMOST packages, the entire flange cannot be eliminated as the dies are mounted on top of the flange. The board space required can be reduced however by reducing the length of the flange, most effectively by shortening it to the size of the alumina frame. Packages with such modified flanges are often referred to as 'earless'. Clamping or reflow soldering are again the recommended mounting methods.

Besides flangeless and earless packages, Philips has introduced a leaded surface-mount package (SOT409). This package, which is based upon the plastic SO8 package, has a copper backpad, a ceramic (alumina or AlN) heat-spreader, a copper leadframe extending beyond the heat-spreader and a ceramic cap. The backpad enables the package to be soldered onto a PCB. To ensure reliable solder joints and low thermal resistance, the specification stipulates that the leads are J-shaped such that backpads and leads are coplanar to within 0.1 mm, and that the leads never extend beyond the backpad plane.

An even more effective way of reducing the required board area is to use leadless packages. Besides saving board space, these are highly cost-effective as they can be mounted in a standard automated SMD reflow soldering process. This kind of package consists of a ceramic (AlN) heat-spreader and a ceramic cap. Leads are replaced by plated contacts on the package sides. To increase the soldering area for the electrical connections (and to obtain more reliable solder joints), the plating is extended onto the back of the package.

Reflow soldering footprints are available for all SMD packages for optimum soldering results. For optimum heat flow between package and heatsink (through a printed circuit board), it is recommended to incorporate vias in the board. The optimum size and location of these vias for each package are available.

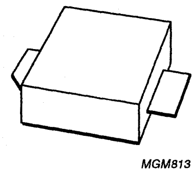

Fig.4-5 SOT391B - a typical flangeless ceramic package.

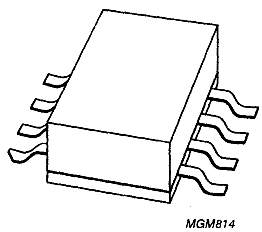

Fig.4-6 SOT409B - a ceramic surface-mount transistor package derived from the SO8 package.

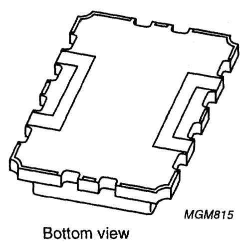

Fig.4-7 SOT511 - a typical leadless ceramic surface-mount package.

4.8 Coefficients of linear thermal expansion of packages

The data of Tables 4-1 and 4-2 (together with manufacturers' board and heatsink data) can be used to obtain good thermal matching in practical amplifiers.

Table 4-1 Overview of materials used in packages

PACKAGE	FLANGE			LEADFRAME				BACKPAD	CERAMIC INSULATOR	
	COPPER	TUNGSTEN -COPPER	Cu-Mo-Cu	ALLOY 42 (Fe58/Ni42)	NICKEL	KOVAR (Fe54/Ni29)	COPPER	COPPER	BeO	AIN
SOT119	√	–	–	√	–	–	–	–	√	–
SOT121	√	–	–	√	–	–	–	–	√	–
SOT123	√	–	–	√	–	–	–	–	√	–
SOT161	√	–	–	√	–	–	–	–	√	–
SOT171	√	–	–	√	–	–	–	–	√	–
SOT262	–	√	–	√	–	–	–	–	√	–
SOT268	–	√	–	√	–	–	–	–	√	–
SOT273	√	–	–	√	–	–	–	–	√	–
SOT279	√	–	–	√	–	–	–	–	√	–
SOT289	–	√	–		–	√	–	–	√	–
SOT324	–	√	–	√	–	–	–	–	√	–
SOT333	√	–	–	√	–	–	–	–	√	–
SOT390	–	√	–	√	–	–	–	–	√	–
SOT391	–	√	–	√	–	–	–	–	√	–
SOT391B	–	–	–	√	–	–	–	√	√	–
SOT409	–	–	–	–	–	–	√	√	–	√
SOT422	√	–	–	–	√	–	–	–	√	–
SOT423	√	–	–	–	√	–	–	–	√	–
SOT437	–	√	–	√		–	–	–	√	–
SOT439	√	–	–	–	√	–	–	–	√	–
SOT440	√	–	–	–	–	√	–	–	√	–
SOT443	–	√	–	–	–	√	–	–	√	–
SOT445	√	–	–	–	–	√	–	–	√	–
SOT448	–	√	–	–	√	–	–	–	√	–
SOT460	–	√	–	√	–	–	–	–	√	–
SOT467	–	√	–	√	–	–	–	–	–	–
SOT468	–	–	√	√	–	–	–	–	–	√
SOT502	–	√	–	√	–	–	–	–	–	–
SOT511	–	–	–	–	–	–	–	–	–	√

Source: Suppliers' data sheets

Table 4-2 Coefficients of linear thermal expansion, α, (in ppm/K) of package materials between 25 and 150 °C;

COPPER	TUNGSTEN COPPER	Cu-Mo-Cu	ALLOY 42 (Fe58/Ni42)	NICKEL	KOVAR (Fe54/Ni29/Co17)	BERYLLIA	ALUMINIUM NITRIDE
17.9	6.6	9.5-6.0	4.5	11.6	4.4	6.7	4.0

Source: Suppliers' data sheets

4.9 Mounting recommendations

When mounting transistors, observing the following recommendations will ensure good thermal and good electrical contact between transistor package and heatsink - a requisite for trouble-free, reliable operation.

4.9.1 Heatsink preparation

- For transistors dissipating up to 80 W, heatsink thickness should be:
  - At least 3 mm for copper heatsinks (>99.9% ETP-Cu)
  - At least 5 mm for aluminium heatsinks (99% Al)

  These thicknesses should be increased proportionally for transistors dissipating more power.
- Minimum depth of tapped holes in heatsinks: 6 mm
- Ensure holes in heatsinks are free of burrs
- Ensure that the mounting area is at a level such that there is a small positive clearance between the transistor leads and the printed circuit board. This prevents any upward bending of the leads which can damage the ceramic heat-spreader and/or the encapsulation.
- Flatness of the mounting area: better than 0.02 mm
- Mounting area roughness: <0.5 μm
- Mounting area should be free of oxidation.

4.9.2 Printed circuit board preparation

- Tin and wash the printed circuit board.

4.9.3 Transistor preparation

- Transistor leads are gold plated. To avoid brittle solder joints (due to too much gold in the joint), pre-tin the leads, for example, by dipping their full length into a solder bath at a temperature of about 230 °C. Minimize the use of flux.
- Apply a thin, evenly-distributed layer of heatsink compound to the flange
- Recommended heatsink compounds are:
  - 'WPS II' (silicone free) Austerlitz-Electronics
  - '340' from Dow Corning.
- When using a thermal pad, take special care with respect to the size as well as the positioning of the pad. If the pad does not cover the entire flange, the package can be stressed so much that the ceramic heat-spreader cracks. Ensure that mounting screws do not contact the thermal pad (prevents the pad wrinkling if the screws are turned).

4.9.4 Mounting sequence

- Position the device with the washers in place
- Use 4-40 UNC-2A cheese-head screws with a flat washer to spread the joint pressure
- Tighten the screws until finger tight (0.05 Nm)
- Further tighten the screws until the specified torque is reached (do not lubricate); for torques, refer to the package outlines section of each data handbook
- To lock mounting screws, allow about 30 minutes for them to bed-down after the specified torque has been applied, re-tighten to the specified torque and apply locking paint
- Solder the transistor leads onto the printed circuit board.

5 SYMBOLS

Table 5-1

α	Coefficient of linear thermal expansion
βl	Electrical line length (stripline)
γ	Mathematical variable
ε_r	Dielectric constant (relative)
ε	Mathematical variable
η_c	Collector efficiency
λ	Failure rate; wavelength
ω	Angular frequency; maximum angular frequency; minimum angular frequency
ω_T	Transition frequency ($2\pi f_T$)
A	Attenuation; difference in IMD between driver and final stage
B	Susceptance; absolute bandwidth; increase in IMD in amplifier output
C	Capacitance
C_c	Total collector or output capacitance
C_{re}	Feedback capacitance, i.e. C_{cb}
C_{is}	Input capacitance when the output is short-circuited
C_{os}	Output capacitance when the input is short-circuited
C_{rs}	Feedback capacitance; this is the same as C_{gd}
C_p	Parallel capacitance
C_s	Series capacitance
d	Intermodulation distortion; mathematical variable
$E_{(SBR)}$	(Reverse) second breakdown energy
f	Frequency
f_T	Transition frequency
G	(Power) gain
g	(Normalized) filter element identifier (resistance, capacitance or inductance)
g_{fs}	Forward transconductance
h_{FE}	DC current gain
h_{fe}	RF current gain
I_C	Collector DC current (i_c denotes varying value)
I_{CM}	Maximum instantaneous value of the collector current
I_D	Drain current
I_{DSX}	Maximum drain current that a device can deliver
k	Constant; mathematical variable: $k = \gamma + \sqrt{(\gamma^2 + 1)}$
L	Inductance
L_p	Parallel inductance
L_s	Series inductance
l_{ch}	Channel length
ppm	Parts per million
P_L	Load power
P_S	Forward power delivered by source
P_{tot}	Maximum RF dissipation at a mounting base temperature of 25 °C
R	Resistance
$R_{DS(on)}$	Total resistance in the drain-source circuit at a high, positive V_{GS}
R_h	Higher resistance
R_l	Lower resistance
R_L	Load resistance
R_p	Parallel resistance
R_s	Series resistance
r	Reflection coefficient
s	Voltage standing wave ratio
SOAR	Safe Operating ARea
T_{stg}	Maximum ($T_{stg\,max}$) and minimum ($T_{stg\,min}$) temperatures at which a device may be stored when not in operation
T_j	Maximum junction temperature in operation
$V_{(BR)CBO}$	Collector-base breakdown voltage with open emitter
$V_{(BR)CEO}$	Collector-emitter breakdown voltage with open base
V_{CBO}	Maximum collector-base voltage with open emitter
V_{CEO}	Maximum collector-emitter voltage with open base
v_{ce}	Collector-emitter voltage (instantaneous value)
V_{CES}	Maximum collector-emitter voltage with a short circuit between base and emitter
$V_{CE\,sat}$	Collector-emitter saturation voltage
V_{CER}	Maximum collector-emitter voltage with a small resistor e.g. 10 Ω, between base and emitter
V_{DS}	Drain-source voltage
V_{EBO}	Maximum emitter-base voltage with open collector
V_{GS}	Gate-source voltage
$V_{GS(th)}$	Gate voltage at which drain current starts to flow
VSWR	Voltage standing wave ratio
X	Reactance
X_p	Parallel reactance
X_s	Series reactance

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PART 2

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GENERAL

APPLICATION NOTES

Considerations on efficiency of the RF power transistors in the different classes of operation

Technical Publication
COE82101

1 SUMMARY

In this report considerations are given concerning the obtainable collector efficiencies in the different classes of operation of R.F. powertransistors. Also the frequency limitations are being considered.

As an exemple it can be mentiond that our 28 V transistors are able to operate in class-E with an efficiency of 85% up to frequencies of 60 to 70 MHz.

2 INTRODUCTION

Some times we receive questions on the possibilities to improve the efficiency of R.F. power amplifiers. Below some considerations will be given for the different classes of operation of nonlinear amplifiers.

3 CLASS-B OPERATION ($V_{BE} = 0$)

For most of our transmitting transistors we publish the collector efficiency as measured in a class-B common-emitter narrow-band test circuit. Typically this efficiency is 65 to 70%. This can be explained as follows:

- The current efficiency of a class-B amplifier is: $\pi/4 \times 100 = 78.5\%$
- The loss of the output matching network is appr. 5% because it is designed for a loaded Q-factor of 10 whilst the unloaded Q-factor is appr. 200
- The remaining losses are D.C. and R.F. losses in the built-in emitter and collector resistances of the transistor. The former is necessary for a good D.C. SOAR and the latter for a high reverse second breakdown energy giving the device sufficient ruggedness against load mismatch.

However from this situation there are deviations in both directions; e.g. the BLW89 has an efficiency of only 53%. This is caused by the tuning method of the narrow-band test circuit, because the circuit is tuned for maximum power gain. The corresponding load impedance of the transistor is sometimes strongly reactive. Phase angles of 40 to 45 ° can occur which means that the collector efficiency must be multiplied with the cosine of this angle. If a different aligning method was applied, e.g. with a more resistive dummy load, the same transistor would show a higher efficiency at the cost of some power gain.

The other extreme is formed by transistors like the BLW60 and BLY90 having efficiencies of appr. 80%. This happens only at relatively high operating frequencies where the power gain is only 4 to 5 dB. In such cases a substantial amount of the drive power is fed directly to the output circuit via the collectorbase capacitance and the emitter lead inductance. This causes an artificially high collector efficiency. It is therefore better to compare transistors on the basis of oscillator efficiency being defined as:

$$\eta o = \frac{Po - Pi}{V_{ce} \times I_c}$$

In addition to the considerations above there is a slow decrease of efficiency when the operating frequency comes in the neighbourhood of 50% of the f_T of the transistor. This is caused by the increased capacitive current through the transistors collector and emitter resistances.

4 CLASS-C OPERATION

The collector current efficiency can be improved by reduction of the angle of current flow. This is achieved by a negative base-emitter D.C.voltage, e.g. caused by an external base resistor which is effective for D.C.

We do not recommend this method because a bias voltage in excess of 300 mV in combination with the increased drive voltage may cause continues breakdown of the base-emitter diode leading to degradation of this diode, i.e. higher leakage current and reduced h_{fe}.

On the other hand bias voltages below 300 mV are not very effective.

5 CLASS-D OPERATION

An excellent description of this type of operation is given in Ref.1. From this article some conclusions can be drawn:

- Push-pull operation is required with a very tight coupling between the two transistors. This can for instance be achieved by a complementary pair of transistors (NPN - PNP). However pairs showing sufficient equality of D.C. and R.F. properties are not available. As an alternative a matched pair of NPN-transistors can be used provided that a good combining transformer can be constructed which is only possible at frequencies up to appr. 30 MHz.
- The maximum frequency of operation is further restricted by the switching times of the transistors. For output powers above 10 W this is about 0.01 f_T. This means for our modern transistors with U.H.F. diffusions a maximum of 5 to 10 MHz.

6 CLASS-E OPERATION

6.1 General considerations

Design information on this class of operation can be found in Ref.2 through 5. The most important paper in this respect is Ref.4, section III B, pp. 731 to 732, equations 3.20 through 3.29. The basic circuit diagram is reproduced in Fig.1a en b. The reactance of RFC must be high compared with the load resistance. The series tuned circuit in Fig.1b. must have a sufficiently high loaded Q, e.g. greater than 5. After some re-arrangement of the above mentioned equations we find that:

$$R_L = \frac{2V_s^2}{P_o \times \left(1 + \frac{\pi^2}{4}\right)} = 0.5768 \times \frac{V_s^2}{P_o}$$

$$B = \omega_o C = \frac{2}{\pi \times \left(1 + \frac{\pi^2}{4}\right) R_L} = \frac{P_o}{\pi V_s^2}$$

$$X = \omega_o L = \frac{\pi}{8} \times \left(\frac{\pi^2}{2} - 2\right) R_L = \frac{\pi\left(\frac{\pi^2}{2} - 2\right) V_s^2}{4\left(1 + \frac{\pi^2}{4}\right) P_o} = 0.6648 \frac{V_s^2}{P_o}$$

An ideal transistor (having zero saturation resistance) will then show a collector efficiency of 100%.

Further we know from Ref.4 that the collector peak voltage is 3.562 times the supply voltage and that the collector peak current is 2.862 times the collector D.C. current.

6.2 Practical example

To show the possibilities of class-E operation we choose the BLV 25 which is able to produce 175 W of output power at a supply voltage of 28 V up to a frequency of 108 MHz. In a ‘normal’ class-B amplifier this transistor shows an efficiency of 70 to 75%.

The guaranteed collector breakdown voltage of the BLV 25 is 65 V and the typical value 70 V. To prevent loss of efficiency by clipping of the collector voltage waveform we choose a supply voltage of 20 V.

The allowable collector peak current is 35 A. If we choose 30 A the drop of f_T is less than 20% compared with the point of maximum f_T.

Then the collector D.C. current becomes:
$I_c = 30/2.862 = 10.5$ A
and the D.C. input power:
$P_{dc} = 20 \times 10.5 = 210$ W.

The saturation resistance is appr. 0.1 Ω and if we consider the collector current as a half sine wave the saturation loss can be approximated by:

$$P_{sat} = \frac{I_{cp}^2 \times R_{sat}}{4} = \frac{30^2 \times 0.1}{4} = 22.5\ \text{W}$$

So the transistor output power becomes:

$P_O = P_{dc} - P_{sat} = 210 - 22.5 = 187.5$ W

As mentioned earlier the loss of the output matching network is 5%, so the output power of the amplifier will then be:

$P_o' = 0.95 \times P_o = 0.95 \times 187.5 = 178$ W

This gives us a collector efficiency of:

$$\eta_c = \frac{P_o'}{P_{dc}} = \frac{178}{210} \times 100\% = 85\%$$

A question that still has to be answered is: up to what frequency can this performance be maintained? The answer can be found by inspection of the formula for B in the previous section. We must keep in mind that C in this formula is the total capacitance from collector to ground, i.e. the sum of the transistors effective collector capacitance and a possible external capacitor. If we reduce the latter to zero and rearrange the formula we will find the maximum frequency of operation:

$$f_{max} = \frac{P_o}{2\pi^2 C_c V_s^2}$$

C_c is the effective collector capacitance which is 344 pF at a collector voltage of 20 V, so:
$f_{max} = 66$ MHz.

Unfortunately this is not sufficient to cover the F.M. broadcast band up to 108 MHz. However at least some of the advantage of class-E operation can be obtained by using the RFC to tune out the surplus of collector capacitance. In this way a collector efficiency of 80% is probably possible.

7 FINAL CONSIDERATIONS

An interesting question is whether the BLV25 is a good or a bad transistor for class-E operation. Examination of many Philips and competition 28 V transistors shows that it is a good average. f_{max} depends on the ratio P_o/Cc which does not spread so much.

A much greater improvement is obtained by the application of 12 V transistors. The quantity f_{max} rises then to the double value. However for a supply voltage of 12 V there are no transistors available with the output power of the BLV25.

If we would try to make such a device it would be a very impractical one, e.g. the optimum load resistance would be less than 0.5 Ω and the power gain 3 dB less than that of the BLV25, i.e. 7 to 8 dB.

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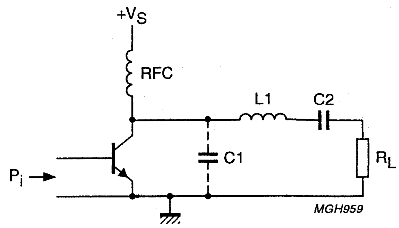
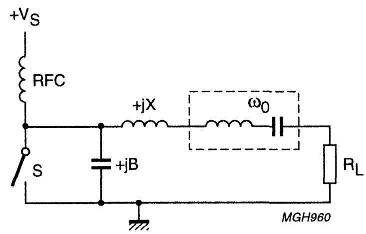


a.



b.

Fig.1

1 INTRODUCTION

Transmission line power transformers can be used to perform a variety of functions, among which are phase reversal, balanced to unbalanced coupling, impedance transformation and hybrid functions. Such transformers find many applications in wide-band power amplifiers for both s.s.b. transmitters in the h.f. region and f.m. transmitters in the lower v.h.f. region.

The properties of a practical h.f. power transformer are discussed here and their effect on transformer performance is analysed. Since losses must be kept low, in practice the transformer will use a ferrite core. Further, we have limited the discussion to cores without an air-gap since these have a low stray magnetic field, a high permeability, and can cover the power range (up to 80 W) dealt with here. Data (dimensions, permeability values etc.) on all core types can be found in our Data Handbook *"Soft Ferrites"*, MA01. A glance through the Handbook will show the wide range of materials, dimensions and types from which the designer may choose. It must be remembered, of course, that when cores constructed in two parts (pot-cores and cross-cores, for example) are used, the type without an air-gap must be selected.

Throughout we have aimed at giving practical solutions to the problems posed by material and design limitations. In particular, compensating techniques for extending the frequency range of a number of transformer configurations are discussed. To give an idea of some application possibilities, practical examples in several transformer configurations have been worked, using transformer cores from our range of ferrites.

2 TRANSFORMER SPECIFICATION

The transformer design considerations dealt with in this publication are:

- Maximum power level to be handled
- Frequency range
- Input and output impedance
- Allowable reflection and resistive losses.

How a transformer can meet the above considerations for a particular application is analysed in the following three sections. The first two sections deal with the influence of the core and transmission line respectively on transformer performance, and the third with mismatch compensation techniques.

3 INFLUENCE OF THE CORE ON PERFORMANCE

3.1 Primary Inductance

This inductance determines the amount of reflection at the low frequency end of the band. It can be calculated using the formula:

$L = \mu_o \mu_r n^2 A/l$

in which:

L = inductance in H

$\mu_o = 4\,\pi\,10^{-7}$ (rationalised M.K.S. units)

μ_r = relative permeability

A = average ferrite cross section in m^2

l = average length of the lines of force in m

n = number of turns between the input connections.

In a simple example, like the phase reversing transformer, this relation holds. Other cases may require a transformation (see Section 7.1).

If degrading of performance at the high end of the band is to be avoided, the value of L must not be higher than really necessary. A good practical value is:

$L = 4R/\omega_{min}$

in which:

R = midband input resistance in Ω

$\omega_{min} = 2\pi$ times the minimum frequency in Hz.

Where requirements are severe the compensation technique described in Section 5.1 may be used.

3.2 Core Losses

The losses caused by the core material will be represented here as a resistance (R_p) in parallel with the input. This resistance depends on:

- The sort of ferrite material
- The frequency
- The quantity L/μ_r
- The maximum flux density B_{max}.

In the small signal case ($B_{max} \rightarrow 0$), R_p can be calculated with the aid of curves of the type shown in Fig.1[(1)]. In these curves a comparison is made between different core materials based on equal core dimensions and equal number of turns. It can be seen that 4C4 and 4C6 are the best materials for frequencies above approximately 2.5 MHz. In the high v.h.f. region IZ2 ferroxplana shows interesting properties as can be seen from the same figure.
The power handling capability of a transformer is closely dependent on the behaviour of R_p as a function of B_{max}. For the section of the B-H curve with which we are dealing, B_{max} can be calculated using the formula:

$B_{max} = V_{max}/\omega \times A \times n$

in which:

B_{max} = maximum flux density in T[(2)]

$\omega = 2\pi$ times frequency in Hz

A = ferrite cross section in m^2

n = number of turns

V_{max} = maximum value of voltage across n turns in V.

(1) The curves of Figs 1 to 7 have been drawn from measurements on single samples of the ferrite materials. Thus the average curves may differ somewhat from those shown.

(2) The letter T stands for Tesla, the unit of magnetic flux density in the SI unit system. The following relationship holds: $1T = 1\ Wb/m^2 = 1\ V_{sec}/m^2 = 10000$ gauss.

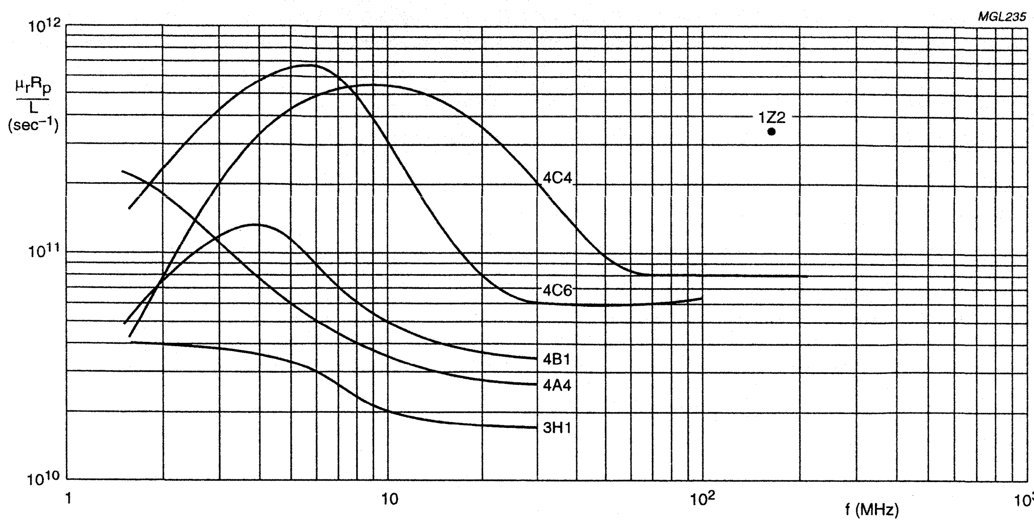


Fig.1 Curves of $\mu_r R_p/L$ plotted against frequency for our various ferrites. The curves have been plotted for small signal conditions ($B_{max} \rightarrow 0$).

In Figs 2 to 7 the quantity $\mu_r R_p/L$ is given for different ferrite materials as a function of the product $B_{max} \times f$ with the frequency as a parameter. The product $B_{max} \times f$ has been chosen because, for most transformers, its value remains constant for changing frequency. From Figs 2 to 7 it can be seen that R_p decreases as B_{max} increases, especially at lower frequencies. This forms the primary limit on the power handling capability of these transformers. If 4C4 material (Fig.5) is used in the h.f. region, the $B_{max} \times f$ product must not be higher than approx. 2×10^4 T.Hz. Combining this with the choice of L according to the second equation in Section 3.1, we find that the power loss caused by the core material will be no more than 1%. At frequencies of 30 MHz and higher it seems that higher $B_{max} \times f$ products, perhaps up to 10^5 T.Hz, can be used. For IZ2 ferroxplana this has already been confirmed by measurements at 165 MHz.

A very conservative choice of the B_{max} value must also be avoided because this leads to a greater length of the transmission line and consequently more loss at the high end of the band.

4 INFLUENCE OF THE TRANSMISSION LINE ON PERFORMANCE

4.1 Resistive Loss and Power Handling

The power loss in the transmission line depends on:

- The type of line
- The frequency
- The length.

Data on power loss in some 50 Ω coaxial cables is given in Fig.8. This power loss and the allowable maximum cable temperature restrict the power handling of the cable. The maximum power which can be transmitted depends on the type of cable and the frequency; data is given in Fig.9.

4.2 Mismatch loss

Another kind of loss caused by the transmission line can occur if the characteristic impedance of this line is not the required value. This results in a mismatch being maximum at the high frequency end of the band. The amount of mismatch depends on:

- The ratio between the length of the line and the wavelength on the line
- The ratio between the required and the actual value of the characteristic resistance.

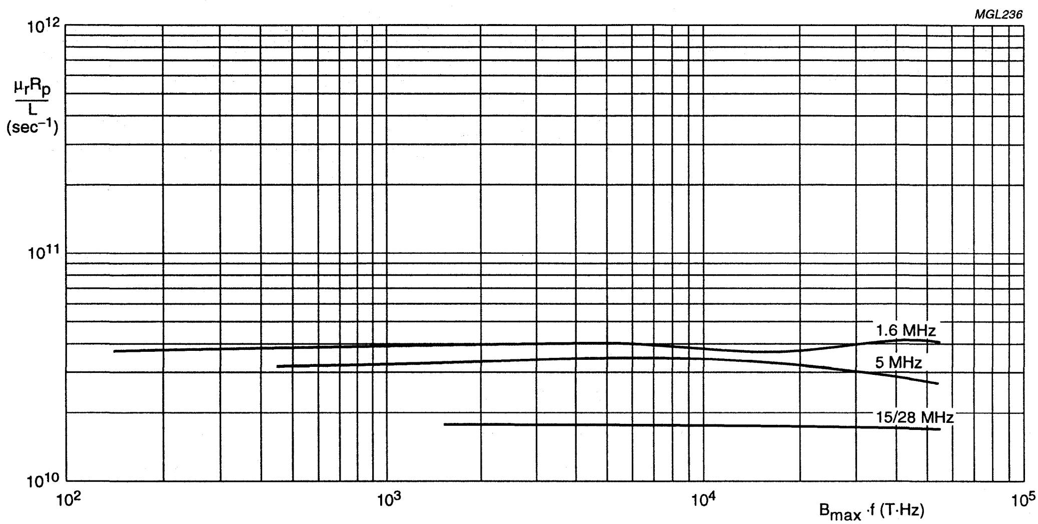


Fig.2 3H1 material.

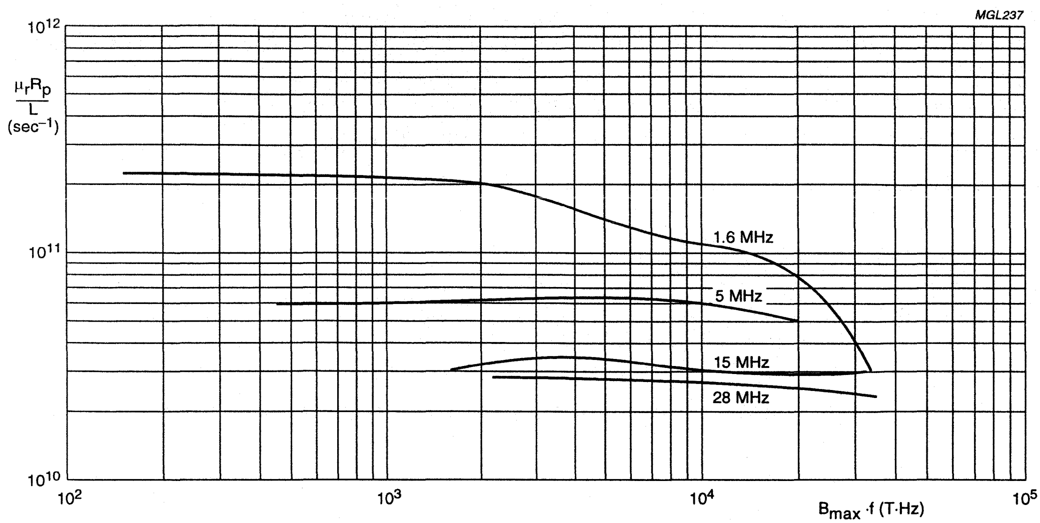


Fig.3 4A4 material.

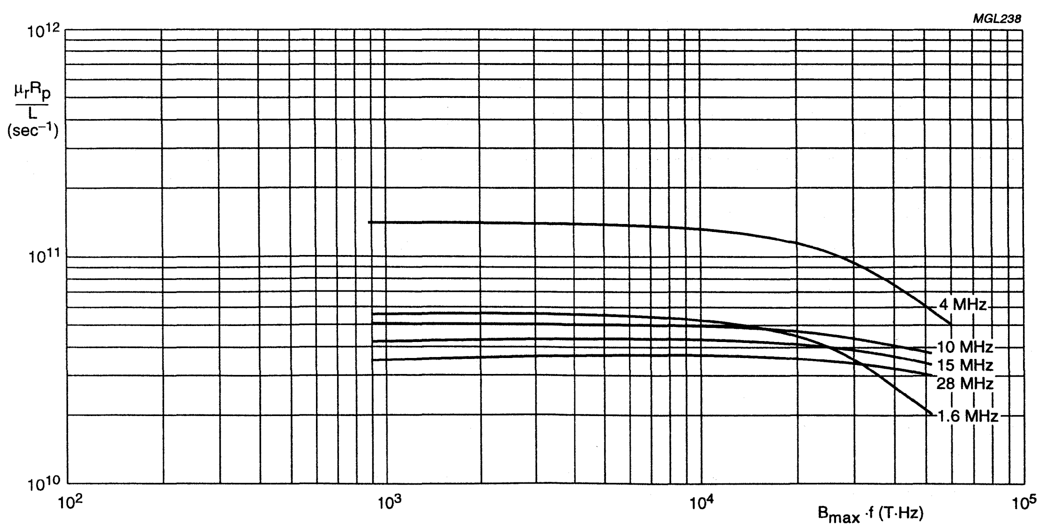


Fig.4 4B1 material.

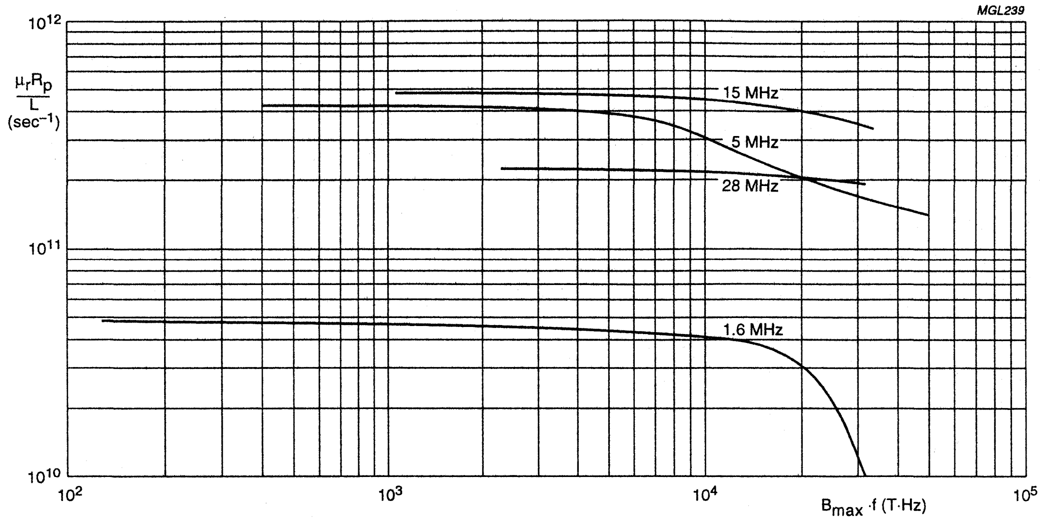


Fig.5 4C4 material.

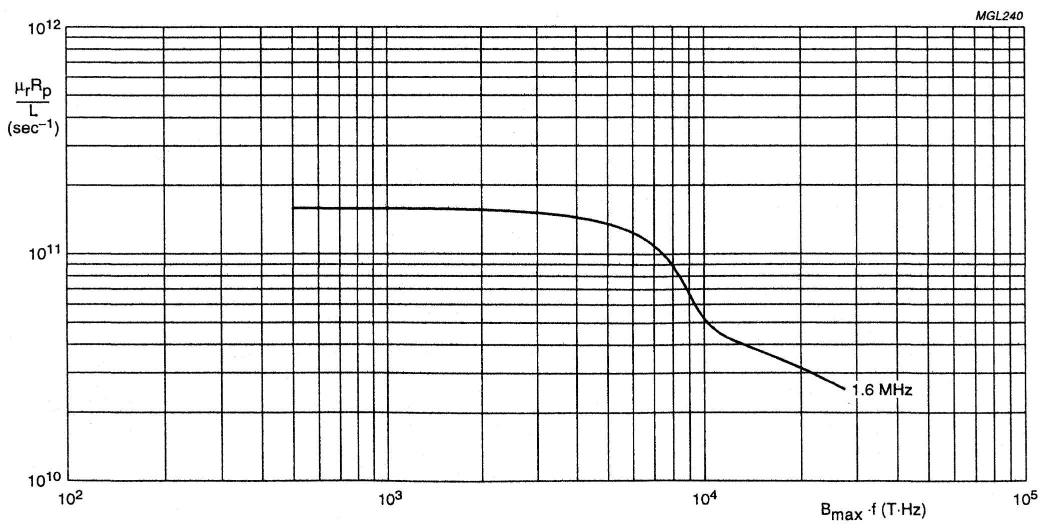


Fig.6 4C6 material.

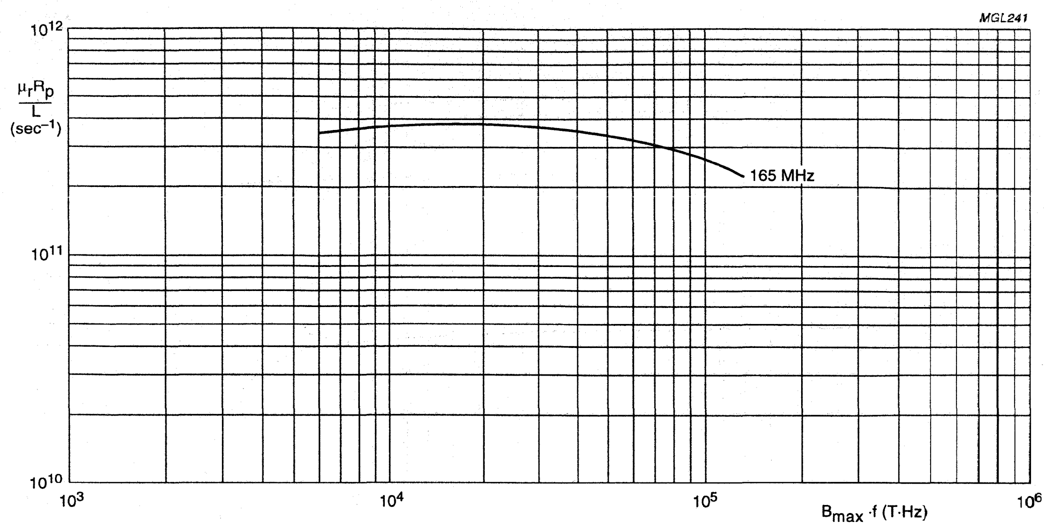


Fig.7 1Z2 material.

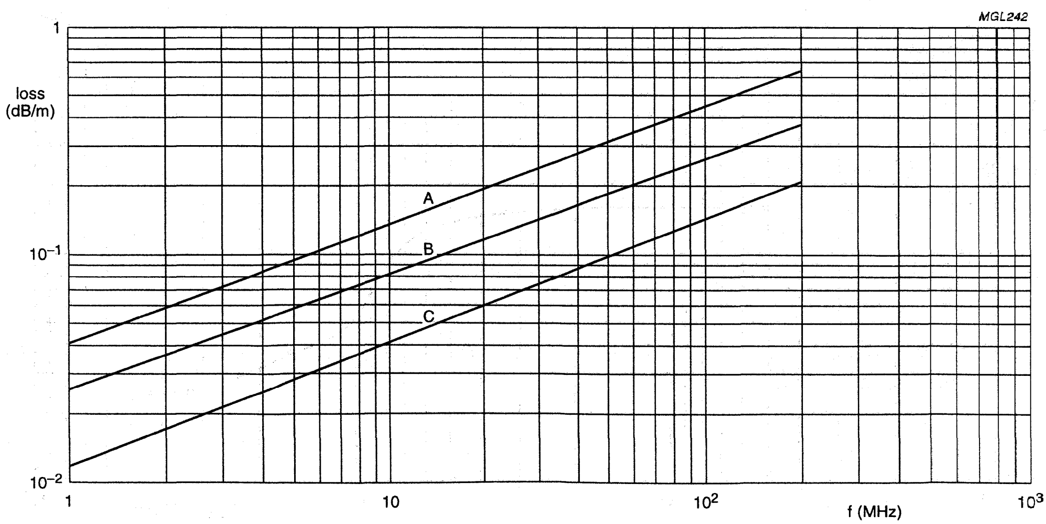


Fig.8 Curves of power loss plotted against frequency for three 50 Ω coaxial cables. A: diameter = 1.7 mm. B: diameter = 2.8 mm. C: diameter = 5 mm.

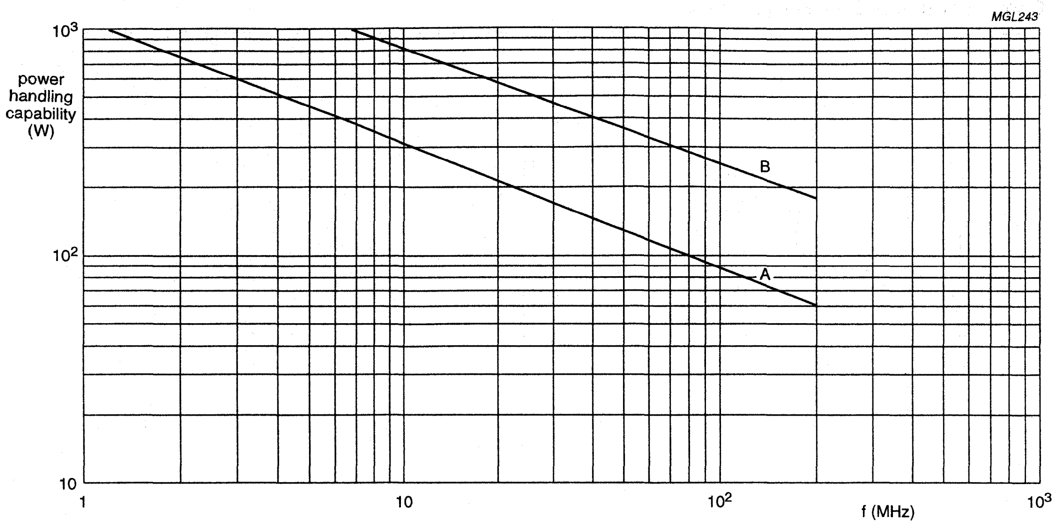


Fig.9 Curves of power handling capability plotted against frequency for two 50 Ω coaxial cables.
A: diameter = 2.8 mm. B: diameter = 5 mm.

From transmission line theory the input impedance is given by:

$$Z_{in} = R_{in} \times \frac{1 + jr\tan\beta l}{1 + j\frac{1}{r}\tan\beta l}$$

in which:

R_{in} = midband input resistance

r = ratio between the actual and the required characteristic resistance

$\beta = 2\pi/\lambda$

λ = wavelength on the line (for 50 Ω coaxial cables approx. 67-70% of wavelength in free space)

l = length of the line.

If the deviation of Z_{in} from the required value is unacceptably large it is in many cases possible to make use of the compensation technique described in Section 5.2.

5 COMPENSATION TECHNIQUES

5.1 Compensation at Low Frequencies

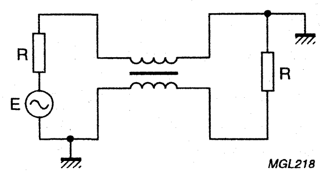


Fig.10 Schematic diagram.

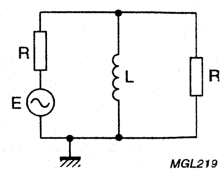


Fig.11 Low frequency equivalent diagram.

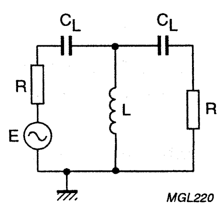


Fig.12 Equivalent diagram with compensation.

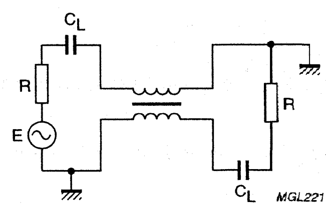


Fig.13 Schematic diagram with compensation.

Compensation will be illustrated by means of the phase reversing transformer. The schematic diagram is given in Fig.10 and the equivalent diagram for the low frequency end of the band is shown in Fig.11. For compensation we add two equal capacitors C_L such that a high-pass T-filter section is formed (Fig.12). According to filter theory:

$$C_L = 2L/R^2$$

The original diagram of Fig.10 is now transformed to the new one of Fig.13. If L is dimensioned according to eq.(2) the input impedance without compensation at the lowest frequency is R//(+ j4R). With compensation the input impedance is (.999R//+j264R), illustrating that the mismatch has been reduced to a negligible level.

For some types of transformer, the capacitor at the output must have a different value from that at the input. With a l : n^2 impedance transformer, for instance, it must be n^2 times smaller than the capacitor at the input.

Sometimes two or more transformers must be connected in cascade. In such a case low frequency compensation is possible if a high-pass π-filter section is used (Fig.14). When the parallel inductance of the transformers at the interconnecting point are both approximately equal to L, the capacitance of C_L must be $L/2R^2$.

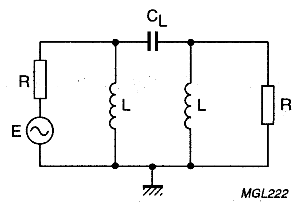


Fig.14 Equivalent diagram of cascaded transformers with compensation.

5.2 Compensation at High Frequencies

This is only necessary when the characteristic resistance of the transmission line differs from the required value. A situation often met with in practice is that in which the required characteristic resistance is lower than that of the available line. Taking the simple case of the phase reversing transformer (Fig.15) with a required characteristic resistance equal to R, we find that compensation for an actual value equal to r × R can be made as follows. In parallel with the load resistance, we connect a capacitor of such a value that at the highest frequency the real part of the input admittance becomes 1/R. The resulting imaginary part of the input admittance is tuned out by means of a capacitor in parallel with the input. Both capacitors turn out to have the same value; given by

$$C_H = \frac{1}{\omega_{max} rR\tan\beta l}\left\{1 - \sqrt{1 - \left(r^2 - 1\right)\tan^2\beta l}\right\}$$

in which $\omega_{max} = 2\pi$ times the maximum frequency. The schematic diagram is shown in Fig.15.

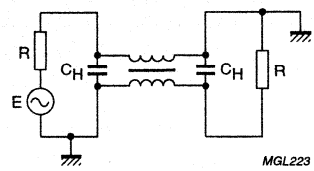


Fig.15 Phase reversing transformer with high frequency compensation.

The result of this compensation is an exact match at the maximum frequency. There will be however, a slight mismatch at lower frequencies which is many times smaller than that at the maximum frequency without compensation.
A combination of high and low frequency compensation is of course possible.

6 TRANSFORMER CONFIGURATION

Because of the variety of the existing configurations it is hardly possible to give a complete survey. Therefore a restriction will be made to some principally different types.

6.1 Phase Reversing Transformer

This type has already been discussed in the previous section.

6.2 Balanced to Unbalanced Transformer

The schematic diagram is shown in Fig.16. This type can be considered as a modification of the phase reversing transformer. The primary inductance in this case is 4 times the inductance of the winding between the points A and B because of the voltage division. If low frequency compensation is used, a capacitor equal to $2C_L$ must be placed in series with each input connection (see Section 5.1) to preserve symmetry, and one capacitor equal to C_L in series with the output (point B).

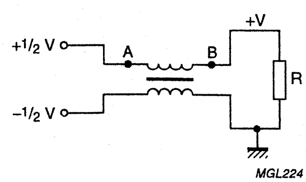


Fig.16 Balanced to unbalanced transformer.

6.3 Symmetrical(1) 1 : 4 Impedance Transformer

The schematic diagram is given in Fig.17. Two cables each having a characteristic resistance of 2R, can be wound on a common core. The direction of the windings follows from the voltage division. Low frequency compensation can be made with a capacitor equal to $2C_L$ (see Section 5.1) in each of the input leads and a capacitor equal to $1/2C_L$ in each of the output leads.

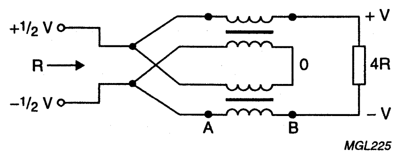


Fig.17 Symmetrical 1 : 4 impedance transformer.

6.4 Asymmetrical 1 : 4 Impedance Transformer

If, in the 1 : 4 impedance transformer of Section 6.3, the points A and B are connected to earth it is no longer possible to wind the two lines on a common core. In fact the lower line may be wound on an ‘air core’ because there is no voltage difference between the points A and B. The logical next step is to omit the lower line completely (with a consequent slight phase difference between the lines). Then we get the transformer shown in Fig.18. The characteristic resistance of the transmission line has again an optimum value of 2R. But even if this value is chosen the input impedance is not constant as a function of frequency. From theory (see Ref.5) it is:

$$Z_{in} = R \times \frac{2\cos\beta l + jr\sin\beta l}{1 + \cos\beta l + j\frac{1}{r}\sin\beta l}$$

in which r = ratio between the actual characteristic resistance and 2R.

(1) Terminology in normal use is employed to describe the various transformer configurations. However the terms ‘symmetrical’, ‘balanced’ and ‘push-pull’ are used here synonymously to mean ‘antiphase port signals having equal amplitudes with respect to ground’, while likewise ‘asymmetrical’, ‘unbalanced’ and single-ended’ are synonymous with ‘one port terminal grounded’. Strictly defined, the terms ‘asymmetrical, and ‘unbalanced’ also apply to unequal port terminal values with respect to ground.

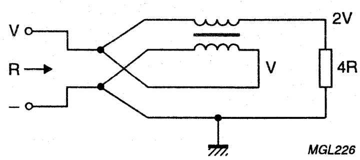


Fig.18 Asymmetrical 1 : 4 impedance transformer.

If r > 1 high frequency compensation is sometimes possible. A capacitor C_1 given by:

$$C_1 = \frac{1+\cos\beta l-\sqrt{(1+\cos\beta l)^2-r^2\sin^2\beta l}}{\omega_{max} rR\sin\beta l}$$

must then be connected across the input and a capacitor C_2 given by: $C_2 = \dfrac{2+\cos\beta l-\sqrt{(1+\cos\beta l)^2-r^2\sin^2\beta l}}{4\omega_{max} rR\sin\beta l}$

must be connected across the output.

6.5 Symmetrical 9 : 1 Impedance Transformer

The schematic diagram is given in Fig.19. The two transmission lines have an optimum characteristic resistance of 3R. They can again be wound on a common core, and the third line omitted as in the previous case. The input impedance is given by: $Z_{in} = 9R \times \dfrac{4+5\cos\beta l+j6r\sin\beta l}{9\cos\beta l+j\frac{6}{r}\sin\beta l}$

in which r is the ratio between the actual characteristic resistance and 3R.
If r > 1 high frequency compensation is sometimes possible. A capacitor C_1 given by:

$$C_1 = \frac{4+5\cos\beta l-\sqrt{9\left(3\cos^2\beta l+4\cos\beta l+2\right)-36r^2\sin^2\beta l}}{6\omega_{max} rR\sin\beta l}$$

must than be connected across the low impedance side, and a capacitor C_2, given by:

$$C_2 = \frac{9\cos\beta l-\sqrt{9\left(3\cos^2\beta l+4\cos\beta l+2\right)-36r^2\sin^2\beta l}}{54\omega_{max} rR\sin\beta l}$$

must be connected across the high impedance side.

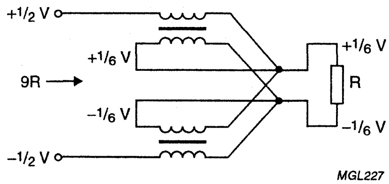


Fig.19 Symmetrical 9:1 impedance transformer.

6.6 Asymmetrical 1 : 9 Impedance Transformer

In this transformer (see Fig.20), two transmission lines are required, each having an optimum characteristic resistance of 3R. Although these lines can be wound on a common core, the upper line must have twice the number of turns of the lower line, because of the voltage division. The third line has again been omitted.

High frequency compensation follows the same principle as that used in previous sections.

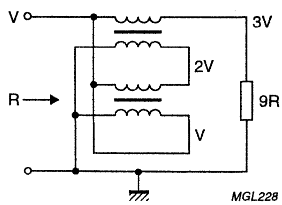


Fig.20 Asymmetrical 1 : 9 impedance transformer.

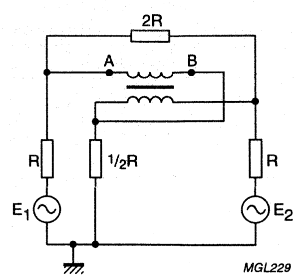


Fig.21 Single-ended hybrid.

6.7 Single-ended Hybrid

This circuit (see Fig.21) permits the combination of two signals in a common load (R/2) in such a way that the signal sources do not influence each other. When the two signals have different frequencies the power is equally divided between the resistors R/2 and 2R. When the two signals have the same frequency, phase and amplitude, all the power is delivered to R/2. The optimum value of the characteristic impedance of the transmission line is equal to R. At the low frequency end of the band the isolation between the sources depends on the inductance of the winding. When the isolation is expressed as a power ratio S the inductance between the points A and B must be: $L = \frac{R}{8\omega_{min}}\sqrt{S-1}$

Even when the optimum characteristic impedance is chosen, high frequency compensation has been found to have a marked influence on the isolation. Practically it has been found that a small capacitor must be connected in parallel with R/2.

To illustrate the degree of isolation that may be expected in a practical design, an example is given of a hybrid transformer designed for the frequency band of 1.6 to 28 Mhz. The requirement was to combine two signals of different frequency and equal power (3 W in 100 Ω) in a single 50 Ω load with a minimum isolation of 40 dB between the sources.

From the equation $L = \frac{R}{8\omega_{min}}\sqrt{S-1}$, it follows that L must be 125 μH minimum. Because of this high inductance it was decided to choose 3H1 material. An available 23 × 14 × 7 mm toroid belonged to 'group 5' which meant that the minimum μ_r was 2680(1).

The required number of turns was 9. The optimum value of the characteristic resistance is 100 Ω, but for reasons of convenience 150 Ω miniature twin lead was used. The calculated value of B_{max} was 87 gauss at 1.6 MHz. High frequency compensation was achieved by means of a 33 pF capacitor in parallel with the 50 Ω load resistance. The isolation between the sources measured as a function of frequency is given in Table 1 below, illustrating that the minimum isolation requirement of 40 dB has been fulfilled over the desired frequency band.

(1) For the convenience of the user the toroids of ferroxcube 3H1 are delivered sorted into groups of approximately equal μ-value. The μ-value is indicated by the colour of the cicumference of the toroids, see *"Data Handbook System"*. Groups are not separately available.

Table 1

f (MHz)	ISOLATION (dB)
0.5	33
1	41
1.6	42.5
5	40.5
15	41
28	43
40	32

6.8 Push-pull Hybrid

Two different versions will be discussed. In the first one the impedance level is stepped-up by a factor of two and in the second the impedance level is stepped-down by a factor of two.

6.8.1 IMPEDANCE STEP-UP TYPE

The two transmission lines (see Fig.22) have an optimum characteristic resistance equal to R and they can be wound on a common core.

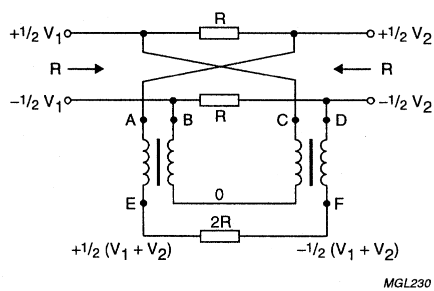


Fig.22 Push-pull hybrid with impedance step-up.

A hybrid can always be used in two ways. The first way has been mentioned in Section 6.7. The second way is the inverse of the first i.e. the power from a single source is equally divided between two loads which are isolated from each other. The latter arrangement allows a more convenient calculation of the lower frequency limit. To do this we must know the effective inductance in parallel with 2R. The voltage across this resistor is 4 times the voltage between the points D and F and therefore the effective inductance in parallel with 2R is 16 times the inductance between the points D and F. For low frequency compensation the effective inductance in parallel with 2R can be considered as two equal inductances in series – one between points E and O and one between points F and O – each having a value of 8 times the inductance between points D and F. The hybrid can then be considered as two balanced to unbalanced transformers on a common core and the compensation can be made as described in Section 6.2.

6.8.2 IMPEDANCE STEP-DOWN TYPE

This hybrid (see Fig.23) is identical to the previous one except that the transmission lines on one side have been connected in parallel instead of in series. When this hybrid is used for the combination of two signals which have the same frequency, phase and amplitude, the ferrite core will not be magnetized. However when V_2 becomes zero, the voltage across each winding will be $V_1/4$ and the voltage across R/2 will be $V_1/2$. This means that the effective inductance in parallel with R/2 becomes 4 times the inductance of a single winding. A similar approach must be used in finding the winding V/turn when calculating B_{max}.

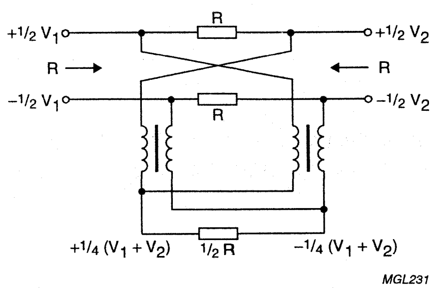


Fig.23 Push-pull hybrid with impedance step-down.

7 PRACTICAL EXAMPLES

It is possible to combine some of the functions, mentioned in Chapter 6, in one transformer. In the two examples given simple calculations show the method used in designing for a particular application.

7.1 12.5 Ω Balanced to 50 Ω Unbalanced Transformer

In this case, the transformers described in Sections 6.2 and 6.3 have been combined. The schematic diagram is shown in Fig.24. A transformer of this type is required for a wideband s.s.b. transmitter in the frequency range of 1.6 to 28 MHz. It must be able to handle a peak envelope power of 80 W. The input impedance of 12.5 Ω balanced and the output impedance is 50 Ω unbalanced. The total amount of resistive and reflection losses is required to be below 5% (power).

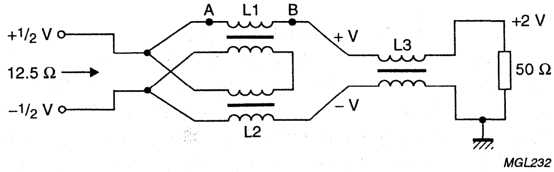


Fig.24 12.5 Ω balanced to 50 Ω unbalanced transformer.

The transformer has been wound on a single 4C4 toroid of 36 × 23 × 15 mm. Windings L1 and L2 must have a characteristic resistance of 25 Ω; they consist of two 50 Ω coaxial cables of 2.8 mm diameter in parallel. Winding L3 must have a characteristic resistance of 50 Ω; a single 50 Ω coaxial cable of 2.8 mm diameter has been used. The winding direction follows from the voltage division. From this it is also clear that windings L1 and L2 must have an equal number of turns and that winding L3 must have twice the number of winding L1.

We can calculate the lower frequency limit from the effective inductance in parallel with the 50 Ω load resistance. We allow a reactance of +j 200 Ω at 1.6 Mhz, corresponding to an inductance of 20 μH, in parallel with the 50 Ω load (see Section 3.1). As the voltage between points A and B is ¼ of the output voltage, the inductance between these points will be 20/16 = 1.25 μH. The corresponding number of turns is:

$$n = \sqrt{\frac{L \times 1}{\mu_o \mu_r A}}$$

in which 1/A = 9.42 cm^{-1} and μ_r is taken to be 100. This gives:

n = 3.06

We take = 3.5 turns, making the inductance in parallel with the 50 Ω load resistance equal to:

$$20\left(\frac{3.5}{3.06}\right)^2 = 26.2\ \mu\text{H minimum}$$

The measured value was actually 39 μH, because the μ_r of the core used was greater than 100.

The maximum flux density B_{max} can be calculated when the maximum voltage across the windings is known. The peak value of the voltage across the 50 Ω load resistance for an 80 W power level is:

$$V_p = \sqrt{2 \times 80 \times 50} = 89.5\text{V}$$

and between points A and B: 89.5/4 = 22.35 V. The ferrite cross section for this core is 0.976 × 10^{-4} m^2. So at 1.6 MHz the maximum flux density is:

$$B_{max} = \frac{V_{max}}{\omega A n} = \frac{22.35}{2 \times \pi \times 1.6 \times 10^6 \times 0.976 \times 10^{-4} \times 3.5} = 65.4 \times 10^{-4}\text{T} \text{ or } 65.4 \text{ gauss.}$$

This corresponds to a $B_{max} \times f$ product of 1.05 × 10^4 T. Hz. From Fig.5 it can be seen that up to this level the variation in core losses in only very small. The minimum value of the parallel loss resistance referred to the 50 Ω level (see Fig.5) is:

$$R_p = \frac{L}{\mu_r} \times 41 \times 10^9 = \frac{26.2 \times 10^{-6}}{100} \times 41 \times 10^9 = 10.7\ \text{k}\Omega$$

So the core losses are: 50/10 700 × 100% = 0.47% maximum.

The cable can handle a power of 170 W at 28 MHz and it has a loss of 0.135 dB/m at this frequency. The length of the cable (the sum of L_1 and L_3) is about 60 cm, giving a maximum cable loss of approximately 1.9%.

When the transformer was driven from an unbalanced 50 Ω source and loaded with two resistors of 6.25 Ω at the balanced side (connecting point of the resistors earthed) the power loss and asymmetry were so small that they could not be measured. The input impedance at the unbalanced side as a function of frequency is given in Table 2.

Table 2

f (MHz)	R_p (Ω)	X_p (Ω)
1.6	49.3	+j 395
5	49.6	+j 1250
15	50.2	+j 21200
28	50.2	–j 1060

7.2 50 Ω Unbalanced to 5.55 Ω Balanced Transformer

In this case the transformers described in Section 6.2 and 6.5 have been combined. The schematic diagram is given in Fig.25. A transformer of this design is again required for a wideband s.s.b. transmitter in the frequency range of 1.6 to 28 MHz. The required peak envelope power handling is 5 W, with an input impedance of 50 Ω unbalanced and an output impedance of 5.55 Ω balanced.

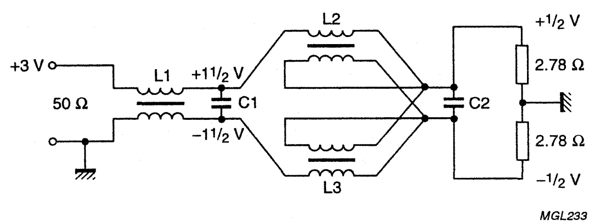


Fig.25 50 Ω unbalanced to 5.55 Ω balanced transformer.

The transformer can be wound on a single 4C4 toroid of 23 × 14 × 7 mm. Winding L_1 must have a characteristic resistance of 50 Ω; this has been approached by a twisted pair of enamelled copper wires of 0.45 mm diameter (R_c = 52 Ω). Windings L_2 and L_3 must have a characteristic resistance of $16\frac{2}{3}$ Ω. For this purpose four enamelled copper wires of 0.22 mm diameter have been twisted and diagonally interconnected as shown in Fig.26; the characteristic resistance was found to be 30 Ω, making a high-frequency correction necessary. The required compensation, determined experimentally gave values for C_1 of 22 pF and for C_2 of 270 pF.

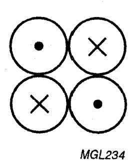


Fig.26 Interconnection of winding wires. In the cross-section shown, the two wires indicated by dots are interconnected, as are those indicated by crosses. This configuration gives a maximum winding capacitance, necessary for a low characteristic resistance.

From the voltage division it follows that winding L_1 must have 1½ times the number of turns of windings L_2 and L_3. The required number of turns can be calculated in the same way as in the previous section. To get a parallel input inductance of 20 μH minimum, 9 turns are required for winding L_1. The measured value was approx. 30 μH.

Calculation of B_{max} according to the method of Section 7.1 gives a value of approx. 40 gauss at 1.6 MHz. This is so low that a smaller core could be chosen. The reason for not doing this is that the smaller core has not sufficient room for the windings. In Table 3 the input impedance is given as a function of frequency.

Table 3

	WITHOUT H.F. COMPENSATION		WITH H.F. COMPENSATION	
	R_p (Ω)	X_p (Ω)	R_p (Ω)	X_p (Ω)
1.6	49	+j 300	48	+j 370
5	50	+j 360	49	+j 840
15	56	+j 220	50	+j 1400
28	71	+j 213	51	−j 11000

If there is no high frequency compensation, the variation in impedance is rather large. This is caused by:

- The characteristic resistance of the transmission lines L_2 and L_3 being 30 Ω instead of 16⅔ Ω.
- The electrical length of the windings L_2 and L_3. Measurements have shown that the wave-length on these lines is only 41% of the wavelength in free space – the decrease in wave-length being caused by the twisting of the wires, the dielectric constant of the wire insulation and the influence of the μ_r of the ferrite core.
- The inductance of the load resistors.

The power loss measured at 28 MHz was 0.34 dB. At lower frequencies it was too small to be measured accurately. Voltage asymmetry between both terminals was less than 4%.

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Design of H.F. Wideband Power Transformers; Part II — ECO7213

1 SUMMARY

In part I of this report (ECO6907) the transmission line transformer has been discussed extensively. In this second part attention has been paid to the conventional transformer as a wideband matching element in e.g. S.S.B. transmitters. The main problem in these transformers is stray-inductance. Some H.F. compensation methods are discussed and a design example is given.

2 INTRODUCTION

Report ECO6907 (Ref. 1) has been devoted entirely to the design of transmission line transformers. This type of transformer has undoubtedly the advantage of the largest possible bandwidth. However it has also some drawbacks:

1. The impedance transformation ratio is restricted to $(n : m)^2$ in which n and m are small integers
2. They are difficult to construct when a number of windings must be combined.

Therefore it is certainly worthwhile to consider the possibility of applying a conventional transformer if the abovementioned problems arise.

3 L.F. LIMITATIONS OF CONVENTIONAL TRANSFORMERS

These limitations are the same as for transmission line transformers, viz. parallel inductance and maximum flux density. They have been described in the abovementioned reports including compensation methods for the parallel inductance.

4 H.F. LIMITATION OF CONVENTIONAL TRANSFORMERS

The most important property that limits the H.F. performance of a conventional transformer is the well-known stray-inductance. The equivalent circuit of the transformer for this frequency region is shown in Fig.1.

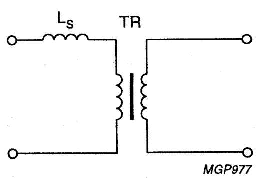

Fig.1

L_S is the stray-inductance and TR an ideal transformer. An easy way of measuring L_S is to measure the reactance between the primary terminals when the secondary is short-circuited. This can be done e.g. with the H.P. Vector Impedance meter. The most accurate result is obtained when the measurement is made at the highest frequency of operation and on the high-ohmic winding.

It is obvious that L_s must be kept as small as possible to avoid degradation of the H.F. performance of the transformer. For this end the following measures are recommended:

1. The windings must be as close to the core and to each other as possible
2. Each winding must be divided equally around the whole periphery of the core
3. Each winding must cover the core as much as possible.

Some practical steps that can be taken are:

1. The use of copper foil for the low-ohmic winding; this can be in direct contact with the core as the resistivity of the ferrite is very high. For better covering of the core two windings can be connected in parallel in such a way that one winding is wound in between the other one; the isolation material required in this case must be very thin.
2. For the high-ohmic winding enamelled copper wire can be used. An appreciable reduction of L_s can be obtained by parallel connection of two or more wires.

5 H.F. COMPENSATION OF CONVENTIONAL TRANSFORMERS

In Ref. 2 some forms of compensation have been described. They are compared in Table 1.

Table 1

NUMBER OF COMPENSATION ELEMENTS	0	1	2
Maximum X/R	0.18	0.44	1.09

Table 1 is based on a maximum input V.S.W.R. of 1.2. The quantity X/R is the reactance of the stray-inductance (referred to the primary) divided by the nominal input resistance of the transformer. Compensation with one element is possible either by connecting a capacitor in parallel with the primary winding, or by connecting a capacitor in parallel with the secondary winding.

Compensation with two elements is carried out by connecting capacitors in parallel with both primary and secondary windings. This method has already been applied several times. A short description will be given with reference to Fig.2.

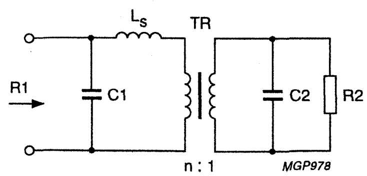

Fig.2

TR is an ideal transformer with a voltage transformation ratio of n : 1 (n > 1) and L_s is the stray-inductance (referred to the primary). R_1 is the nominal input resistance:

$R_1 = n^2 \times R2$

First we determine the normalized stray-inductance:

$L_{sn} = \frac{\omega_{max} \times L_s}{R_1}$, in which ω_{max} must be equal to or higher than 2π times the maximum frequency to be handled.

With the aid of Fig.5 we find the maximum input V.S.W.R (S) and the normalized correction capacitance (C_{1n}). Then C1 and C2 can be calculated:

$C_1 = \frac{C_{1n}}{\omega_{max} \times R_1}$ and $C2 = n^2 \times C_1$

A practical problem that can arise is that the capacitor across the low-ohmic winding must have such a high value that it approaches series resonance with its own lead inductance. In that case a sufficiently large number of smaller capacitors must be connected in parallel.

The practical limit to which the above described compensation system can be used is appr.:

$L_{sn} = 1$

If the stray-inductance is larger a more complicated compensation system is required. The above described system is based on a 3-element Chebyshev low-pass filter, but this can be extended to a 5-element network, which means that for the compensation 4 elements are required. This situation is depicted Fig.3.

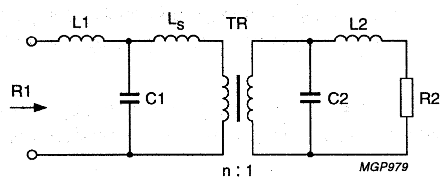

Fig.3

Two inductors (L1 and L2) have been added. The normalized elements versus the maximum input V.S.W.R. (S) have been given in Fig.6 (this graph and that of Fig.5 have been made with the aid of a computer program which is based on the design formulae for Chebyshev low-pass filters as can be found e.g. in Ref. 3.). From this graph it can be seen that L_{sn} may be as high as 1.77 for $S_{max} = 1.2$. A good practical limit is: $L_{sn} = 1.6$

The procedure for calculating the compensation elements is very similar to the previous case. We start again with determination of the normalized stray-inductance: $L_{sn} = \frac{\omega_{max} \times L_s}{R_1}$

With the aid of Fig.6 we find the maximum value of S and the normalized values of the correction elements C_{1n} and L_{1n}.

Now C_1 and L_1 can be calculated: $C_1 = \frac{C_{1n}}{\omega_{max} \times R_1}$ and $L_1 = \frac{L_{1n} \times R_1}{\omega_{max}}$

At the secondary side the correction components become:

$$C_2 = n^2 \times C_1 \text{ and } L_2 = \frac{L_1}{n^2}$$

In general L_2 is so small that the tracks on the p.c. board can perform this function.

6 A PRACTICAL EXAMPLE

For a low voltage S.S.B. amplifier a transformer was required with the following specification:

Frequency range: 1.6 – 28 MHz

Power handling: 52 W

Load impedance: 100 Ω

Input impedance: 4.6 Ω

The most suitable Ferroxcube material for this frequency range is 4C6. From the power handling point of view a toroid core will be chosen with the dimensions: 23 × 14 × 7 mm^3, catalog nr. 4322 020 91070. The parallel reactance at 1.6 MHz measured at the secondary side must be +j400 Ω (see Ref. 1), corresponding with an inductance of 40 μH. The required number of turns is then:

$$n_{sec} = \sqrt{\frac{L \times l}{\mu_o \times \mu_r \times A}}$$

in which $\frac{A}{l} = 0.5525 \text{ mm}$ for this core and $\mu_r = 120$ for 4C6 material, so:

$n_{sec} = 21.9$

A logical choice would be $n_{sec} = 22$. The voltage transformation ratio is $\sqrt{\frac{100}{4.6}} = 4.66$, by which the primary number of turns must be: $\frac{22}{4.66} = 4.7$

We choose: $n_{pr} = 5$.

The required transformation ratio can be approached better if the secondary number of turns is modified from 22 to 23. Now the secondary parallel inductance becomes 44 μH and the impedance transformation ratio $\left(\frac{23}{5}\right)^2 = 21.1$ by which the input impedance will be 4.74 Ω being appr. 3% higher than the required value.

L.F. compensation of the parallel inductance can be carried out by means of a single capacitor in series with the secondary (see Ref. 1):

$$C_L = \frac{L_{psec}}{R_{sec}^2} = \frac{44 \times 10^{-6}}{100^2} = 4400 \text{ pF}$$

A standard value of 4700 pF has been chosen.

The maximum voltage across the secondary winding is: $V_{sec} = \sqrt{2R_{sec} \times P} = \sqrt{2 \times 100 \times 52} = 102 \text{ V}$

Now the maximum flux density can be calculated:

$$B_{max} = \frac{V_{sec}}{\omega_{min} \times A \times n_{sec}}$$

in which A = 31.5 mm^2 for this core, so: $B_{max} = \frac{102}{2\pi \times 1.6 \times 10^6 \times 31.5 \times 10^{-6} \times 23} = 140$ gauss at 1.6 MHz

This gives a core loss of appr. 1% or 0.5 W.

To keep the stray-inductance low the transformer has been wound as follows:

- The primary consists of the parallel connection of two windings each having 5 turns of 4 mm wide copper foil. Each winding has been equally divided around the periphery of the core; one winding was wound in between the other one. Between these two windings a thin layer of isolation material was used.
- The secondary consists of the parallel connection of two windings each having 23 turns of 0.45 mm enamelled copper wire. The method of winding was the same as for the primary.

The stray-inductance measured at the secondary side was 0.67 µH. To make the correction less critical we choose a maximum frequency of 35 MHz instead of the specified 28 MHz. The normalized stray-inductance becomes then:

$$L_{sn} = \frac{2\pi \times 35 \times 10^6 \times 0.67 \times 10^{-6}}{100} = 1.47$$

From Fig.6 we find:

$S_{max} = 1.064$

$C_{1n} = 1.24$

$L_{1n} = 0.66$

In this case the index 1 applies to the secondary and index 2 to the primary. The compensation elements become:

$$C_1 = \frac{1.24}{2\pi \times 35 \times 10^6 \times 100} = 56.4 \text{ pF}$$

$$L_1 = \frac{0.66 \times 100}{2\pi \times 35 \times 10^6} = 0.3\ \mu\text{H}$$

C2 = 21.1 × 56.4 = 1190 pF
L2 = 0.3/21.1 = 0.0142 µH

For C1 a standard value of 56 pF was chosen. C2 consisted of the parallel connection of 330 pF and 3 × 270 pF being 1140 pF in total; the slightly lower value was chosen because of the series inductance of the capacitors. L2 was formed by the tracks on the p.c. board.

The first measurements on the compensated transformer showed a too high V.S.W.R. at 28 MHz together with a capacitive behaviour of the impedance from which we got the impression that it was over-compensated. This appeared to be due to the capacitance between the primary and the secondary winding. Therefore we reduced the values of the compensation elements by 10 to 20%. The new values are:

C1 = 47 pF

L1 = 0.27 µH

C2 = 980 pF (parallel connection of 2 × 270 pF and 2 × 220 pF)

L2 ≈ 2 × 6 nH (tracks on p.c. board)

The complete situation is depicted in Fig.4. The load impedance Z_L consisted of the parallel connection of 2 resistors of 15 Ω, 1 resistor of 12 Ω and a capacitor of 120 pF. The latter was added to compensate the series inductance of the resistors.

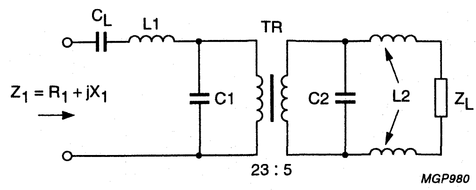

Fig.4

The results of the measurements have been summarized in Table 2.

Table 2

f (MHz)	R1 (Ω)	X1 (Ω)	V.S.W.R. (–)
1.6	98	–1.87	1.03
3.5	100.5	–2.1	1.02
7.0	98.3	–5.84	1.06
14	89.9	–4.41	1.12
20	87.4	+1.24	1.14
28	100	+7.18	1.07

It can be seen from Table 2 that the maximum input V.S.W.R has been reduced to 1.14. Without H.F. compensation this V.S.W.R. would have been appr. 3 at 28 MHz.

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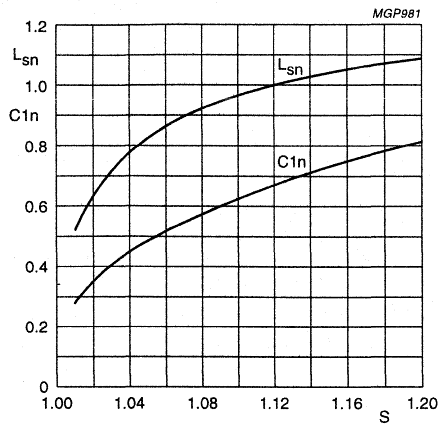

MGP981
1.2
L_{sn}
1.0
C1n
0.8
0.6
0.4
0.2
0
1.00
1.04
1.08
1.12
1.16
1.20
S
L_{sn}
C1n

Fig.5

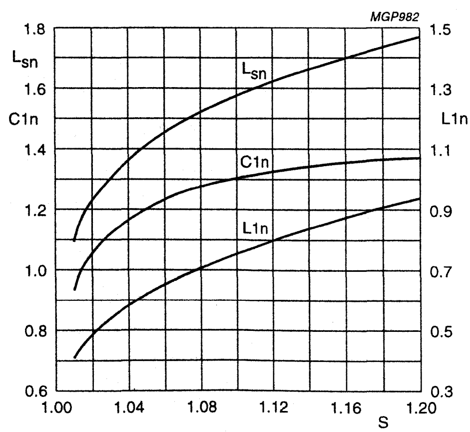

MGP982
1.8
L_{sn}
1.6
C1n
1.4
1.2
1.0
0.8
0.6
1.5
1.3
L1n
1.1
0.9
0.7
0.5
0.3
1.00
1.04
1.08
1.12
1.16
1.20
S
L_{sn}
C1n
L1n

Fig.6

Thermal aspects of flange-mounted r.f. power transistors

1 INTRODUCTION

R.F. power transistors often operate under conditions of severe mismatch. This often increases collector dissipation and consequently junction temperature. Failure mechanisms in high power transistors (breakdown, degradation, electromigration, thermal fatigue) are highly temperature dependent, so proper attention must be paid to their thermal conditions. However, it is an area where calculations are difficult and misunderstandings abound; this article is intended to clear up some of the misunderstandings and correct a number of misconceptions.

2 PRACTICAL POINTS:

- The central area of the flange directly under the crystal contributes much less to heat transfer than has hitherto been thought; it is the area under and around the mounting bolt heads that conducts the bulk of the heat away.
- Although lapping the contacting surfaces of both heatsink and flange does improve thermal conductivity, the improvement is less than if a very thin layer of heatsink compound is used.
- Both of the commonly used bolts (M3 and UNC4-40) provide sufficient pressure when torqued to between 0,6 and 0,75 Nm. Using higher torques with a view to improving thermal contact resistance is counterproductive. Thermal contact resistance is more likely to increase.
- Except in the case of the UNC4-40 bolt, the maximum pressures encountered under these conditions do not cause excessive plastic deformation of the underside of the flange, and the minimum is sufficient to provide good thermal contact throughout life.

3 THERMAL MODELS

Many thermal models have been proposed in efforts to provide an analytical base from which to calculate the thermal behaviour of operating transistors. Because of the number of assumptions that have to be made, none survive comparison with actual measurements. Particularly with regard to hot-spotting and thermal contact resistance, theory and practice often differ by a factor of three.

The most dangerous assumption is probably that the chip surface temperature can be averaged and, therefore, that a uniform heat flux exists on the surface of the silicon chip. Although a large number of small base areas are distributed over the chip surface in order to promote even heat distribution, this assumption assigns too low a temperature to certain critical points on the chip surface. Because the hottest point presents the highest reliability risk, averaging leads to this risk being underestimated.

The situation is made clearer if we consider the power dissipation per unit area and the temperature gradients in and near the crystal of a high power transmitting transistor. In the crystal itself, in the base area a few micrometres under the emitter fingers the dissipation is about 500 W/mm^2 with a temperature gradient of about 5000 K/mm; in the BeO disc, about 5 W/mm^2 with a gradient of 25 K/mm; and in the flange, 2 W/mm^2 with a gradient of 5 K/mm. Efficient heat distribution is, therefore, essential if junction temperature is to be held below 200 °C.

Other assumptions that undermine the validity of current thermal models are: that heat distribution is uniform; and that the base of the transistor flange and the heatsink surface are isothermic.

Figures 1 to 6 show known models. These illustrate the difficulties of calculating thermal resistance when boundary conditions have to be assumed. It is clear that the influence of the finite thermal resistance of the heatsink is great, as is that of the mounting base. The most important result is that for a thick heatsink the contact area formed by the annulus between 0,8r and r largely determines the thermal resistance of the whole contact area. These results are confirmed by measurements (described in the “Appendix”) that show that removing metal from the flange centre barely affects the thermal resistance of the contact area. Other reasons for the bolt head are being important are discussed below.

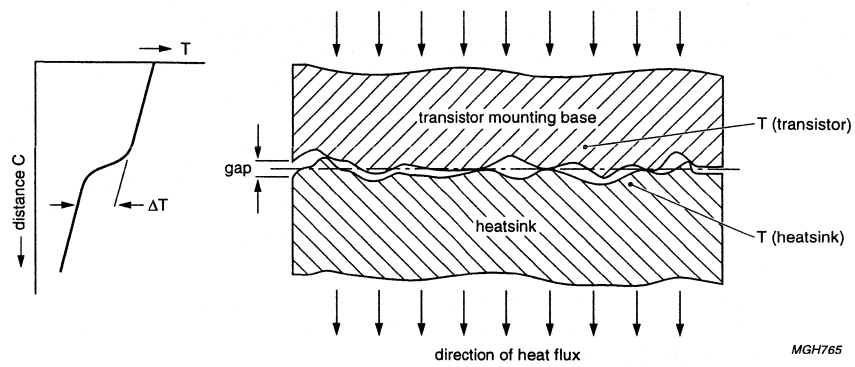


Fig.1 This rather simplified case is often mentioned in the literature to describe contact surface thermal resistance. It assumes a constant heat flux normal to the contact area. Thermal resistances can be calculated using the average gap between the surfaces (caused by micro-asperities, see Thermal contact) which is filled with air or heatsink compound. Ref. 1, 2.

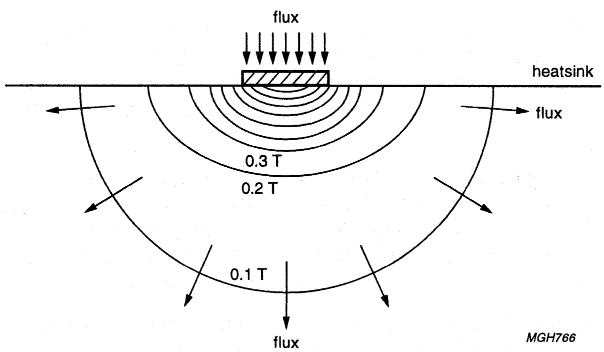


Fig.2 This theoretical approach assumes an infinite heatsink with a uniform constant heat flux normal to a circular contact area. The temperature distribution on the heatsink surface requires the solution of complete elliptic integrals. The results are plotted in Fig.3. The most important facts emerging from this approach are: the average angle of the heat flux in the heatsink is >60° to the direction of the assumed transistor heat flux; and that the thermal resistance of the heatsink is inversely proportional to the radius of the heat flux and not to the surface area of the heat flux. Ref. 3, 4.

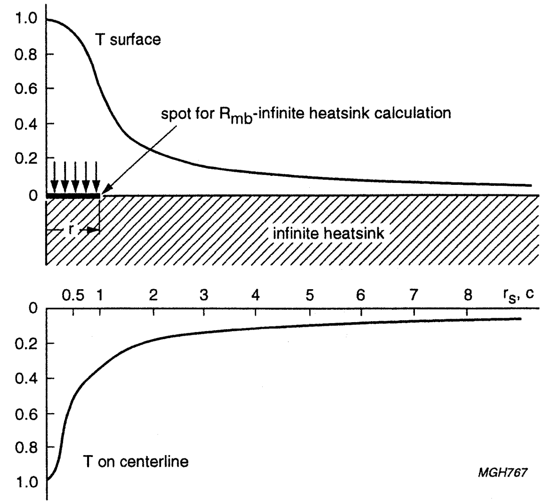


Fig.3 Temperature of (a) the heatsink surface and (b) the centre of the body of the heatsink normal to the surface, as calculated using the approach of Fig.2.

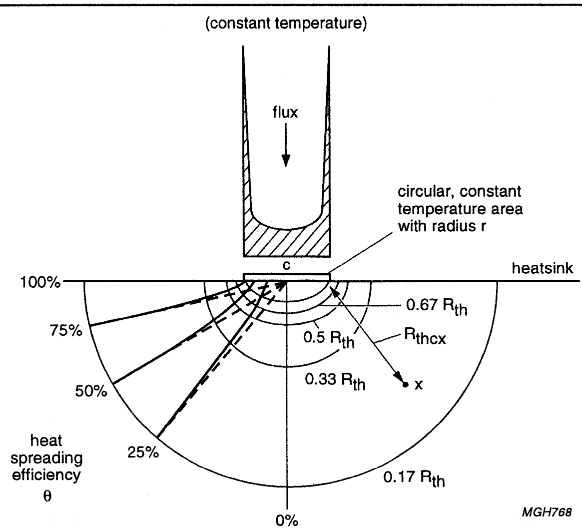


Fig.4 This approach assumes a constant mounting base temperature and a low contact thermal resistance. This also requires the solution of complete elliptic integrals, but with a simpler result for calculating the temperature at a distance x from the centre; Ref. 5, 6. For large distances the results are the same as for Fig.2. For an elliptic contact area (or, with slight error, for a rectangular flange) a form factor can be applied. The main difference with Fig.2 is in the flux, which has infinite intensity at the edge of the contact area. The most important result of this is that 50% of the total heat flux passes through an annulus of r – 0,9r; i.e., if a circle of 0,9r is removed from the contact area, thermal resistance is only doubled.

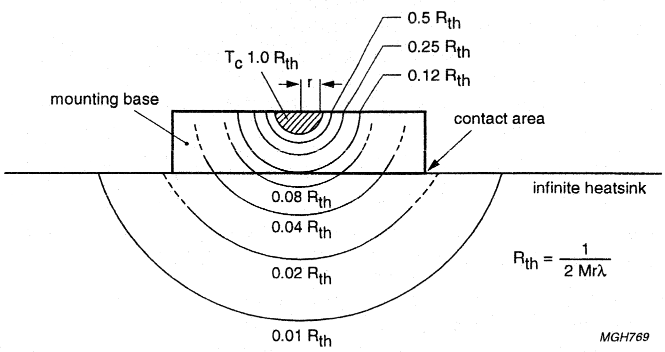


Fig.5 The fourth approach is to assume a small hemispherical heat source of constant temperature half buried in the upper surface of the flange. If flange and heatsink are of the same material and the thermal contact resistance is low, the isothermals will be hemispheres passing through flange and heatsink and temperature will decrease with the square of the distance.

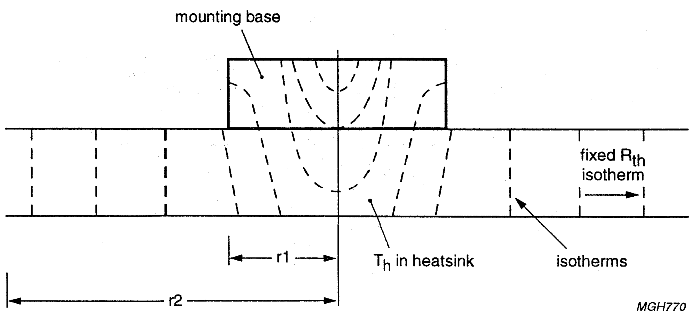


Fig.6 If, in the case of Fig.5 we assume the heatsink to be thin (thickness <r), the thermal resistance will be infinite if the heatsink is not connected to a point of fixed thermal resistance such as fins or water jacket. If, at a distance r2, such a (circular) connection does exist, the isotherms will be concentric circles on the surface of the heatsink and, if $r2 \approx 2r1$, heat flux will decrease linearly with distance. The R_{th} of the transistor will be higher because the heat spreads differently.

4 SURFACE CONDITIONS

Because of irregularities in their surfaces two apparently flat objects will probably contact over less than a thousandth of their common surface area when pressed together. Three types of surface irregularity are of interest to us here:

- Waviness, i.e., deviation from flatness (see Fig.7(a)). This includes the plastic deformation of the transistor flange cause by the differing coefficients of expansion of BeO and Cu. After the BeO disc has been attached the two materials contract at different rates, setting up stresses that deform the flange, making it slightly concave. Although the flange is subsequently ground, residual stresses cause the copper to creep and the flange is therefore very slightly concave (typically 7 μm) when delivered (see Fig.15).
- Grooving, a repetitive form of deformation that is usually the result of milling, turning, grinding, etc. This is rarely a problem in transmitting transistor flanges but may occur in heatsink, especially those of poor quality. (See Fig.7(b)).
- Non-repetitive micro-asperities, a random phenomenon that is reduced but not entirely removed by lapping or polishing. It is characteristic of all normal surfaces. (Fig.7(c)).

Surface irregularities of the last two types are usually expressed in terms of average roughness (r_a), as shown in Fig.7(c). Instead of arithmetic average. The r.m.s. value (a slightly higher value) is often used in the USA. Although most suited to defining the smoothness of sliding surfaces, r_a does not indicate the intimacy of contact between two surfaces, which is what concerns us here. A more useful way of expressing roughness for our purposes, one rarely used for transistor flanges, would be that of DIN4762, i.e., the percent bearing surface (t_p) at a given depth (c). Figure 8 compares r_a and t_p for a selection of surface profiles.

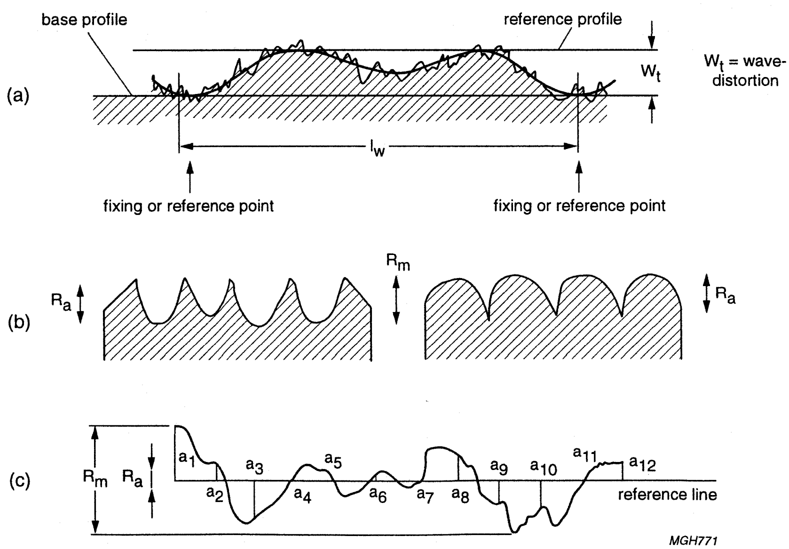


Fig.7 Three types of surface distortion of interest in thermal contacts. That of (a) can be cured by lapping or polishing whereas those of (b) and (c) can only be reduced.

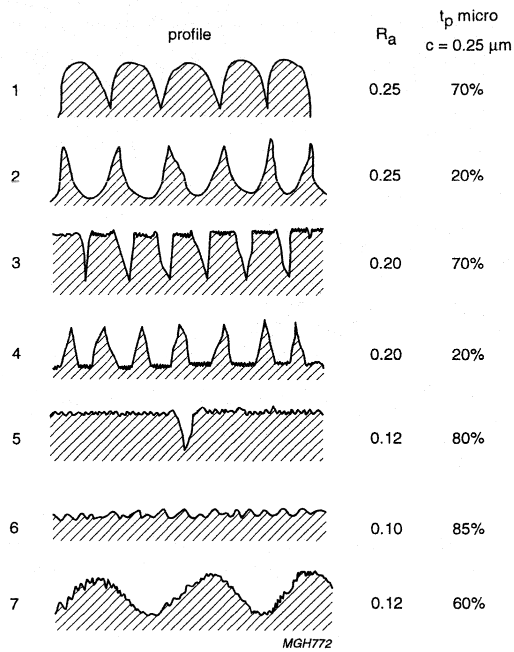


Fig.8 Although R_a is a good indication of the frictional behaviour of mating surfaces, it is less effective in defining the intimacy of contact as is needed for our purposes. A better indication is given by percent bearing surface, t_p, at a given depth, c, in this case 0,25 µm.

5 THERMAL CONTACT

From the foregoing it will be seen the contact conductance between two surfaces is the sum of the conductances of a very large number of metallic contacts in parallel with a similar number of air gaps (perhaps filled with heatsink compound). $R_{th\ mb\text{-}hs} = 1/h_t$ where $h_t = h_m + h_f$: h_m and h_f being the conductance of the metallic paths and of the air (or heatsink compound) paths, respectively.

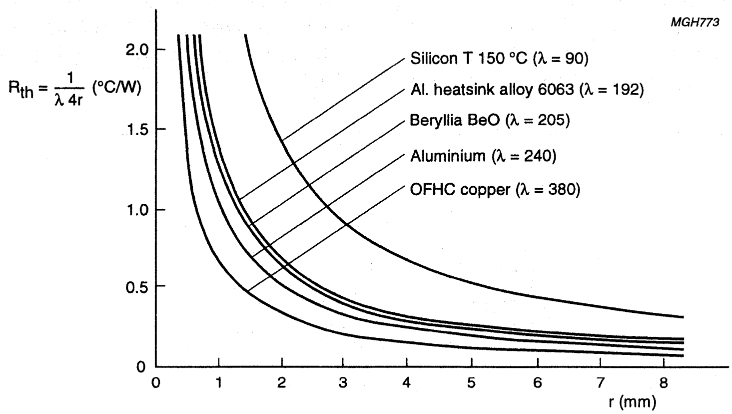


Fig.9 Thermal resistance of various materials as a function of distance measured from the edge of a circular heat flux into an infinite heatsink. The thermal resistance in the centre of the heath flux is higher by a factor of 1,57.

Of course, the contacting surfaces of heatsink and transistor flange will not remain unaffected by the pressure when the two are clamped together. Where the pressure is greatest the asperities will, naturally, be to some extent crushed, thus increasing the area of metallic contact at these point. It is worth examining how the applied pressure is distributed.

6 PRESSURE DISTRIBUTION

Because the transistor flange is flexible the pressure imparted by the clamping bolts is not distributed uniformly over it. Accurate calculation of the actual pressure distribution is impeded by a number of difficulties:

- The flange is not perfectly flat
- Its shape is irregular
- The modulus of elasticity is higher in the centre of the flange than elsewhere.

In fact about 90% of the clamping force is exerted in an area twice that of the screw head (or washer, if used). Away from this area the force falls rapidly, its approximate value being given by:

$$F = F_i\left(\frac{Ph^3}{L^3} + \frac{K}{L^3}\right)$$

here:

F = pressure

P = the product of modulus of elastically, mass moment of inertia, shape factor and roughness factor

K = waviness factor (which may be negative)

h = height of flange

L = distance from fixing point

F_i = force under bolt head.

Because the denominator includes the third power of the distance, pressure falls off rapidly with distance from the fixing point and may even become negative. This is confirmed by the fact that the centre of a transistor flange lifts away from the heatsink when too high a torque is applied to the bolts. Figure 10 illustrates how pressure is distributed over the flange. In the following we shall see what actual forces are involved.

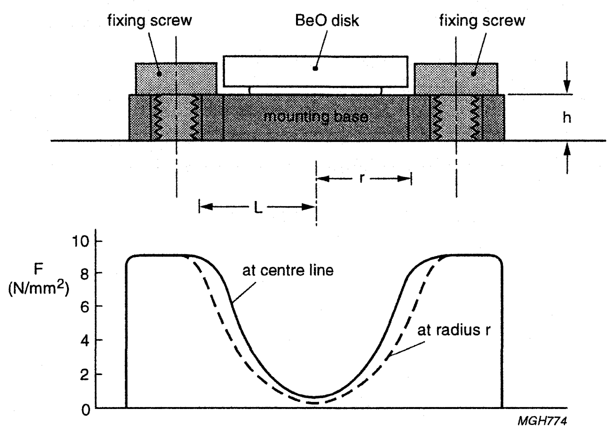


Fig.10 Pressure distribution over the mounting surface of an ideal (flat) flange. The highest pressure occurs round the bolt heads.

7 FORCE UNDER THE BOLT HEAD

The equation for clamping force would be simple were it not for the effect of friction. Friction enters in two ways: friction between bolt head and flange and friction between the external and internal screw threads. The coefficient of friction depends on the two materials in contact and the degree of lubrication. Table 1 shows the coefficient of friction for the materials of interest, the bolts being usually of steel and the heatsink either of copper or aluminium. Sometimes a steel nut is used.

Table 1

MATERIAL	COEFFICIENT OF FRICTION			
	UNLUBRICATED		LUBRICATED	
	MIN.	MAX.	MIN.	MAX.
steel – copper	0,5	0,8	0,2	0,6
steel – aluminium	0,5	1,3	0,2	0,6
steel – steel	0,3	0,7	0,1	0,2

Note: at higher contact pressures the coefficient of friction increases due to atomic adhesion and gouging.

The relation between torque and the force under the bolt head is:

$$F_i = \frac{2T}{D_m f_b + D_p \frac{\tan(B + \varnothing)}{\cos\alpha}}$$

where:

- T = applied torque (0,6 to 0,75 newton metres)
- D_m = mean bearing diameter of bolt (M3 = 4,2 mm; UNC4-40 = 3,9 mm)
- D_p = pitch diameter of thread (M3 = 2,675 mm: UNC4-40 = 2,433 mm)
- B = helix angle of thread (M3 = 3,41°; UNC4-40 = 4,77°)
- f_b = coefficient of friction between bolt head and flange (0,5 – 0,8)
- $\varnothing$ = friction angle ($\varnothing = \tan^{-1} f_t$, where f_t, the coefficient of friction between the screw threads, is 0,3 to 1,3)
- α = half thread profile (30° for both threads).

Table 2 shows the maximum and minimum figures for the two bolts in question and the three materials into which the bolts are screwed. In all cases friction between bolt head and flange is assumed to be steel-to-copper. The minimum values were calculated using minimum torque and maximum coefficient of friction. Estimating probable maximum values is less straightforward. Friction will increase, even from the minimum value, as pressure increases. The chance of some lubricant (in the form of heatsink compound) being present is quite high, even if care is taken. On the basis of experience, we have taken a median value for coefficient of friction to arrive at the maximum force values in Table 2.

Table 2

MATERIAL INTO WHICH BOLT IS SCREWED	FORCE UNDER BOLT HEAD (NEWTONS)			
	M3		UNC4-40	
	MIN.	MAX.	MIN.	MAX.
copper	308	385	322	403
aluminium	308	385	322	403
steel	369	461	394	493

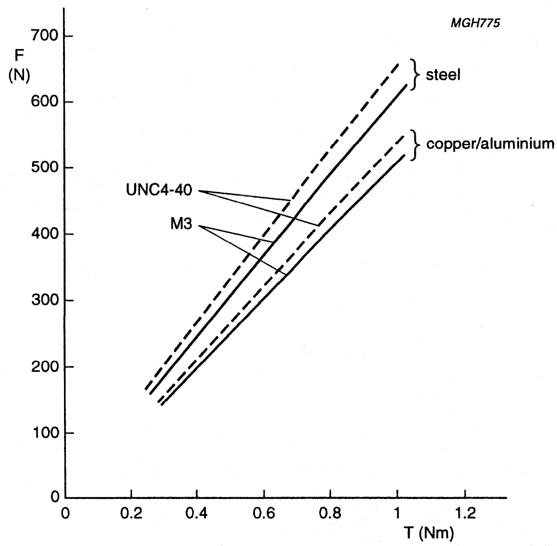


Fig.11 Force under the bolt head as a function of applied torque. Note that the UNC4-40 bolt gives a slightly higher force than the M3.

These results are plotted in Fig.11. The curves are extended to higher torque values to take account of torquing error. Depending on the type of tool used and the speed of operation, the bolts may be over-torqued by a factor of up to 1,6.

It is clear that the UNC4-40 bolt gives a somewhat higher force under the head than the M3. The difference in pressure is even greater because the UNC4-40 bolt head is smaller than the M3.

It should be borne in mind that the relation and curves are only valid up to certain limits. At some point the bolt head starts biting into the material under it and the threads start biting into each other. At the limit either the threads strip or the bolt shears. So, instead of being straight lines the curves will flatten out.

8 MOUNTING PRESSURE

We can derive the actual mounting pressure from the contact area between bolt head and flange.

Bearing area = bolt head area - flange hole area.

Minimum bearing area = minimum head area - maximum hole area.

Maximum bearing area = maximum head area - minimum hole area.

The lowest and highest pressures are then obtained by combining the above results with the force values from Table 2.

$$\text{Minimum pressure} = \frac{\text{minimum force}}{\text{maximum area}}$$

$$\text{Maximum pressure} = \frac{\text{maximum force}}{\text{minimum area}}$$

9 DEFORMATION

Metals, particularly copper which is highly ductile, deform when loaded. Up to a specific stress this deformation is elastic, i.e., remove the load and the metal returns to its original shape. Above this point permanent deformation occurs. Compared with metals such as steel, the elastic limit of copper is quite low; depending on its production history, plastic deformation can begin at stresses of about 20 N/mm^2.

The production history of the flange copper is not published. However it is reasonable to assume that it is cold rolled with some consequent work hardening. Brazing on the BeO disc at a temperature of about 800 °C will cause annealing. Under the disc, however, the differing expansion coefficients of copper and beryllium (18 compared with 5,8) will cause stresses. The copper, being the more ductile of the two, will deform with consequent work hardening around the centre. Machining flat will also cause some work hardening. The result is that the material properties of the flange lie somewhere between those of cold drawn copper and fully annealed copper.

Figure 12 shows the probable stress/strain curve for these conditions. Inserting the stress values obtained in Table 3, we get the expected degree of deformation. The highest stresses occurring with M3 bolts (±35 N/mm^2) are just over the border of elastic deformation (strain not exceeding 0,05%). Even with a factor of 1,6 to allow for over-torquing we are still within safe limits, below, say, 0,08%. With UNC4-40 the stresses are much higher than this and, if an allowance of 1,6 is made for torquing error, strains of up to 1,0% (and not less than 0,04%) are likely. Where possible this should be avoided, if necessary by fitting a 5,5 mm washer under the head.

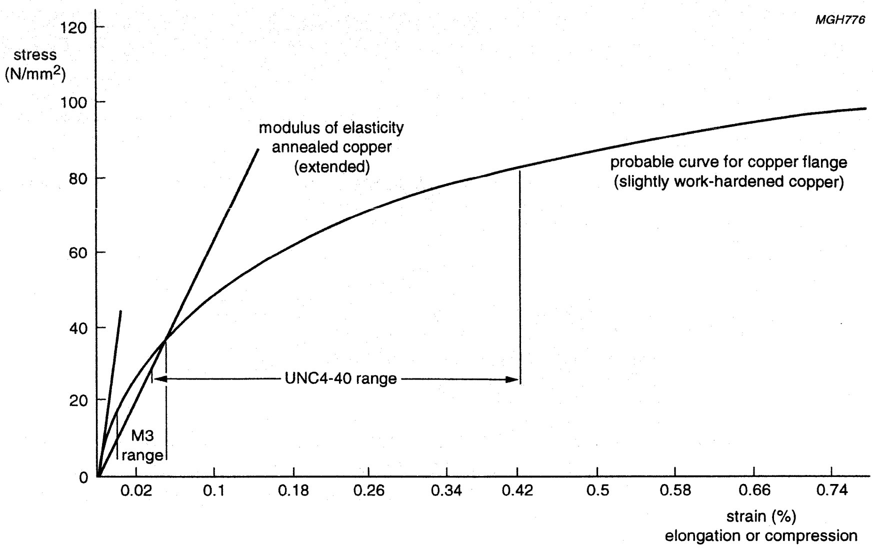


Fig.12 Stress/strain curve for the copper flange. The smaller head diameter of the UNC4-40 bolt leads to much higher strains than with the M3. When maximum torque is applied a washer will reduce strain to an acceptable level.

Table 3 Pressure in newtons/mm^2; note 1

MATERIAL	M3		UNC4-40	
	MIN.	**MAX.**	**MIN.**	**MAX.**
copper	18	29	30	68
aluminium	18	28	30	68
steel	22	35	36	83

Note

1. 1 newton/mm^2 = 1 MPa.

10 EFFECTS OF DEFORMATION

Because the copper flange is compressed between bolt head and heatsink, displaced metal can only escape radially. Some will escape toward the centre, but most will flow outward. Along the axis between the bolts two stresses will be operating from opposite directions. The metal can only escape by lifting the centre of the transistor flange away from the heatsink, as shown in Fig.13.

Figure 14 shows the result of tests in which a flange was mounted by high tensile steel M3 bolts to a thick tool-steel heatsink with polished surface. The M3 bolts were screwed into steel nuts, a friction coefficient of about 0,3 being applicable. The torque on the bolts was increased in steps of 0,2 Nm from an initial 0,4 Nm. After each step the flatness was measured along the dotted line. The enlarged curve for a torque of 0,8 Nm shows that the centre of the flange has lifted by 7 μm. This lifting will increase contact thermal resistance and as, in any case, normal heatsink are not perfectly flat, it is clear that torques of 0,75 Nm should not be exceeded. It is worth nothing that even though the tests extended to torques as high as 2,0 Nm, in no case was a beryllium oxide disc damaged.

Among the conclusions to be drawn from the above are that high torques do not improve contact thermal conductivity and that once a transistor has been mounted it should never be removed to another heatsink. For one thing it has adapted to the footprint of the heatsink it was first mounted on, and further, because of tolerances, the pitch of the mounting hole threads will differ.

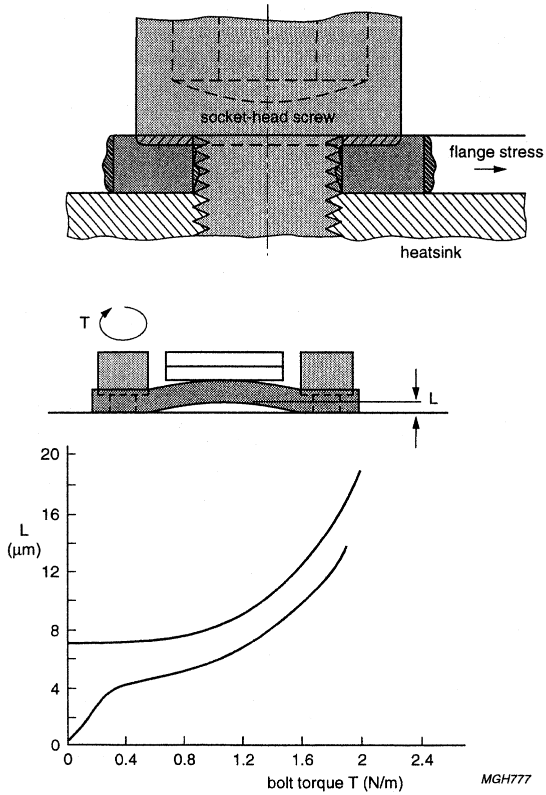


Fig.13 Above, plastic deformation in the flange. Below, how the centre of the flange tends to lift under excessive pressure.

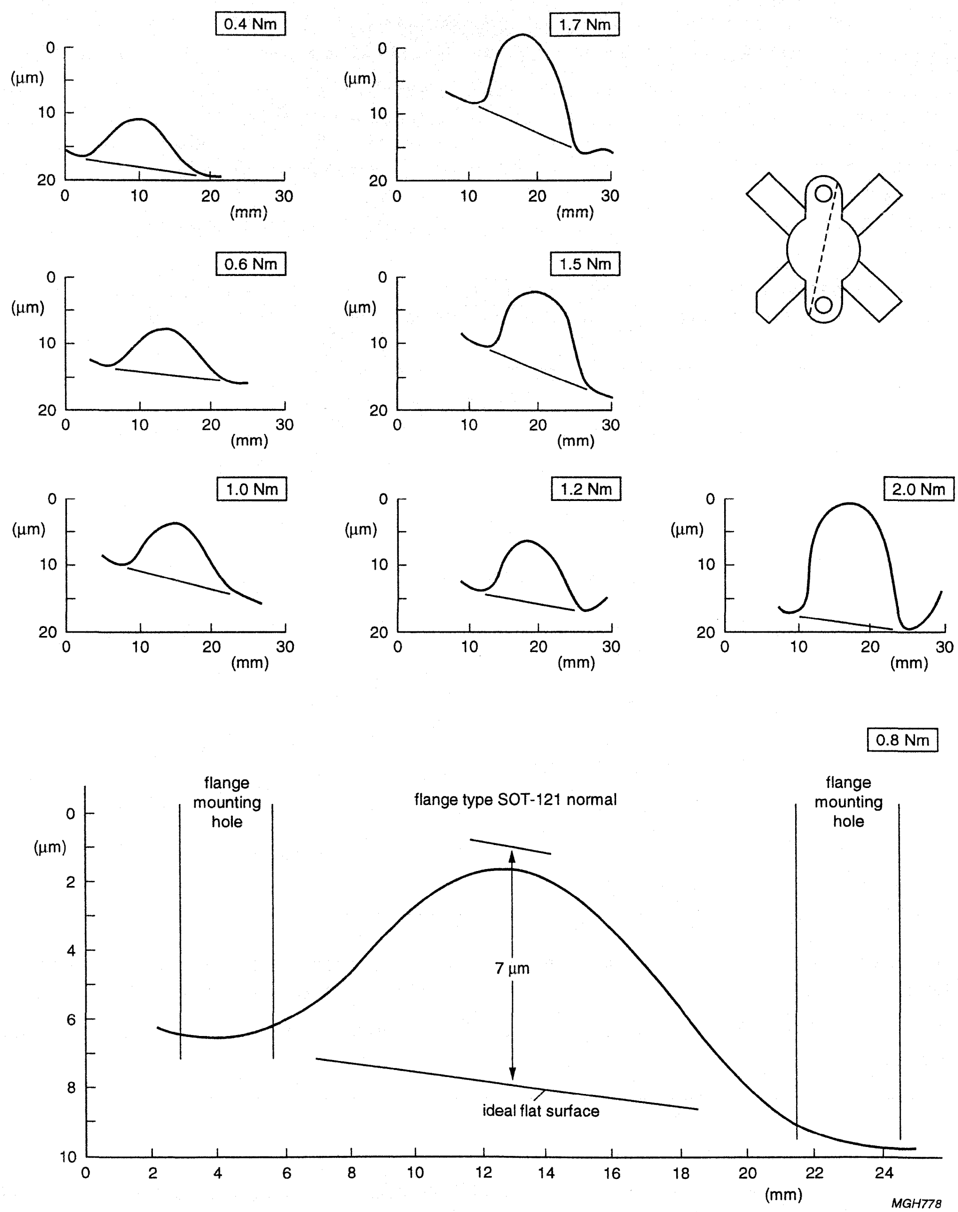


Fig.14 Measured deformation in an unlapped flange when steel M3 bolts are torqued in steps to 2,0 Nm. The curves have been smoothed to remove the effects of micro-asperities. The enlarged curve is for a torque of 0,8 Nm and shows a deformation of 7 µm at the centre.

11 CREEP

The deformation just described occurs immediately the stress is applied; under continued stress there is a further slow deformation that tends to reduce the applied stress. This slow deformation is known as creep.

Creep causes plastic strain to increase with time and, because the strain in a mounted transistor flange is constant, elastic strain decreases. Stress decreases as the elastic strain decreases. Figure 15 shows how stress reduces over time. It is, however, no more than an indication because relaxation speed is highly dependent on temperature, cyclic strain, work hardening and recrystallization. Under normal operating conditions temperature cycling will cause work hardening which will promote resistance to stress relaxation. On the other hand the cyclic strain imposed by temperature variations and the (more or less) elevated temperature of the flange during operation will tend to increase stress relaxation.

Our experience in temperature cycling (thermal fatigue) tests shows that relaxation reaches 30% in the first 100 hr and 50% in the first thousand. These tests are, of course, severer than normal operating conditions.

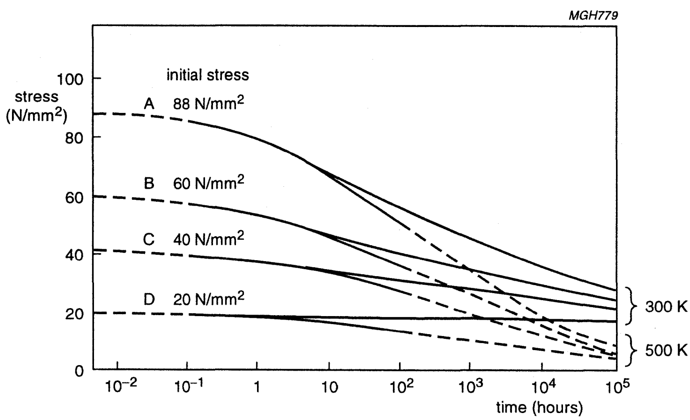


Fig.15 Typical creep curves in oxygen-free high conductivity copper. These are representative for the transistor flange copper but can only be considered as indicative because creep is also influenced by cyclic strains (temperature) such as occur in an operating transistor.

12 APPENDIX

12.1 Cavity test

The transistors were mounted on a water-cooled copper rod (30 mm dia.), the centre of the upper surface of which was maintained at 70°C. The upper surface was lapped to a flatness of <3 μm and a roughness r_a < 0,4 μm. The flange of one transistor was lapped to a flatness of <1 μm and a roughness r_a < 0,2 μm. The other transistor was not lapped and its flatness was 6 μm and its roughness r_a < 0,8 μm.

Dow Corning DC340 heatsink compound was used, except in one case where is was omitted to prove its efficacy. The transistors were adjusted to dissipate 150 W.

A circular cavity 1 mm deep was miled in the centre of the base of the flange. Initially it was 4 mm diameter and was increased in steps of 1 mm, burrs being removed at every stage. The percentage non-contacting surface area as a function of cavity diameter is shown in Fig.16. The amount of metal removed (1 mm depth) was insufficient to affect the bulk thermal properties of the flange.

Crystal temperatures were measured with a specially calibrated infra-red microscope. Heatsink and flange temperatures were measured with thermocouples places as in Fig.17. Thermocouple 1 was used as monitor and maintained at 70 °C.

Crystal temperatures were plotted, a typical scan being shown in Fig.18 (left), and average peak temperatures entered on thermal maps as in Fig.18 (right). Finally, curves were plotted of peak average temperatures at given points on the crystal against cavity size. The highest and lowest curves are those shown in Fig.19. Intervening curves have been omitted for clarity.

It will be seen that at a cavity of 7 mm, junction temperature has risen by less than 10 K and that it is not until the cavity is 9 mm or more that maximum junction temperature is exceeded. Clearly, lapping the transistor flange does reduce $R_{th\ mb\text{-}hs}$, but using heatsink compound has an even greater effect.

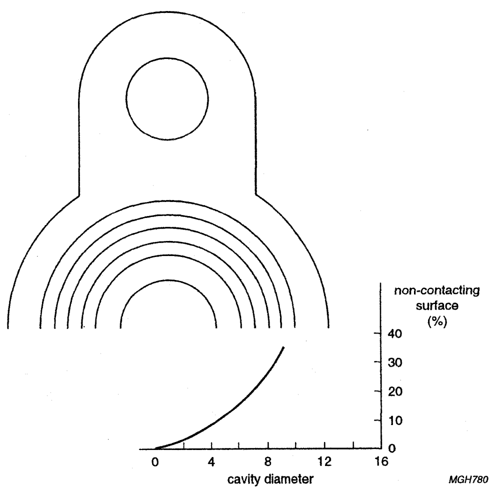


Fig.16 Contact surface area as a function of cavity size.

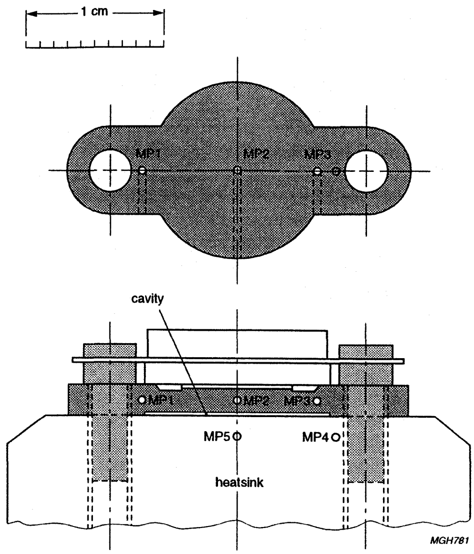


Fig.17 Placement of thermocouples for monitoring heatsink temperature.

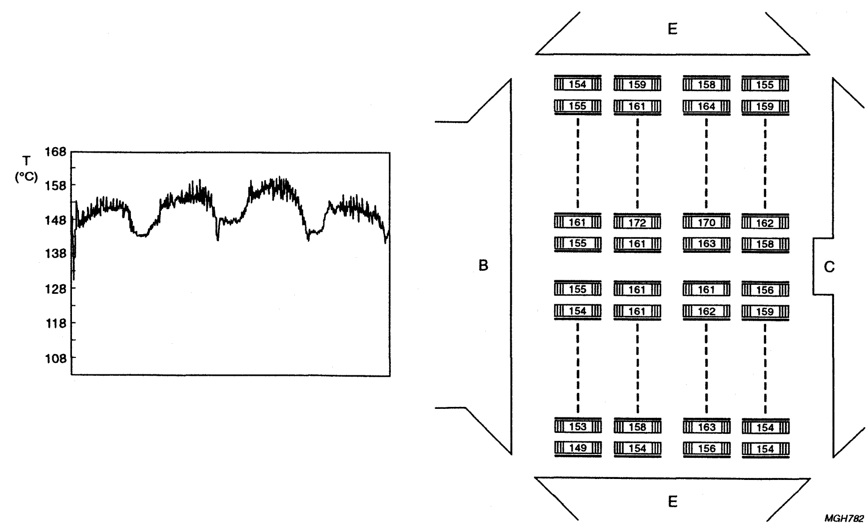


Fig.18 Junction temperature measurements. Left, a typical scan with the infrared microscope and right, a partial thermal map of average peak temperatures.

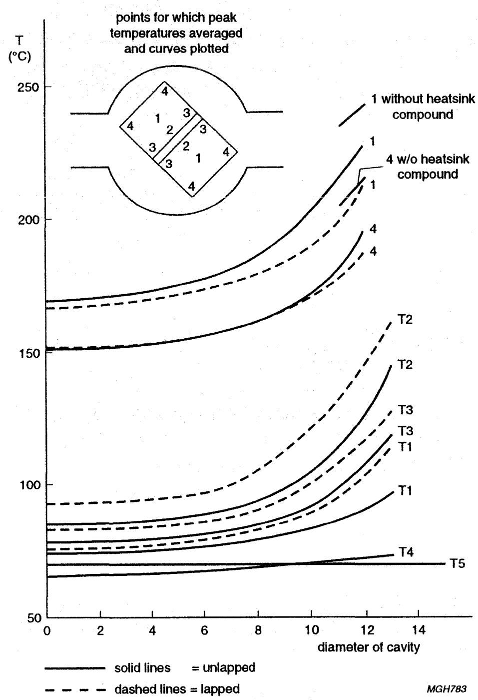


Fig.19 Curves of junction temperature against cavity size for a lapped transistor (solid line) and an unlapped transistor (broken line). It is not until the cavity is about 7 mm in diameter that junction temperature rises more than about 10 K.

1 INTRODUCTION

For both 820 – 960 MHz (GSM) and 1800 – 1990 MHz (PCN and PCS), Philips has introduced a series of RF power transistors for base station applications at 26 V power supply. The driver stage transistors are mounted in a SO-8 style surface mount package (SOT409B), suitable for pick and place assembly. SOT409B packages have an AlN substrate to electrically isolate the flange from the leads. Table 1 summarizes the RF performance and thermal resistances of the transistors.

Table 1 SOT409B driver stage transistors with typical values between brackets

TRANSISTOR TYPE	f (MHz)	PL-1 dB (W)	Gp (dB)	Eff (%)	R_{thj-mb} (K/W)	P_{dmax} (W)
BLV904	960	5	>13 (15.5)	>50 (55)	10	17
BLV909	960	9	>9.5 (11.5)	>50 (55)	6	29
BLV2042	1990	4	>11 (13)	>40 (45)	10	17

In this paper the mounting of the SOT409B devices is considered. By focusing on the heatflow from junction (at die level) to the heatsink of the application, criteria for best thermal performance (lowest thermal resistance between mounting base and heatsink), can be derived. Simulation results are presented to show the behaviour of using different ways of mounting the device, resulting in a proposal for surface mounted assembly.

2 MOUNTING OF SOT409B DEVICES

Thermal investigations has shown that both the copper pad of the device's backside (connected to the AlN substrate) as well as the leads of the SOT409B, contribute to the heat transfer from junction to heat-sink. For the most optimal results two options are available:

The most effective way to thermally connect the SOT409B devices, is to directly solder the device's backside, together with the device's emitter leads (4 are available, at the edges; see Fig.1) to the heatsink or to an insert mounted to the heatsink; see Fig.2. A more practical option is a footprint on the P.C.B. with a number of through metallized holes to transfer the heat. In that case the device's copper pad is soldered to a footprint, of at least the same dimensions as the device (see Fig.3). Connection to the fully metallized backside of the P.C.B. is achieved by placing a sufficient number of plated through metallized holes just under the device:

- To achieve good grounding for best R.F. performance
- To optimize the heat transfer.

To optimize the thermal contact between the board and the heatsink a thin coating of thermal past should be applied locally to minimize voids. Further that P.C.B. should be fastened to the heatsink with extra screws as close as possible to the device. Another possibility is to solder the P.C.B. to the heatsink or use thermal conductive glue.

Pinning SOT409B

PIN	DESCRIPTION
1	emitter
2	base
3	base
4	emitter
5	emitter
6	collector
7	collector
8	emitter

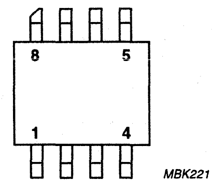


Fig.1 SOT409B outline.

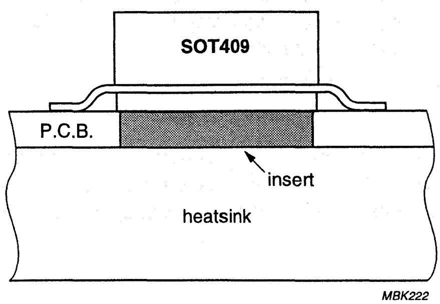


Fig.2 Cross section of the SOT409B mounted on an insert.

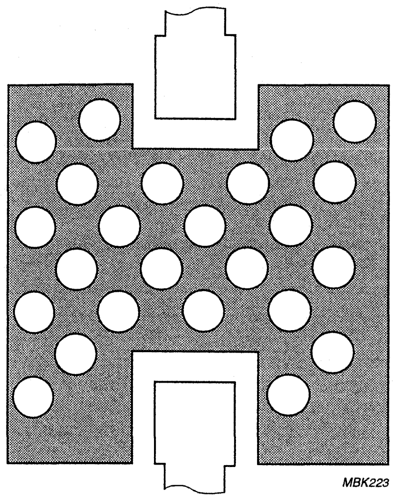


Fig.3 Example of a footprint for soldering.

3 HEATFLOW IN APPLICATION

In Fig.4 a cross section and a schematical representation is given of an application in which a mounted SOT409B device is used. The device has been mounted on top of a P.C.B. equipped with through metallized holes to transfer the heat from the device to the base to heatsink. This figure is used to determine the thermal resistance of the P.C.B.

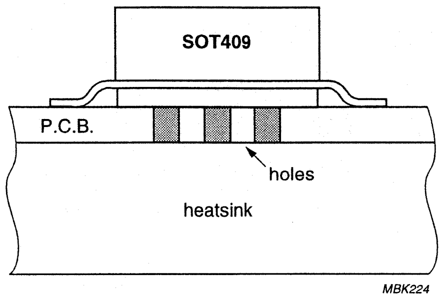


Fig.4 Cross section to the SOT404 mounted on the footprint.

4 IMPORTANT FACTORS FOR THERMAL RESISTANCE OF THE P.C.B.

- Thickness of P.C.B. material
- Thickness of metallization of P.C.B.
- Copper growth in holes (depending on process used)
- Fill factor (percentage of solder present in through plated holes)
- Number of plated through holes
- Diameter of plated through holes.

Other parameters were taken into consideration, but have marginal effects on thermal resistance:

- P.C.B. material used (Duroid, epoxy)
- Pb percentage in PbSn.

5 SIMULATION EXAMPLES

With the help of simulations, each of the critical factors have been investigated. For calculations, the following parameters have been used.

- Heat area dimensions: 4.13 × 3.18 mm
- PbSn thickness on top of P.C.B. metallization (24 μm)
- Pb % in PbSn (37%)
- Cu growth in via holes (32 μm)
- P.C.B. material (Duroid)
- P.C.B. copper thickness (1 Oz. or 35 μm).

The result on thermal resistance is given in Table 2 and 3, for 9 and 12 through metallized holes respectively:

Table 2 Footprint area equipped with 9 through metallized holes

CASE	FILL FACTOR (%)	HOLES DIAMETER (mm)	P.C.B. THICKNESS (mm)	Rth mb-hs (K/W)
1	10	0.65	0.79	5.4
2	100	0.65	0.79	3.4
3	100	0.65	1.59	5.7
4	100	1.00	1.59	2.9
5	100	1.00	0.79	1.7

Table 3 Footprint area equipped with 12 through metallized holes

CASE	FILL FACTOR (%)	HOLES DIAMETER (mm)	P.C.B. THICKNESS (mm)	Rth mb-hs (K/W)
1	10	0.65	0.79	–
2	100	0.65	0.79	2.5
3	100	0.65	1.59	4.3
4	100	1.00	1.59	–
5	100	1.00	0.79	1.3

6 CONCLUSION

Using the material and permanent values given in the example, thermal resistance of the footprint design can be as low as 1.5 K/W for the optimum case. Even the most powerful transistor available in the SOT409B range, BLV909 (nominal 9 W of RF power at 960 MHz) can be operated with a sufficiently low junction temperature (T_j). A T_j of 137 °C is possible while heatsink temperature (T_h) is assumed to be 70 °C and 50% collector efficiency is achieved at nominal loadpower.

7 REMARK

SOT409B is a SMD package which can withstand a normal reflow soldering process. Since the leads are plated with typically 3 μm of gold, either sufficient solder material (≈150 μm) should be applied or the leads should be pre-tinned in order to minimize brittle Au-Sn intermettalics which can introduce cracks during power cycling. A footprint for reflow soldering is available upon request.

0. Contents

1. Introduction

The data of circulators and isolators given in the data sheets or other publications assume, that all ports of the device are matched with the nominal impedances of the lines. When measuring the devices or in the application these impedances will deviate from the ideal matching, often very drastically. Therefore we will investigate what happens when we use not ideal loads and equipment to measure circulators and isolators, and how these devices behave in the practical environment.

2. Measuring circulator data

2.1 Isolation

When measuring the isolation of a 3-port-circulator we connect one port with the source, on the next port in the sense of circulation we put a matched load, and the third port is connected to a detecting device (Figure 1). This technique can be done with low signal level but also with high power. For

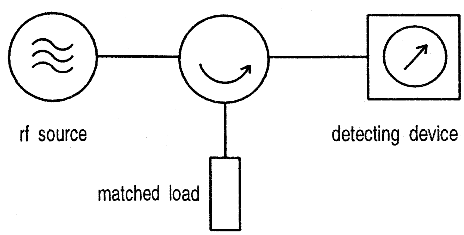


Fig.1: Measurement of isolation

low level measurements we can use also a network analyzer, connecting two ports to it and the remaining port gets a matched load.

The "matched load" used for terminating one port is not an ideal matching but has a small vswr s_{load}. This small reflection superimposes the signal caused by the not ideal isolation of the circulator. Therefore we measure a combination of the circulator isolation and the vswr of the connected load, the value of which depends on the phase between the two signals. The minimum value of isolation is measured when both signals add, the maximum when the signals subtract one from the other.

For the calculation we convert the isolation of the circulator D into an equivalent vswr s_D. Then we combine the vswr of the load s_{load} and s_D to the maximum and minimum vswr of both ($s_{meas\ max}$ and $s_{meas\ min}$) and convert these back to the extremes of the measured isolation $D_{meas\ max}$ and $D_{meas\ min}$:

$$s_D = \frac{1 + \frac{1}{10^{\frac{D}{20}}}}{1 - \frac{1}{10^{\frac{D}{20}}}}$$

$$s_{meas\ \mathrm{min}} = s_D \times s_{load}$$

$$s_{meas\ \mathrm{max}} = s_D \,/\, s_{load} \qquad if\ s_D \,/\, s_{load} \geq 1$$

$$s_{meas\ \mathrm{max}} = s_{load} \,/\, s_D \qquad if\ s_D \,/\, s_{load} < 1$$

$$D_{meas\ \mathrm{max,min}} = 20\ lg\frac{s_{meas\ \mathrm{max,min}} + 1}{s_{meas\ \mathrm{max,min}} - 1}$$

These correlations between maximum and minimum measured isolation D_{meas}, the real isolation of the circulator D, and the vswr of the load s_{load} can be seen as a graph in figure 2. The measured isolation will lie between the upper and lower curve of the relevant load vswr.

If for example we use a load with a vswr of s_{load}=1,02 and the isolation of our circulator is 25 dB, our measurement can lie between 23,6 and 27,6 dB.

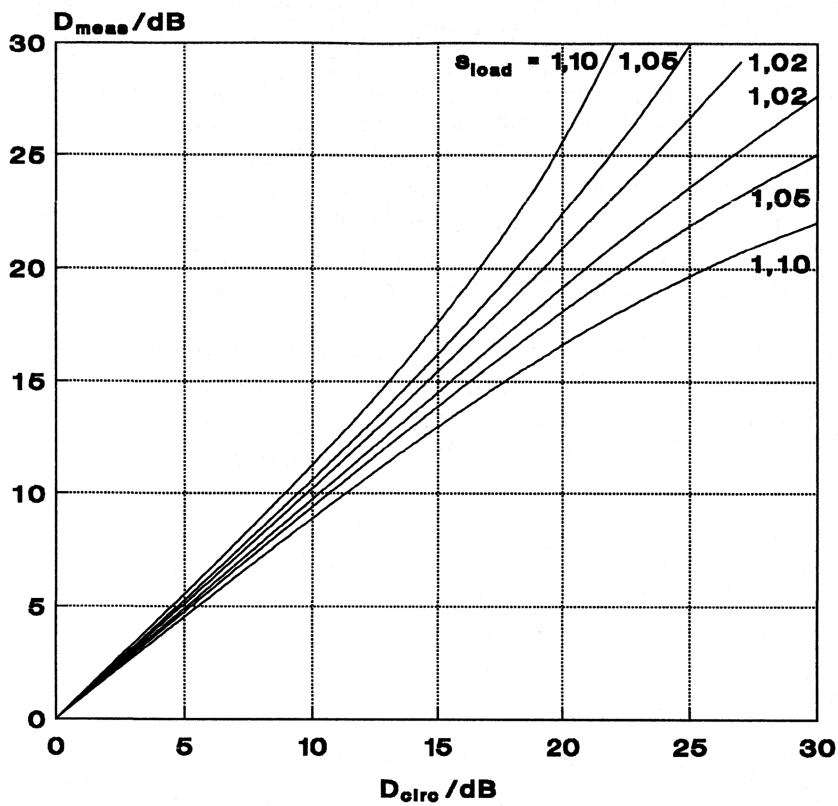


Fig.2: Measured maximum and minimum isolation as a function of the isolation of the circulator D_{circ} with the load vswr s_{load} as a parameter

To give a better idea how big the difference between the real isolation of the circulator and the measured isolation can be, figure 3 shows this difference as a function of the isolation of the circulator D_{circ} with the vswr of the load s_{load} as a parameter.

For example for a load with a vswr of s_{load}=1,05 and an isolation of the circulator of 20 dB the maximum difference of the measured isolation and the real isolation of the circulator is +2,4 dB and -1,9 dB.

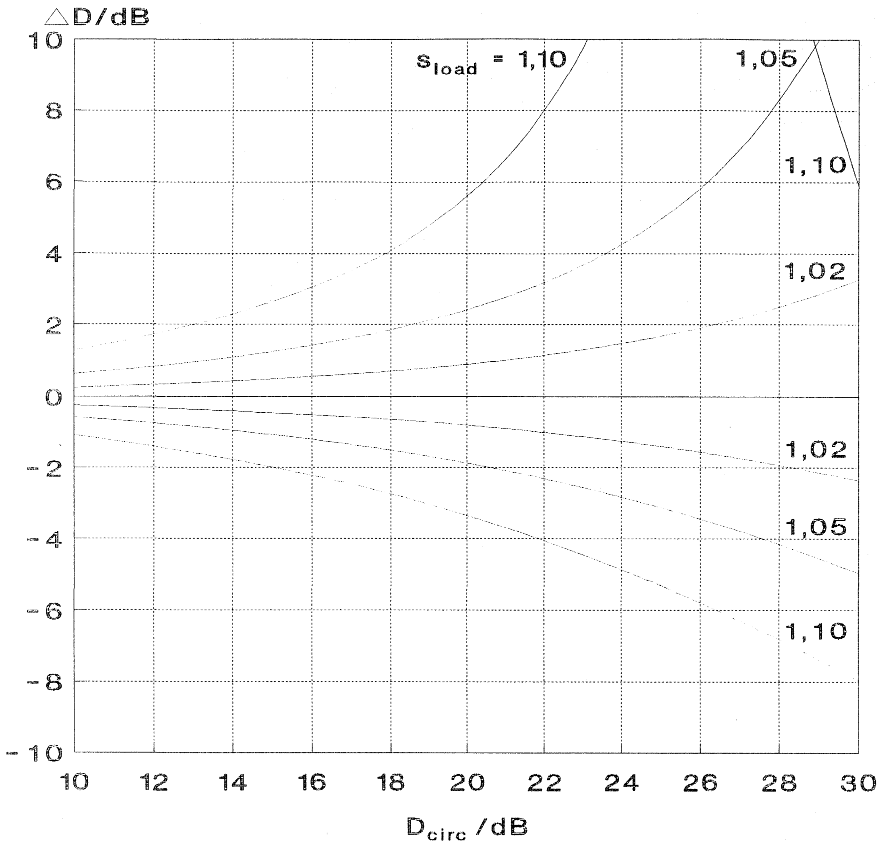


Fig.3: Maximum difference between the isolation of the circulator and the measured isolation as a function of the isolation of the circulator D_{circ} with the load vswr s_{load} as a parameter

2.2 Input reflection

The input reflection of the ports of a circulator is often measured by directional couplers. For low level measurements network analyzers, bridges, and slotted lines can be used too. On the ports not being measured we put matched loads, and the port being measured is connected to the directional coupler, bridge, slotted line or network analyzer. If the loads used have an input vswr lower than 1,1 we can neglect their influence on the measurement of the input reflection.

When using a directional coupler or bridge the main source of failures in this measurement is the directivity D_R of the directional coupler or bridge measured in dB. The signal resulting from the directivity combines with the signal returning from the circulator and we measure a vswr which lies between a maximum value $s_{meas\ max}$ when both signals add and a minimum value $s_{meas\ min}$ when the signals subtract one from the other. We can calculate these limits in the following way.

We transform the directivity D_R into the equivalent vswr s_D

$$s_D = \frac{1 + \dfrac{1}{10^{\frac{D_R}{20}}}}{1 - \dfrac{1}{10^{\frac{D_R}{20}}}}$$

and now we combine s_D with the vswr of the circulator port s to the extremes $s_{meas\ max}$ and $s_{meas\ min}$

$$s_{meas\ \max} = s_D \times s$$

$$s_{meas\ \min} = s_D / s \quad if \quad s_D / s \geq 1$$

$$s_{meas\ \min} = s / s_D \quad if \quad s_D / s < 1$$

This relationship is given in figure 4. In this diagram we can see, that a circulator with an input vswr of 1,25 will show figures between 1,22 and 1,28 if measured with a directional coupler or bridge having a directivity of 40 dB.

When using a slotted line the residual vswr of this line corresponds to the directivity of the bridge or directional coupler. If we transform the residual vswr s_D to the directivity

$$D_R = 20\ lg\frac{s_D + 1}{s_D - 1}$$

then we can use figure 4 for estimating the maximum failure.

When measuring the input reflection with modern network analyzers, the analyzer corrects the failure during calibration with the calibration kit. If there is no calibration kit for the line used and we have to use additional transitions, this results in measurement uncertainties.

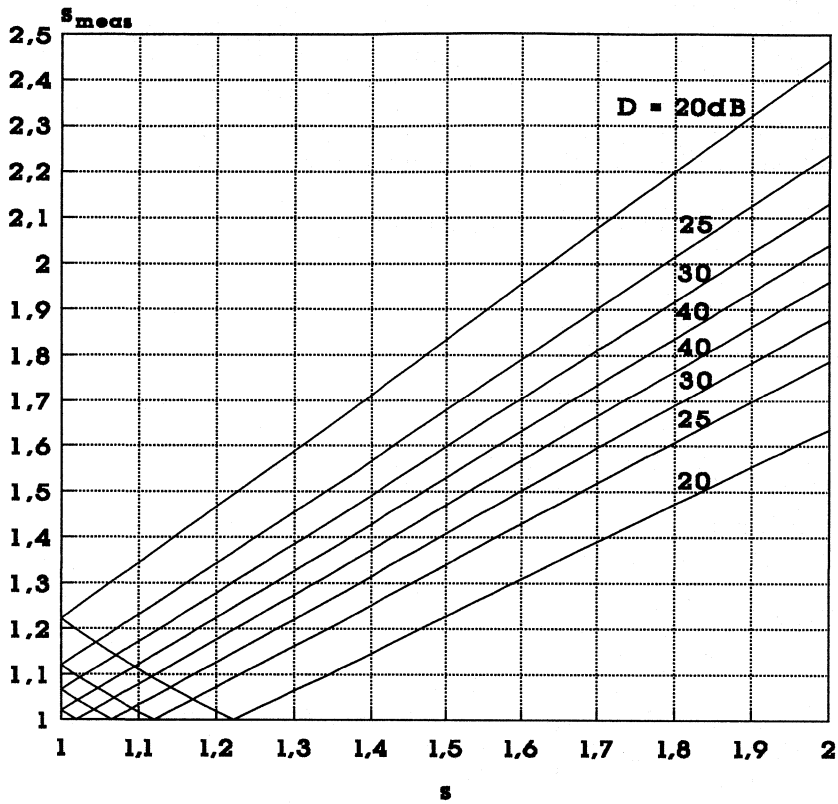


Fig.4: Measured maximum and minimum input vswr s_{meas} as a function of the input vswr of the circulator s with the directivity D of the directional coupler or bridge as a parameter

Up till now we assumed that we have a pure signal. If there are harmonics on our signal, which happens very often when measuring with power, we can get big failures. A normal circulator or isolator represents a more or less good match in its operating band, but reflects nearly all harmonics or other spurious frequencies far outside the operating band. Therefore these frequencies have to be removed by suitable filters.

To estimate the failures, which may happen, we can calculate in the following way.

If we have a harmonic x dB under our signal level and we measure with a power measuring device (e.g. a thermistor or baretter, or a diode in the square-law-region), the harmonic power adds to the reflected power of the career:

reflected power of the career

$$P_r = P \times \left(\frac{s-1}{s+1}\right)^2$$

harmonic power, totally reflected

$$P_h = P \times 10^{-\frac{x}{10}}$$

$$s_{meas} = \frac{1+\sqrt{P_r+P_h}}{1-\sqrt{P_r+P_h}}$$

In figure 5 we see, that with a harmonic content of -20 dBc we will measure the vswr of a circulator to s_{meas}=1,31 instead of its real value of s_{circ}=1,20.
If we measure with an amplitude measuring device (e.g. a diode in the linear region) we have to calculate the areas between the time axis and the curve resulting from the reflected original signal and the totally reflected harmonics. We get the biggest deviation for the third harmonic, which is one of the most important too.
For small vswr's of the circulator the resulting curve cuts the time axis more often than for a normal sine wave, and we have to integrate the parts. There are two extremes for the phase of signal and harmonic: they are in phase or in antiphase.
With

$$r_{circ} = \frac{s_{circ} - 1}{s_{circ} + 1}$$

$$a_3 = 10^{-\frac{x}{20}}$$

we get the following equations for a third harmonic of x dBc:

a. time axis cut also within a half sine wave of the signal

$$\omega t_1 = \arcsin\sqrt{\frac{3}{4} \pm \frac{r_{circ}}{4a_3}}$$

$$r_{meas} = \left|r_{circ}(1 - \cos\omega t_1) \pm \frac{a_3}{3}(1 - \cos 3\omega t_1\right| +$$

$$+\left|r_{circ}\cos\omega t_1 \pm \frac{a_3}{3}\cos 3\omega t_1\right|$$

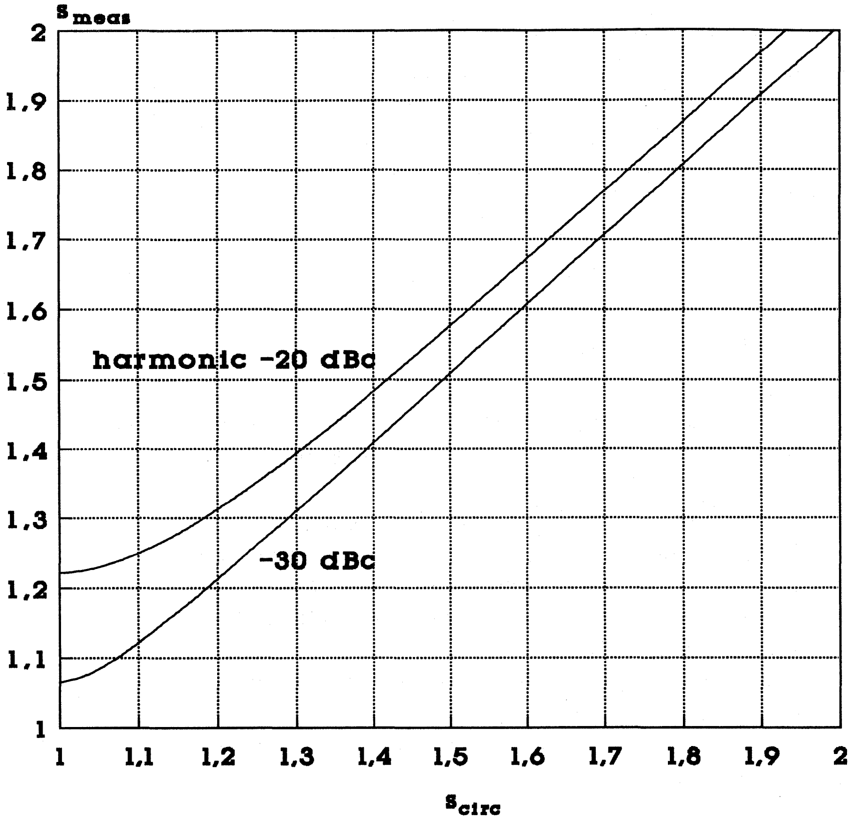


Fig.5: Measured input vswr s_{meas}, using a power measuring device, as a function of the vswr of the circulator s_{circ}, with the harmonic level as a parameter

b. time axis not cut within the half sine wave of the signal

$$r_{meas} = r_{circ} \pm \frac{a_3}{3}$$

and

$$s_{meas} = \frac{1 + r_{meas}}{1 - r_{meas}}$$

This relationship is given in the figures 6.

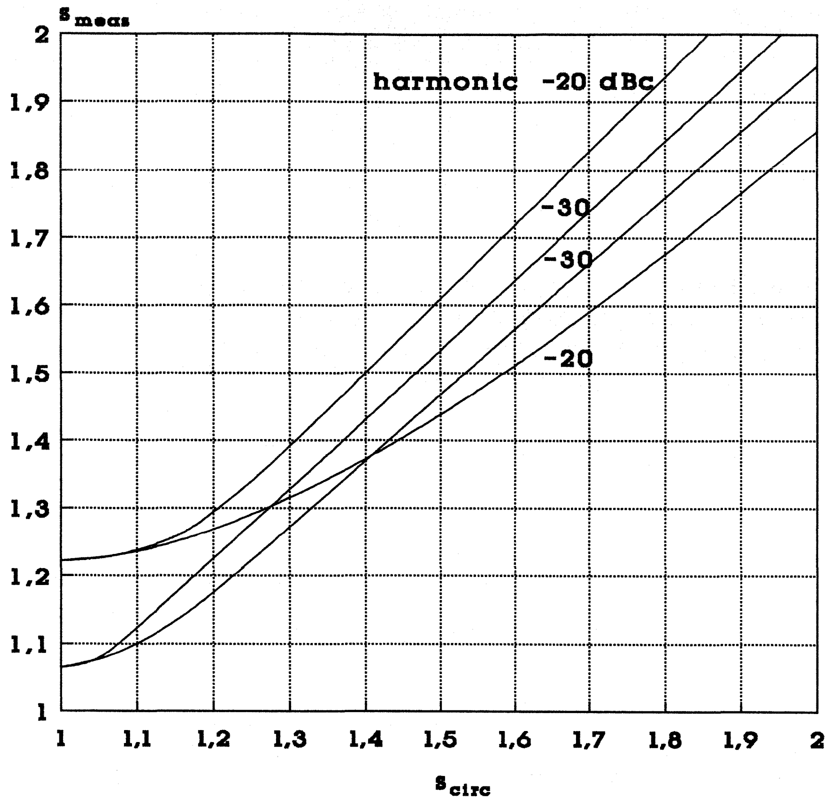


Fig.6: Measured maximum and minimum input vswr s_{meas}, using an amplitude measuring device, as a function of the vswr of the circulator s_{circ}, with the third harmonic level as a parameter

For a circulator with a vswr s_{circ}=1,20 and a third harmonic of -20 dBc the reading of an amplitude measuring device may lie between s_{meas}=1,31 and s_{meas}=1,27.

2.3 Insertion loss

At high power level the insertion loss of a circulator will be measured between isolators and directional couplers, similar to the measurement of the isolation, but with the circulator put in the forward direction, see figure 7. The value to be measured is very small, therefore we have to look for some sources of failure which could be neglected when we measured the isolation. On the other hand the loads on the ports not used in this measurement do not influence the result as long as they have a vswr lower than 1,1.

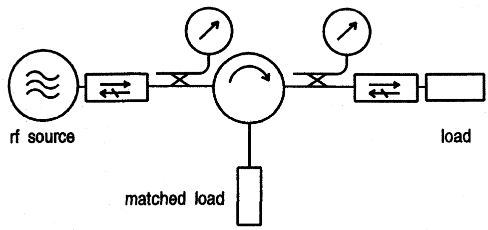


Fig.7: Measurement of the insertion loss

With s_i, the vswr of the isolators used, and s, the vswr of the circulator to be measured, we get a maximum reading of the input power $P_{in\ max}$ which deviates from the power of the generator due to the reflected waves

$$P_{in\ max} = P\left(\frac{1}{1-rr_i}\right)^2$$

with

$$r = \frac{s-1}{s+1} \qquad r_i = \frac{s_i-1}{s_i+1}$$

and a minimum reading

$$P_{in\ min} = P\left(\frac{1-2rr_i}{1-rr_i}\right)^2$$

For this calculation we assume that the vswr of the directional couplers is very low compared to the other reflections and can be neglected. For the output power we have a maximum reading with d, the real insertion loss of the circulator

$$P_{out\ max} = P\left(\frac{1}{1-rr_i}\right)^2 10^{-\frac{d}{10}}\left(\frac{1}{1-rr_i}\right)^2$$

$$= P \times 10^{-\frac{d}{10}} \times \left(\frac{1}{1-rr_i}\right)^4$$

and a minimum reading

$$P_{out\ min} = P\left(\frac{1 - 2rr_i}{1 - rr_i}\right)^2 10^{-\frac{d}{10}} \left(\frac{1 - 2rr_i}{1 - rr_i}\right)^2$$

$$= P \times 10^{-\frac{d}{10}} \times \left(\frac{1 - 2rr_i}{1 - rr_i}\right)^4$$

The measured insertion loss lies now between

$$d_{meas\ max} = \frac{P_{in\ max}}{P_{out\ min}} = d + 20\ lg\ \frac{1 - rr_i}{(1 - 2rr_i)^2}$$

$$d_{meas\ min} = \frac{P_{in\ min}}{P_{out\ max}} = d + 20\ lg\ [(1 - rr_i)(1 - 2rr_i)]$$

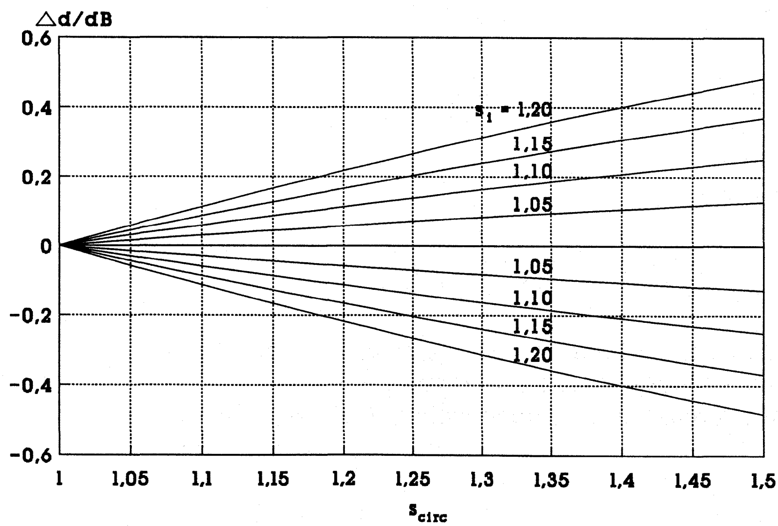


Fig.8: Max. diff. between the insertion loss of the circ. and the measured insertion loss as a function of the vswr of the circ. s_{circ} with the vswr s_i of the isolator of the measurement setup as a parameter

For small values of r and r_i we get the following deviation from the real value of the insertion loss

$$\Delta d_{meas} = 20\ lg\ (1 \pm 3rr_i)$$

The exact values of the deviation are presented in figure 8. It shows, that the measured insertion loss of a circulator with a vswr of s=1,25 measured between isolators with a vswr of s_i=1,10 may deviate from the real value by ±0,14 dB.
The same measurement setup can be used also at low power levels. Here we can use attenuators instead of isolators too.
But we can use also network analyzers. If we calibrate the network analyzer with the simple through calibration, then we get the same failures as discussed, taking s_i as the vswr of the ports. But using the 2-port-calibration the failure is reduced drastically by calculations.

There is also another method some times used, given in figure 9. It is very inaccurate and therefore not recommended. Here the measurement is done by connecting at first the signal source, which is decoupled by an isolator, directly to the detecting device, which is also decoupled by an isolator.

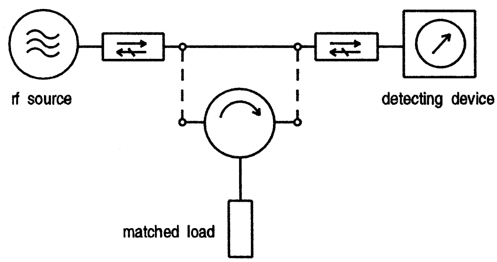


Fig.9: Another measurement setup for the insertion loss

For small signal measurements we can use attenuators instead of the isolators. Then the circulator to be measured is inserted. If the isolation of the isolators is higher than 20 dB or the attenuation of the attenuators is higher than 10 dB, the main sources of failure in the measurement of the insertion loss are the input and output reflections of the isolators or attenuators and the circulator being measured. During calibration the detected signal will lie between a maximum value $A(1+r_i)$ and a minimum value $A(1-r_i)$ caused by the vswr of the isolators or attenuators s_i, which multiply in the worst case.

$$r_i = \frac{s_i^2 - 1}{s_i^2 + 1}$$

If we now put the circulator with its vswr s in, then we get a maximum reading $A_1(1+r)$ and a minimum reading $A_1(1-r)$ with

$$r = 2\,\frac{ss_i - 1}{ss_i + 1}$$

The measured insertion loss lies now between

$$d_{meas\ \max} = 20\ lg\frac{A\ (1 + r_i)}{A_1\ (1 - r)} = d + 20\ lg\frac{1 + r_i}{1 - r}$$

and

$$d_{meas\ \min} = 20\ lg\frac{A\ (1 - r_i)}{A_i\ (1 + r)} = d + 20\ lg\frac{1 - r_i}{1 + r}$$

with d the real insertion loss of the circulator, or given as the deviation from the real value

$$\Delta d_{\max} = 20\ lg\frac{1 + r_i}{1 - r}$$

$$\Delta d_{\min} = 20\ lg\frac{1 - r_i}{1 + r}$$

and as an approximation for small values of r_i and r

$$\Delta d_{\max,\ \min} = 20\ lg[1 \pm (r_i + r)]$$

When measuring in this setup the measured insertion loss of a circulator with a vswr of s=1,20 measured between attenuators or isolators with a vswr of s_i=1,05 may deviate from the real value by +2,7 dB and -2,2 dB.

Also the measurement of the insertion loss is influenced by harmonics and other spurious signals for the same reason as under 2.2, and we have to remove them by filters.

3. Some applications

3.1 Reduction of the vswr or return loss of a load by using an isolator

Often the vswr of a load is high and fluctuating. For example the vswr of a gas filled chamber is very high, but after ignition this gas forms a plasma with high absorption. Or when curing rubber the impedance of the rubber changes with the progress of the process. Or the impedance of an antenna changes with obstacles in its neighbourhood.

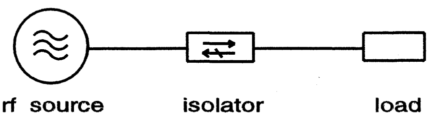


Fig.10: Reduction of the input vswr of a load by using an isolator

To reduce this vswr we can use isolators.
The resulting input vswr of the cascade load and isolator depends on the load vswr, the isolation of the isolator, the vswr of the isolator, and the phase between load and isolator. For the calculation of the resulting input vswr we use the signal flow diagram of a circulator as given in figure 11.

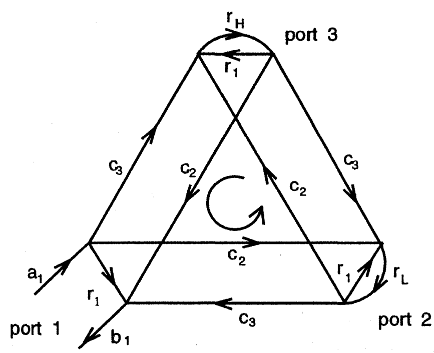


Fig.11: Signal flow diagram of a circulator

- port 1 — the input port, connected to the generator
- port 2 — the output port, connected to the fluctuating load with the reflection coefficient r_L
- port 3 — the internal port when using a circulator as an isolator, terminated with a matched load with the reflection coefficient r_H
- c_2 — the insertion loss of the circulator, given as a vector, $|c_2| = 10^{-d/20}$ with d = insertion loss in dB
- c_3 — the isolation of the circulator, given as a vector, $|c_3| = 10^{-D/20}$ with D = isolation in dB

Using the rules of the signal flow diagram, we get the reflection coefficient r at the input of the circulator

$$r = \frac{b_1}{a_1} =$$

$$= \frac{r_1(1 - r_1 r_H - r_1 r_L - c_2 c_3 r_L r_H + r_1^2 r_H r_L) + c_2 c_3 r_L (1 - r_1 r_H) + c_2 c_3 r_H (1 - r_1 r_L) + c_2^3 r_H r_L + c_3^3 r_H r_L}{1 - r_1 r_H - r_1 r_L - c_2 c_3 r_H r_L + r_1^2 r_H r_L}$$

This expression looks very complicated, but it simplifies, if we take the following assumptions of practical nature:

1. The isolation of the circulator terminated with matched loads is equivalent to the return loss of the input: $c_3=r_1$.
   In practice these values differ only slightly.
2. The insertion loss of the isolator is very small, and we can neglect it: $c_2=1$.
   In practice the small attenuation will improve the maximum vswr calculated a bit.
3. The third port has a perfectly matched load: $r_H=0$. Normally the loads used for terminating the third port are much better than the input reflection of the circulator, therefore the failure made by this assumption is negligible.

With these assumptions we get for the reflection factor

$$r = \frac{r_1(1 - r_1 r_L + r_L)}{1 - r_1 r_L} = r_1 + \frac{r_L}{1 - r_1 r_L}$$

where r, r_1, r_L are complex. Depending of the phase of the load reflection we will get different values for the input reflection of the isolator. In figure 12 the input vswr is calculated for an isolator with a vswr of 1,25 terminated with a phase varying load with a vswr of 5. As we can see the input vswr can lie between 1,47 and 1,09.
We get the maximum reflection factor, which is very interesting for the design of systems, from the last equation when taking the magnitude of the complex numbers and maximizing the whole expression:

$$r_{\max} = r_1 + \frac{r_L}{1 - r_1 r_L}$$

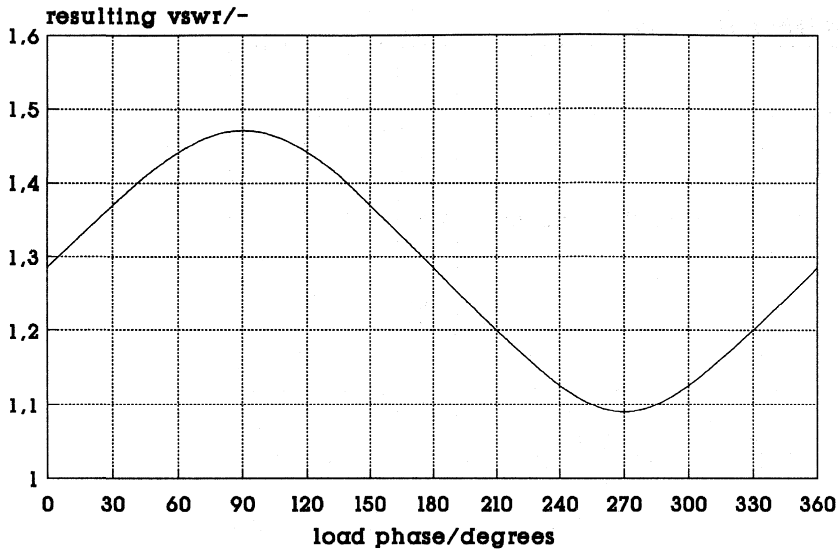


Fig.12: Resulting vswr at the input of an isolator with vswr of 1,25 terminated with a load of vswr=5 varying in phase

The maximum input vswr is then

$$s_{max} = \frac{1 + r_{max}}{1 - r_{max}}$$

In figure 13 the maximum vswr of the input of an isolator is given as a function of the load vswr with the vswr of the isolator as a parameter. For high load vswr's it is easier to look not at the vswr but at the return loss

$$r_{return\ loss} = -20\ lg(r)$$

Therefore in figure 14 the minimum input return loss of an isolator is given as a function of the return loss of the terminating load with the return loss of the isolator as a parameter. Here we can see, that the return loss of a load of 0 dB (vswr=∞, total reflection) is increased by an isolator with a return loss of 20 dB to a minimum return loss of 13,5 dB.

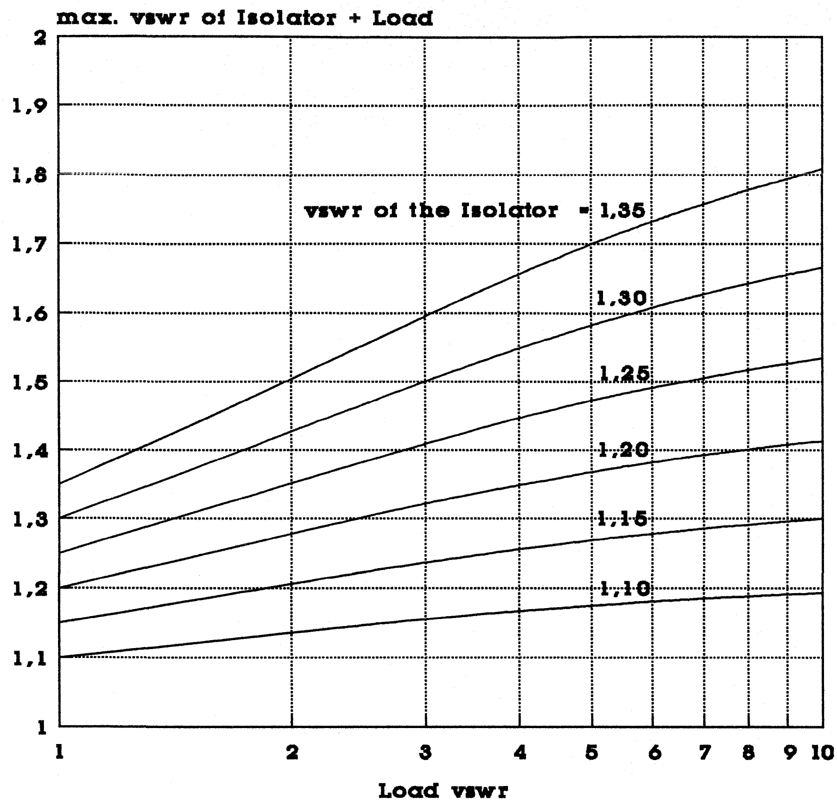


Fig.13: Reduction of the load vswr by an isolator. The maximum vswr of the cascade load plus isolator is given as a function of the load vswr with the vswr of the isolator

3.2 Behaviour of the input vswr or return loss of a circulator terminated with a filter

In applications with one transmitter and one receiver on one aerial or two or more transmitters or receivers on one aerial the circulator used is terminated with filters on two ports (see figure 15).
We assume that the transmitter and the receiver are reasonably matched at their ports. When looking into the filters from the circulator,

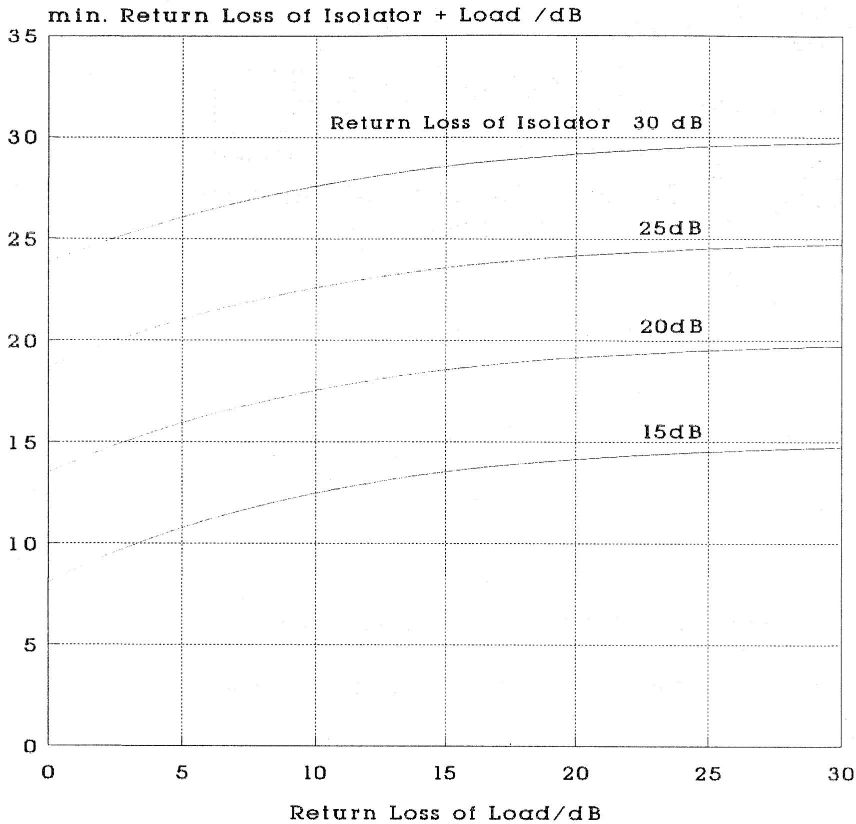


Fig.14: Increasing the load return loss by an isolator. The minimum return loss of the cascade load plus isolator is given as a function of the load return loss with the return loss of the isolator as a parameter

we see a reasonable match in the pass-band, but about total reflection in the stop-bands. These reflections influence the vswr s_a of the circulator at the antenna port.

We can calculate s_a by using the signal flow diagram of figure 11. As in the previous paragraph we can assume that

1. the isolation of the circulator terminated with matched loads is equivalent to the return loss of the input: $c_3=r_1$,
2. the insertion loss of the isolator is very small and can be neglected: $c_2=1$.

For the frequency bands of interest, receiving band and transmitting band, we have total reflection on one port (r_H=1) and a vswr s_L on the other port.
With these assumptions and the calculation of r_L out of s_L

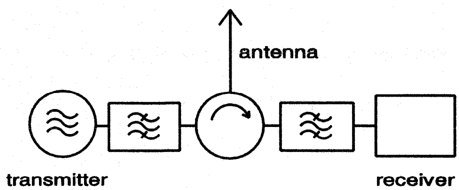


Fig.15: Transmitter and receiver on one antenna

$$r_L = \frac{s_L - 1}{s_L + 1}$$

we can simplify the complicated expression of page 15 to

$$r_a = \frac{r_1(2 - r_1 - 4r_1 r_L + 2r_1^2 r_L + r_L) + r_L}{1 - r_1 - 2r_1 r_L + r_1^2 r_L}$$

This approximation is valid for circulators with a vswr up to 1,30 and load vswr's up to 2. For higher values we have to take into account the insertion loss and the possible phases of r_1 and c_3.The maximum value of the reflection coefficient is

$$r_{a\,\max} = \frac{r_1(2 - r_1 - 4r_1 r_L + 2r_1^2 r_L + r_L) + r_L}{1 - r_1 - 2r_1 r_L + r_1^2 r_L}$$

or as a standing wave ratio

$$s_{a\,\max} = \frac{1 + r_{a\,\max}}{1 - r_{a\,\max}}$$

This is the worst vswr of the circulator at the antenna port when all the reflections add (see figure 16). But with variations in the line length between the filters and the circulator it can be improved drastically.

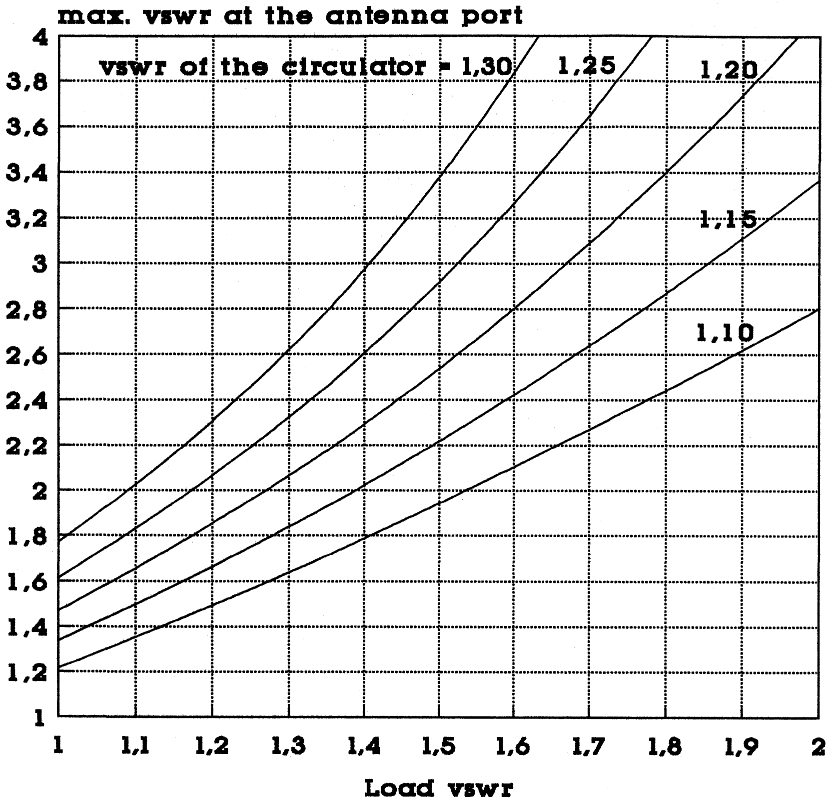


Fig.16: Worst vswr at the antenna port of a circulator terminated with a filter and a reflecting load

Literature:

1. Butterweck, H.J.: Der Y-Zirkulator, AEÜ 17(1963) S.163ff
2. Fiebig, A.: Lineare Signalflußdiagramme, AEÜ(1961), S.285ff

1992-08

1. Introduction

Circulators and isolators are passive devices used in modern rf and microwave equipment since some decades. By using them the stability, performance, and reliability of the systems can be improved, and often better and cheaper solutions are possible. In addition, in certain applications, e.g. one-port-amplifiers, the use of circulators is a must.
This booklet will help you to understand these important devices and give you some hints to use them effectively.

2. Definitions

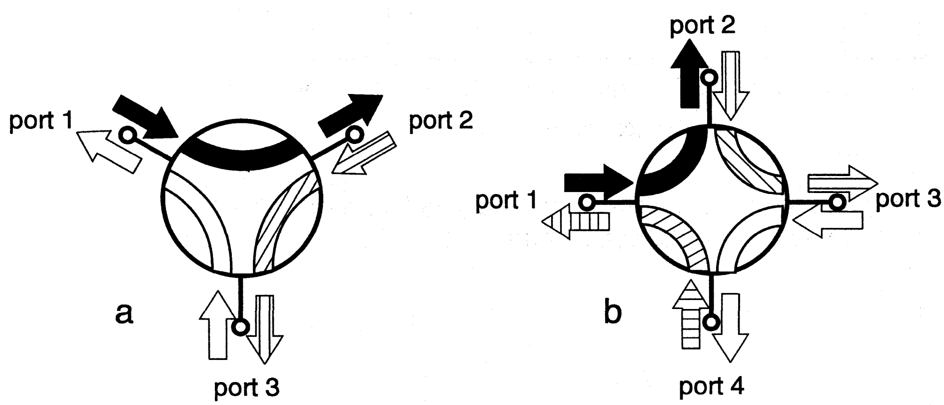


Fig.1: Energy flow in a. a 3-port-circulator
b. a 4-port-circulator

The circulator is defined as a passive device with 3 or more ports, where power is transferred from one port to the next in a prescribed order. That means for a 3-port-circulator (see fig.1a): power entering port 1 leaves port 2, port 3 is decoupled; power entering port 2 leaves port 3, port 1 is decoupled; and power entering port 3 leaves port 1,

port 2 is decoupled. For a 4-port-circulator it is similar (see fig.1b): power entering port 1 leaves port 2, port 3 and 4 are decoupled etc.
The isolator is defined as a passive two-port, where power is transmitted in one direction and absorbed in the other direction. That means power entering port 1 leaves port 2, but power entering port 2 is absorbed (see fig.2).

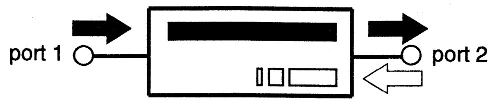


Fig.2: Energy flow in an isolator

An isolator can be a specially developed item. But we get also an isolator if we connect a matched load to port 3 of a 3-port-circulator.
Figure 3 gives the symbols used for circulators and isolators in circuit drawings.
By these definitions circulators and isolators are non-reciprocal devices, that means, their behaviour in one direction is very different from that in the other direction.

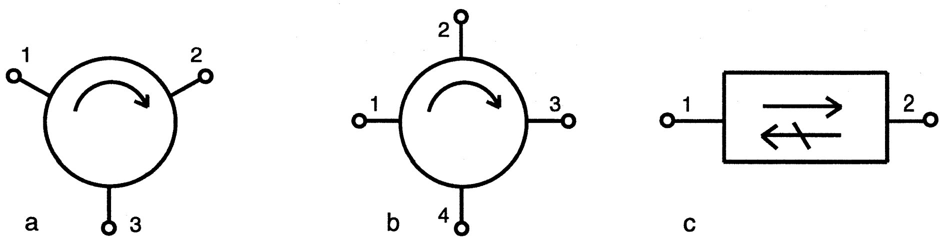


Fig.3: Symbols for a. 3-port-circulator
b. 4-port-circulator
c. isolator

3. Behaviour of ferrites

The way of operation of circulators and isolators is based on the unique properties of microwave ferrites. Therefore we will have a look on the behavior of ferrites under static and alternating fields at first.
Ferrites are magnetic material with very high ohmic resistance. Therefore they have nearly no eddy currents and are suitable for the operation at rf and microwave frequencies.
Like ferromagnetic material

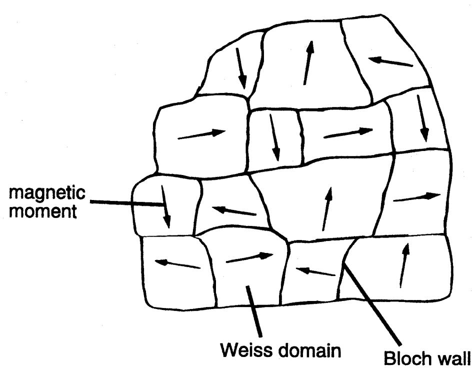


Fig.4: Planar model of Weiss domains

they consist of magnetic domains called Weiss domains, for Pierre Weiss discovered them 1908. The individual domains with dimensions of 1 to 100 μm are inherently magnetized by mutual exchange effects between adjacent electron spins. They are separated from each other by Bloch walls, named after their discoverer Felix Bloch. If there is no external magnetic field, the individual Weiss domains are oriented randomly. Therefore the resulting magnetization is zero (see fig.4).
If we apply an external magnetic field of sufficient strength, the magnetic moments of the individual Weiss domains are oriented in the direction of the external field and Bloch walls are displaced, resulting in an increase of the domains aligned with the external field. During this alignment the spinning electrons whose direction is changed makes a damped processional motion around the direction of the magnetic field as we know it in the mechanics from a gyro. If the procession has stopped, all magnetic moments are in the direction of the external magnetic field and the ferrite has its saturation magnetization.

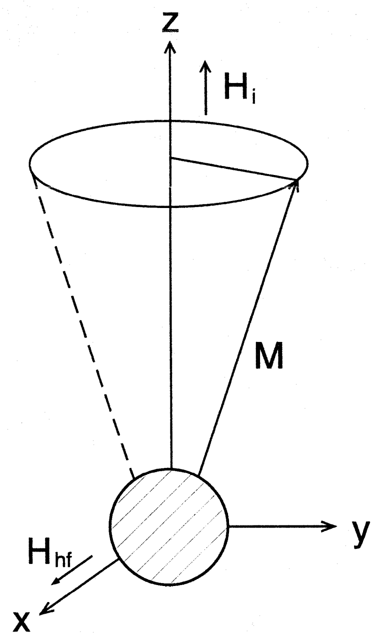


Fig.5: Precession of the spinning electron

If a small alternating rf field of a suitable frequency is applied perpendicular to the direction z of the strong static magnetic field H_i, e.g in the x-direction as shown in figure 5, the magnetic Moment M processes around the direction of H_i. Therefore there is not only a component of the magnetic moment in the x-direction but also one in the y-direction. Now the μ in the relationship between induction B and magnetic field H is no longer scalar but a tensor, known as the Polder tensor [1]. And we can write the relationship between B and H as follows:

$$\begin{aligned} B_x &= myH_x - j\kappa H_y \\ B_y &= j\kappa H_x + myH_y \\ B_z &= my_0 H_z \end{aligned} \qquad (3.1)$$

or expressed as a tensor

$$\begin{pmatrix} B_x \\ B_y \\ B_z \end{pmatrix} = \begin{pmatrix} my & -j\kappa & 0 \\ j\kappa & my & 0 \\ 0 & 0 & my_0 \end{pmatrix} \begin{pmatrix} H_x \\ H_y \\ H_z \end{pmatrix} \qquad (3.2)$$

The value of the induction component perpendicular to the magnetic rf field is determined by the value of κ. The values of $\mu = \mu' - j\mu''$ and $\kappa = \kappa' - j\kappa''$ are complex and depend on the static magnetic field, the frequency, and the material properties of the ferrite.
If the magnetic plane of an electromagnetic wave is parallel to H_i, the relative permeability is $\mu_{eff\parallel} = \mu_0$, for the ferrite is saturated. The propagation speed is

$$\gamma_{\parallel} = j\omega\sqrt{\epsilon my_0} \qquad (3.3)$$

The ferrite has no gyromagnetic effect on the wave.

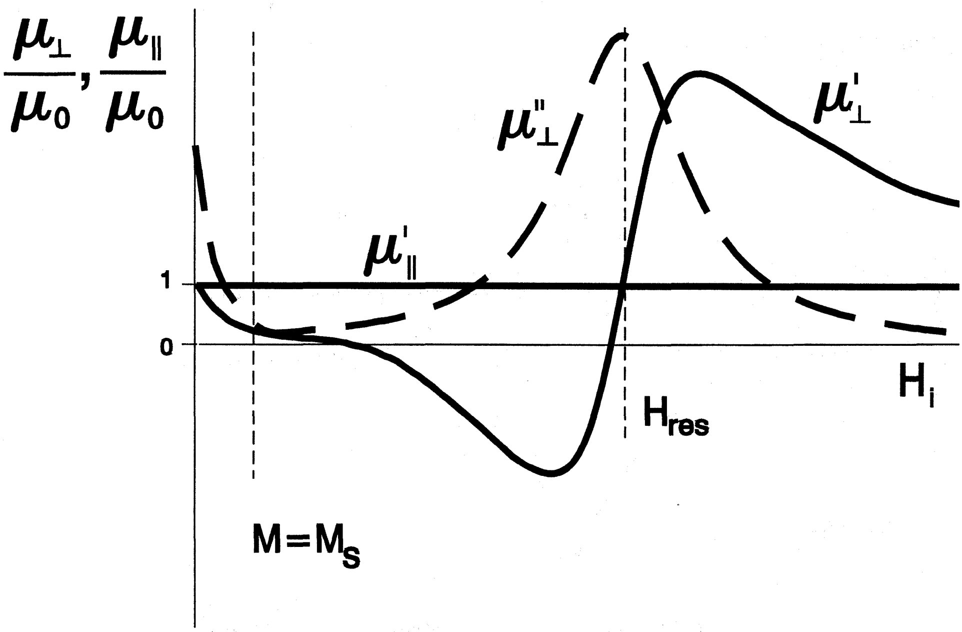


Fig.6: $\mu_{eff\parallel}$ and $\mu_{eff\perp}$ of a microwave ferrite as a function of the static magnetic field H_i

If the magnetic plane of the electromagnetic wave is perpendicular to H_i, the relative permeability is

$$my_{eff\perp} = \frac{my^2 - \kappa^2}{my} \qquad (3.4)$$

and the propagation constant

$$\gamma_{\perp} = j\omega\sqrt{\epsilon my_{eff\perp}} \qquad (3.5)$$

Figure 6 shows the real and imaginary parts of $\mu_{eff\parallel}$ and $\mu_{eff\perp}$ as a function of H_i. In the vicinity of the resonant value H_{res} of the static magnetic field the losses in the ferrite, represented by $\mu''_{eff\perp}$, rise steeply, for the precessional motions of the electron spins are generated by the components perpendicular to the static field.
If a circular polarized wave with a plane perpendicular to the direction of the magnetic field is polarized clockwise (+), the interaction with the electron spins results in a permeability of $\mu_+=\mu-\kappa$. The corresponding propagation speed is

$$\gamma_+ = j\omega\sqrt{\epsilon m y_+} \tag{3.6}$$

The Ferrite has no gyromagnetic effect on the wave.

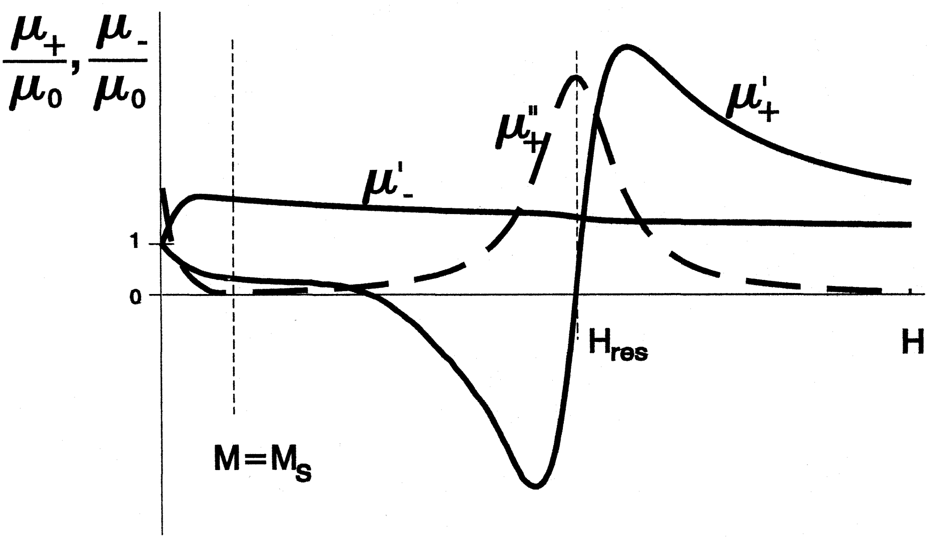


Fig.7: μ_+ and μ_- of a microwave ferrite as a function of the static magnetic field H_i

If the polarization of the wave is anti-clockwise (-), the interaction with the electron spins give the permeability $\mu_-=\mu+\kappa$, and the propagation speed is

$$\gamma_- = j\omega\sqrt{\epsilon m y_-} \tag{3.7}$$

Figure 7 gives μ_+ and μ_- as a function of the magnetic field. μ_+, which rotates in the same direction as the electron spins, shows a resonance, for it causes them to precess, μ_- counteracts the precession, and therefore there is no resonance.

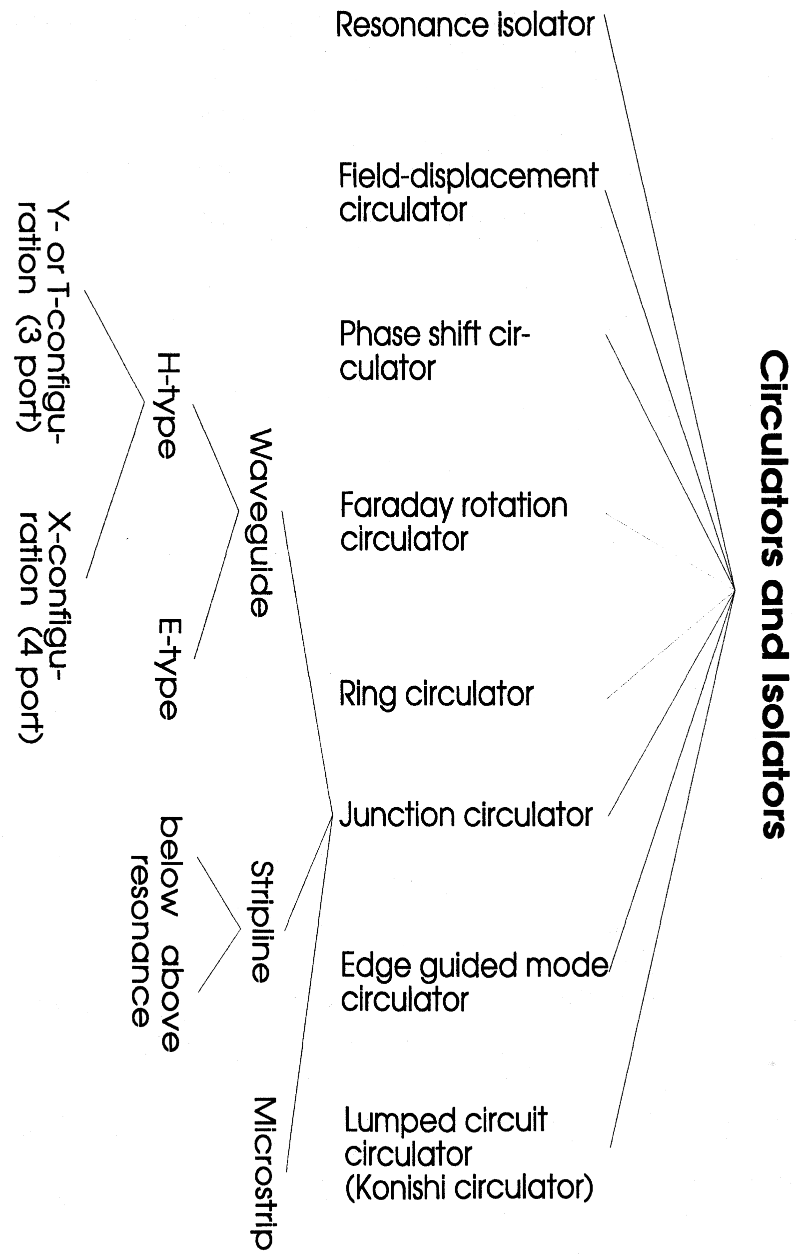

Circulators and Isolators
Resonance isolator
Field-displacement circulator
Phase shift circulator
Faraday rotation circulator
Ring circulator
Junction circulator
Edge guided mode circulator
Lumped circuit circulator (Konishi circulator)
Waveguide
Stripline
Microstrip
H-type
E-type
below resonance
above resonance
Y- or T-configuration (3 port)
X-configuration (4 port)

Figure 8

4. Principles of operation and construction

The behavior of ferrites described in chapter 3 is the basis for different modes of operation for circulators and isolators. Figure 8 gives a survey.

4.1 Resonance isolator

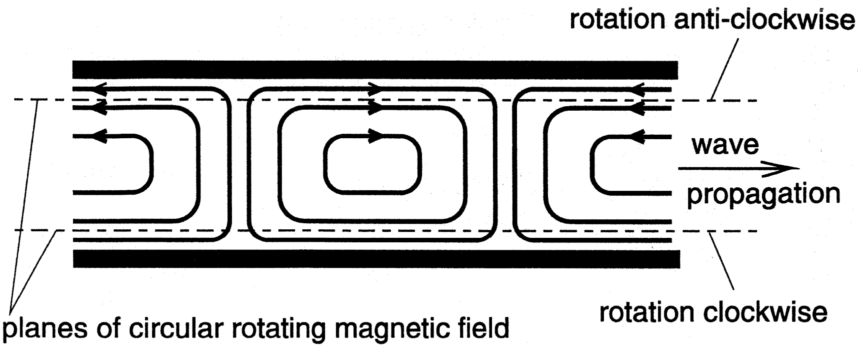


Fig.9: Rectangular waveguide with H_{10}-mode

Resonance isolators are constructed in rectangular waveguides carrying the fundamental mode H_{10}. In two planes parallel to the small sides of the waveguide the magnetic field of the wave is circular rotating, in one direction of the wave propagation clockwise, in the opposite direction of the wave propagation anti-clockwise (see figure 9). The position of these planes is frequency dependant.

If we put ferrite slabs in these planes and magnetize them to the resonance field H_{res} as shown in figure 6, we get an isolator: the wave with μ_- has low losses in the ferrite, the opposite travelling wave with μ_+ has high losses and is damped.

Figure 10 shows the principle construction of such an isolator. The ferrites are in contact with the waveguide walls to transfer the heat generated in the ferrite to the waveguide. In principle the isolator is a small band device, for the resonance peak giving the isolation is not broad. But if we shape the static magnetic field we can make it broader.

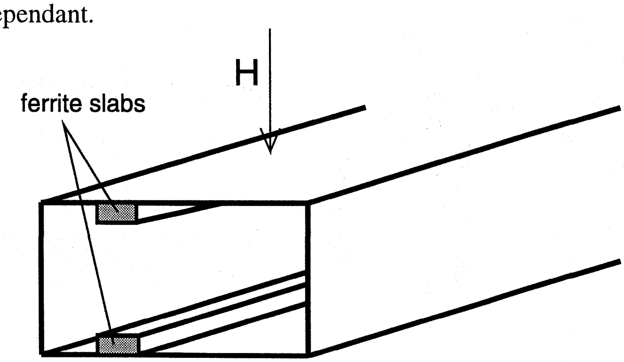


Fig.10: Principle construction of a resonance isolator

These devices are heavier compared with others and are not often used nowadays.

4.2 Field displacement circulator

Also the field displacement circulator [2] is built in rectangular waveguide with the H_{10}-mode and uses the planes of circular rotating magnetic rf fields. But the static magnetic field is not adjusted to the resonance but much lower.
A ferrite slab extending from one broad side to the other will influence the H_{10}-mode in such a way, that for a wave travelling in one direction the electrical field is taken into the ferrite giving a high value on one side of the slab, and pushing it out if the wave travels in the opposite direction giving a very low value on that side of the slab (see fig.11).
Although it is possible to make circulators with this phenomenon, the practical devices are isolators. Figure 12 shows the common construction.
A ferrite slab smaller than the small side of the waveguide is situated in one of the planes of circular rotating rf fields. On the inner side of the slab a resistive layer is put, often in thick film techniques. In the forward direction of the isolator the electric rf field in this plane is a minimum, resulting in low insertion loss. In the backward direction the rf field in this plane is high and the wave is damped by the resistive layer, giving high isolation. The value of this isolation can be increased by increasing the length of the isolator. A ceramic slab clad to the ferrite is used to increase the bandwidth of the isolator by fixing the minimum and the maximum of the rf fields in the plane of the resistive layer.

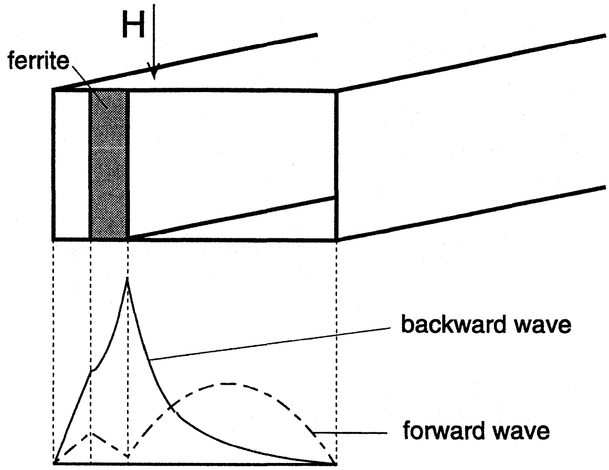


Fig.11: Electrical field of a field displacement circulator with a ferrite extending from one broad side to the other

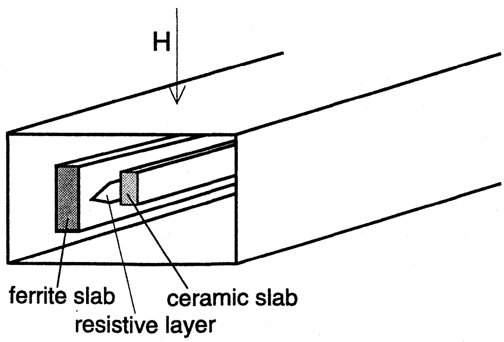


Fig.12: Principle construction of a field displacement isolator

4.3 Phase shift circulator

The phase shift circulator is built in rectangular waveguide with the H_{10}-mode. It uses three elements:

- a folded magic tee
- a non-reciprocal phase shifter
- a 3dB-coupler

see figure 13.

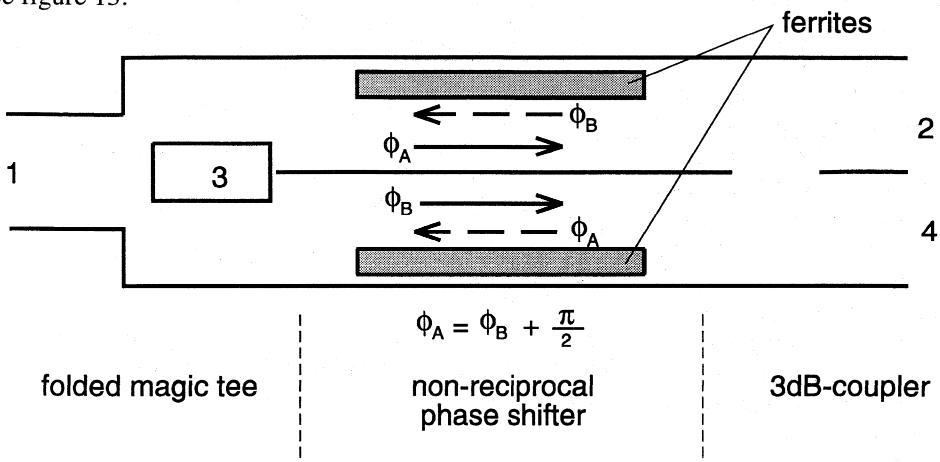


Fig.13: Principle construction of a phase shift circulator

A wave entering port 1 of the magic tee is split into 2 waves of equal energy and equal phase, which enter the non-reciprocal phase shifter. The first wave will be shifted by the non-reciprocal phase shifter by ϕ_A, the second wave by ϕ_B, where $\phi_A = \phi_B + 90$ degrees. In the 3dB-coupler the two waves are split again into two equal parts, but the wave going to the other guide is delayed by 90 degrees. Therefore the waves add at port 2 and cancel each other at port 4.

A wave entering port 2 is split in the 3dB-coupler into 2 waves with equal amplitude but 90 degrees phase difference. The first one will be shifted by ϕ_B, the second by ϕ_A. In the magic tee both waves combine and cancel each other at port 1, but add at port 3, and so on.

The principle construction of the non-reciprocal phase shifter is the same as the resonance isolator. But the permanent magnetic field is lower than for resonance. The interaction of the rf wave with the spinning electrons give a delay in one direction and no effect in the other. Thickness and length of the ferrite slabs, and the permanent magnetic field are chosen to give a phase difference of 90 degrees.

The phase shift circulator is used for high power handling. The construction is bulky, especially for high cw power (e.g. 1.5 MW_{cw} at 500 MHz).

4.4 Faraday rotation circulator

The Faraday rotation circulator [3] is based on the rotation of the polarization plane of an rf wave by the magnetic moments of the ferrite.
A H_{10}-wave in a rectangular waveguide traverses via a transition into a round waveguide and forms the linear polarized H_{11}-wave. In the middle of the linear waveguide there is a round ferrite rod magnetized in the direction of the rod.

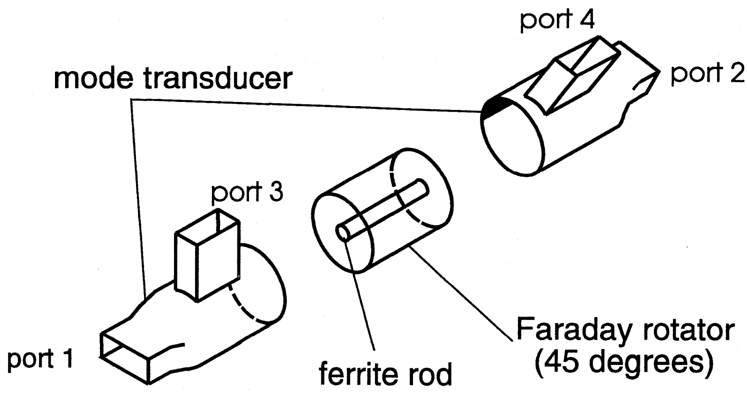


Fig.14: Principle construction of a Faraday rotation circulator

We can split a linear wave into two circular rotating waves, one rotating clockwise, the other anti-clockwise when looking in the direction of propagation. These two waves interact with the electron spins of the ferrite rod and have the propagation speed μ_+ and μ_- which differ from each other. If we combine the two rotating waves after they have travelled some distance, we get a linear wave again, but rotated some degrees.
The length of the ferrite rod and the magnetic field are chosen for a rotation of 45 degrees. Another transition from round waveguide to rectangular waveguide finishes the circulator (see figure 14). A H_{10}-wave entering port 1 is transformed to the round waveguide. The ferrite rotates the wave clockwise by 45 degrees. The second transition transforms it to the rectangular waveguide which has also an angle of 45 degrees with respect to the first rectangular waveguide, and the wave leaves the circulator at port 2. A wave entering port 2 travels in the opposite direction and is also rotated clockwise by 45 degrees. Now it is perpendicular to the waveguide of port 1, but can leave the circulator at port 3, etc.
Most of the devices using the Faraday rotation are not circulators but isolators. They have only the input and output ports 1 and 2 and absorb the waves perpendicular to them by resistive sheets.
Faraday rotation isolators are built for very high frequencies and nowadays for optical isolators for fibre cables.

4.5 Ring circulator

The ring circulator is a circulator discussed in theory, but not really used in practice. It is formed out of three junctions and three nonreciprocal phase shifters (see figure 15). A wave entering port 1 is split into one going clockwise around and another going anticlockwise around the circulator ring. The phase shift of the nonreciprocal phase shifters is adjusted so, that they cancel each other at port 3 and add up at port 2 and leave the circulator.

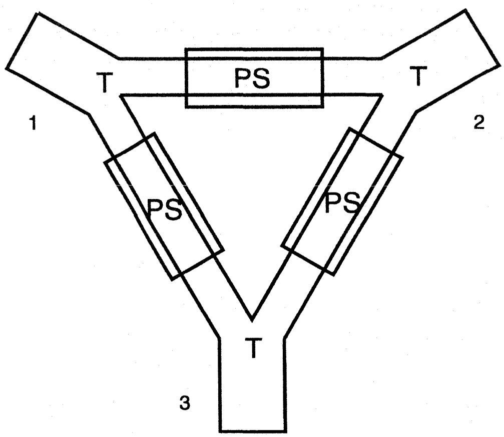


Fig.15: Principle construction of a ring circulator
T reciprocal T-junction
PS non-reciprocal phase shifter

4.6 Junction circulator

The junction circulator is the most common circulator. It is done in waveguide, in tri-plate mostly with coaxial connectors, and in microstrip.
Let us start with a tri-plate circulator. The principle construction is given in figure 16: between two outer conductors are two ferrite discs, and between them the inner conductor. This inner conductor forms a resonator and the matching networks to the ports. Two magnets out-side the outer conductors give the static magnetic field.

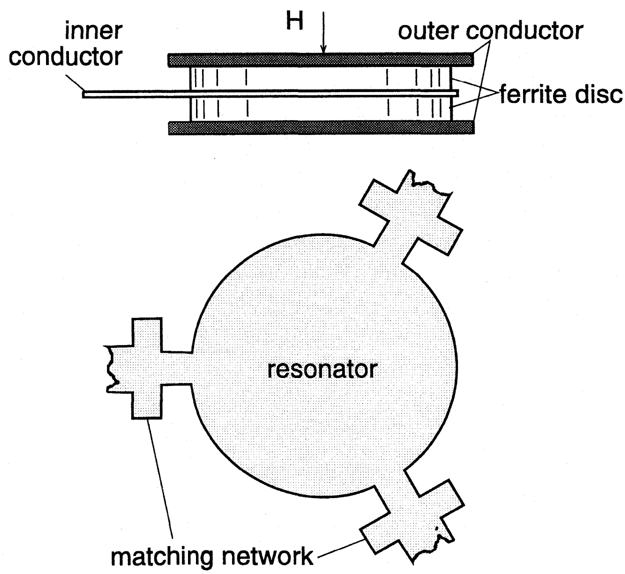


Fig.16: Principle construction of a tri-plate junction circulator

Fay and Comstock [4] explained the operation in the following way (see fig 17):
Without a permanent magnetic field a wave entering port 1 is split into two rotating waves with the same propagation speed, one rotating clockwise, the other anti-clockwise, giving a standing wave pattern in the resonator, which is coupled to port 2 and port 3. The incoming wave is divided and half of the power leaves port 2, the other half port 3 (figure 17a).

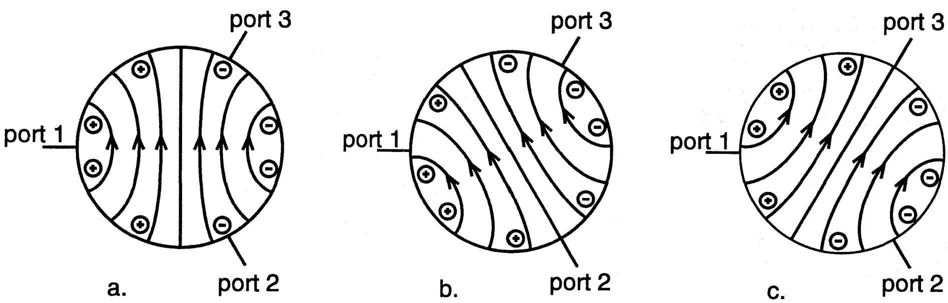


Fig.17: Standing wave pattern of a junction circulator
a. unmagnetized
b. magnetized below resonance
c. magnetized above resonance

With a permanent magnetic field supplied perpendicular to the ferrite discs, the propagation speed of the two rotating waves is no longer the same. The wave rotating clockwise has now the propagation speed γ_+, the wave rotating anti-clockwise the propagation speed γ_-. This results in a rotation of the standing wave pattern. By increasing the magnetic field the standing wave pattern rotates anti-clockwise. If the angle of rotation is 30 degrees, the device is a circulator (see figure 17b): Port 3 is decoupled and all energy passes from port 1 to port 2.
But there is also another magnetic field for circulator operation. If we use a much higher magnetic field and adjust it so, that the standing wave pattern is rotated 30 degrees clockwise, port 2 is decoupled and all energy passes from port 1 to port 3 (see figure 17c).
For the first mode of operation we need a static magnetic field lower than for putting the ferrite into resonance, therefore this mode is called below resonance, for the second mode of operation the magnetic field is higher than for resonance, therefore we call this mode above resonance.
Tri-plate junction circulators are made as above resonance circulators in the frequency range 150 MHz to about 2 GHz and as below resonance circulators in the frequency range 1.5 to 20 GHz.

The operation of microstrip junction circulators is very similar as this of tri-plate circulators. They operate in the below resonance mode.
Also waveguide junction circulators operate below resonance. Figure 18 shows the principle construction. The operation can be explained in the same way as for the tri-plate circulator.

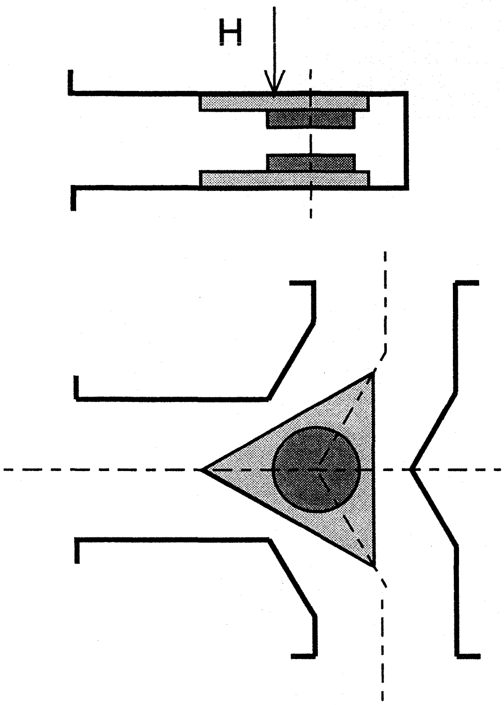


Fig. 18: Principle construction of a waveguide junction circulator

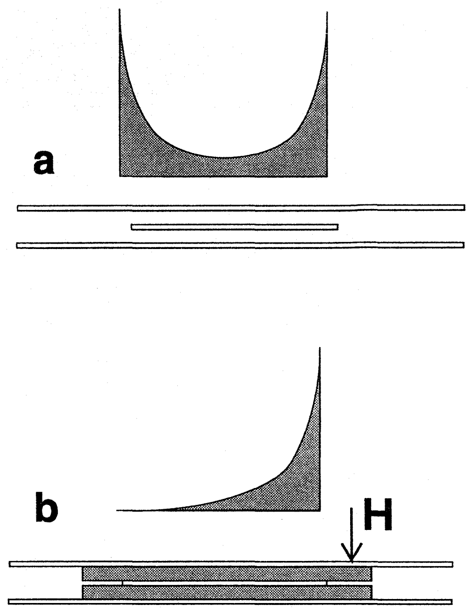


Fig.19: Current density in a broad inner conductor of a tri-plate line

a. normal line
b. line filled with ferrite and magnetized perpendicular

4.7 Edge guided mode circulator

In broad tri-plate or microstrip lines the rf currents run on the two edges of the inner conductor (see figure 19a). Is there a microwave ferrite between inner and outer conductor biased with a permanent magnetic field perpendicular to the line, then the rf current runs on one edge of the inner conductor only for the forward wave and on the other for the backward wave (see figure 19b).
This behaviour can be used for the construction of circulators, but normally very broadband isolators (broader than one octave) are made by this effect. In figure 20 such an isolator is shown schematically. The wave coming from the input passes at first a

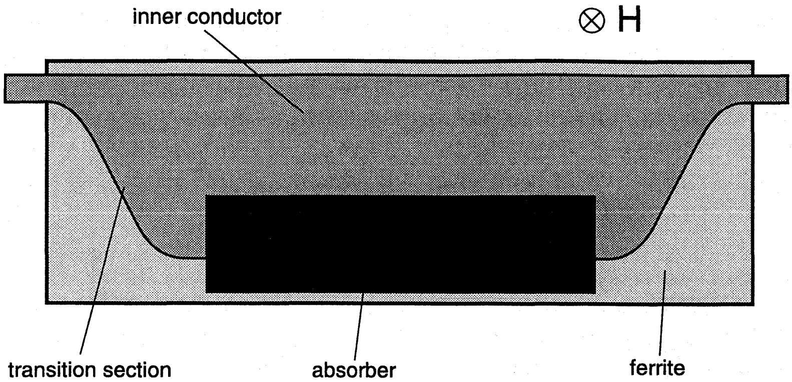
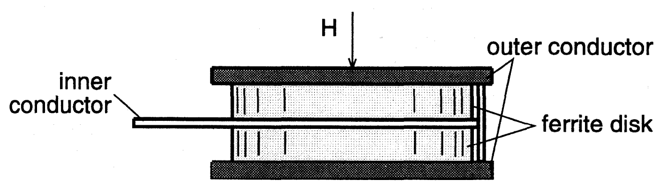


Fig. 20: Principle construction of an edge guided mode isolator

transition to the broad stripline. In the forward direction it runs nearly unattenuated on the left edge of the inner conductor of this line and reaches the second transistion and finally the output. The wave entering the isolator at the output passes the second transition to the broad stripline and runs on the right edge of the inner conductor. Here it comes to the damping material and will be attenuated.



The operation of the edge guided mode circulator is very similar to the operation of the field displacement circulator in the waveguide.

4.8 Lumped element circulator

For low frequencies the principles of operation described up till now give too big and too heavy constructions. This is the domain of the circulators built of lumped elements. The core of them is the non-reciprocal junction, often called isoductor. Figure 21 shows the principle construction of such an

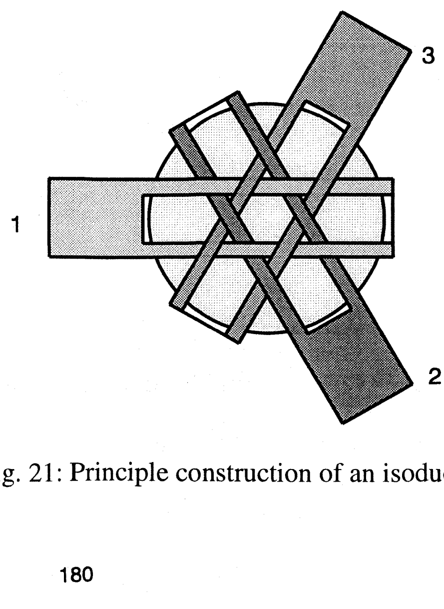


Fig. 21: Principle construction of an isoductor

isoductor: three inner conductors coming from the three ports cross under an angle of 120 degrees and are connected to the outer conductors at the other end. They are isolated from each other where they cross each other. Between the inner and outer conductors there are two ferrite disks, magnetized by a permanent magnetic field.

An rf current in inner conductor 1 generates in the ferrite disks an rf magnetic field perpendicular to the plane of the loops, which it makes together with the outer conductors. Due to the properties of the ferrite the rf magnetization is not in the same direction, as we can see in the Polder tensor page 3. The angle between the rf magnetic field and the rf magnetization depends on the frequency and the permanent magnetic field. If we adjust the permanent magnetic field so that the rf magnetization is parallel to the inner conductor 3, then loop 3 is not induced but only loop 2: an excitation of inner conductor 1 will be coupled to inner conductor 2 but not to inner conductor 3, inner conductor 3 is decoupled.

If we look from outside into one port of the isoductor, we see an inductance parallel to a resistor (see figure 22).

The simplest way to make a ciculator out of this isoductor is given in figure 23: We bring the inductance of the isoductor into resonance by a parallel capacitor and match the whole to the line by a series capacitor. With more complicated networks we can build broadband circulators with a band-width of up to one octave.

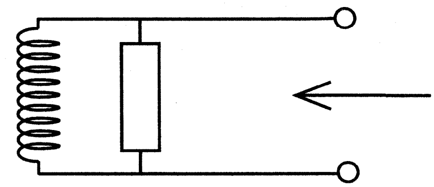


Fig.22: Equivalent circuit of an isoductor

Lumped element circulators can be made for frequencies between 30 MHz and about 2 GHz, but normally they are used between 50 and 500 MHz.

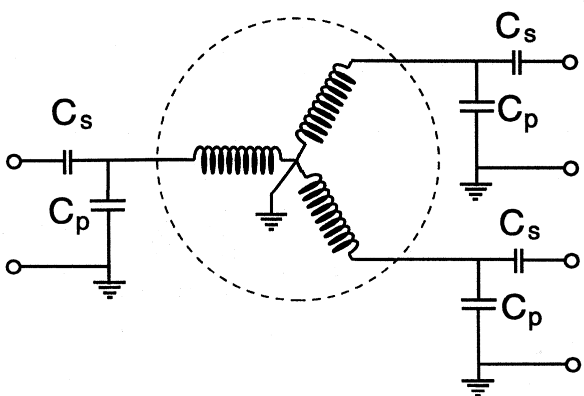


Fig. 23: Small band lumped element circulator

6. Correlation of parameters of a symmetrical 3-port-circulator

6.1 The lossless symmetrical 3-port- circulator

The relationship of the input waves a_n and the output waves b_n of a 3-port-circulator (see figure 24) can be written as

$$\begin{pmatrix} b_1 \\ b_2 \\ b_3 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{pmatrix} \cdot \begin{pmatrix} a_1 \\ a_2 \\ a_3 \end{pmatrix} \quad (6.1)$$

or

$$b = S \cdot a \quad (6.1a)$$

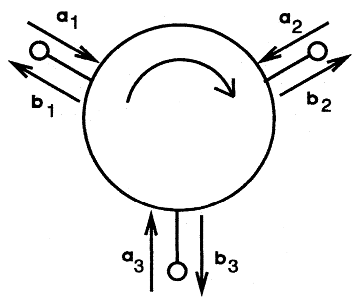


Fig. 24: Input and output waves

with S_{nm} the scattering parameters and S the scattering matrix respectively. The non-reciprocal behaviour of the circulator is reflected in the asymmetry of the scattering matrix:

$$\begin{pmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{pmatrix} \neq \begin{pmatrix} S_{11} & S_{21} & S_{31} \\ S_{12} & S_{22} & S_{32} \\ S_{13} & S_{23} & S_{33} \end{pmatrix} \quad (6.2)$$

that means $S_{12} \neq S_{21}$, $S_{13} \neq S_{31}$, $S_{23} \neq S_{32}$. If we assume that the circulator is lossless, then the sum of the input powers is equal to the sum of the output powers, or in the expressed in the form of a matrix: the product of the scattering matrix S with the transposed and conjugate complex scattering matrix S'^* equals the unity matrix

$$\begin{pmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{pmatrix} \cdot \begin{pmatrix} S_{11}^* & S_{21}^* & S_{31}^* \\ S_{12}^* & S_{22}^* & S_{23}^* \\ S_{13}^* & S_{23}^* & S_{33}^* \end{pmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{pmatrix} \quad (6.3)$$

or

$$S \cdot S^{|*} = E \qquad (6.3a)$$

If we assume, that our circulator is cyclically symmetrical, then we can write

$$= S_{22} = S_{33} = S_1 \quad \text{the input reflexion of the ports}$$
$$= S_{23} = S_{31} = S_2 \quad \text{the isolation of the circulator} \qquad (6.4)$$
$$= S_{13} = S_{32} = S_3 \quad \text{the insertion loss of the circula}$$

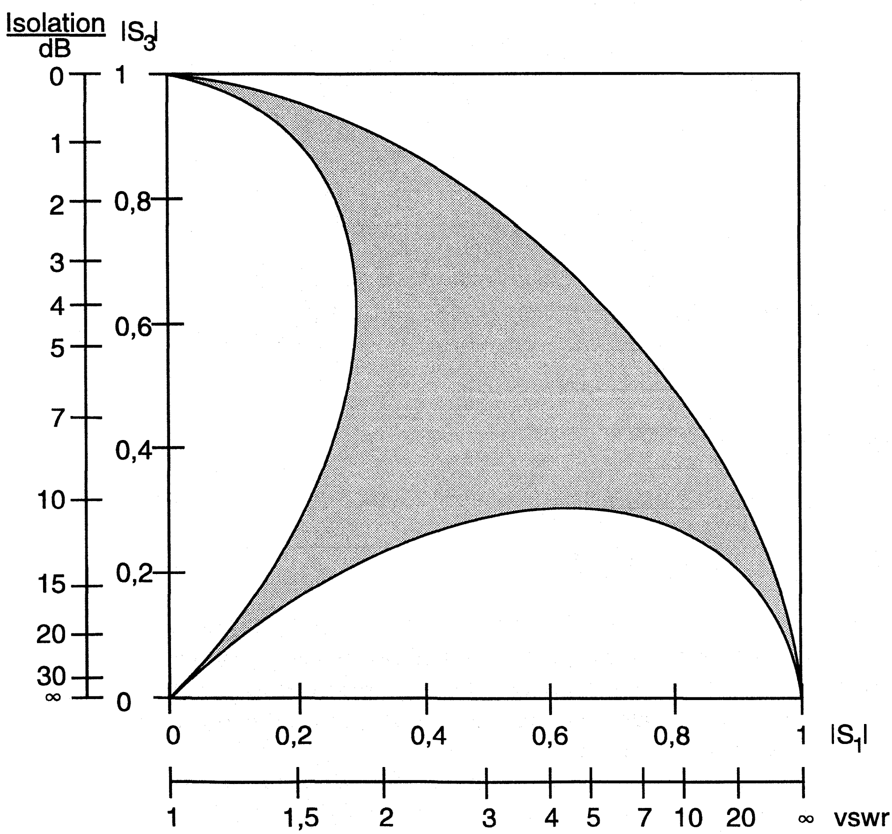


Fig. 25: Permissible area for $|S_1|$ and $|S_3|$

but for the reason of non-reciprocity $S_2 \neq S_3$. Now we can write the scattering matrix more simple:

$$S = \begin{pmatrix} S_1 & S_2 & S_3 \\ S_3 & S_1 & S_2 \\ S_2 & S_3 & S_1 \end{pmatrix} \qquad (6.5)$$

If we combine now the scattering matrix (6.5) and the matrix equation (6.3a), then we get

$$\begin{aligned} S_1^* S_1 + S_2^* S_2 + S_3^* S_3 = |S_1|^2 + |S_2|^2 + |S_3|^2 &= 1 \\ S_1^* S_2 + S_3^* S_1 + S_2^* S_3 &= 0 \\ S_1^* S_3 + S_3^* S_2 + S_2^* S_1 &= 0 \end{aligned} \qquad (6.6)$$

These relationships show us that not all combinations of S_1, S_2, and S_3 are possible for a lossless, cyclical symmetrical 3-port-circulator (see Butterweck [6]). The permissible combinations of e.g. $|S_1|$ and $|S_3|$ values can be given graphically as a curved triangle in the $|S_1|,|S_3|$-plane limited by elliptical curves as given in figure 25 as a shaded area.
In this figure we find for high isolation, that means low $|S_3|$, two permissible regions for the input vswr or $|S_1|$, one for low vswr ($|S_1| \approx 0$) and a second one, which is not of interest for circulators, for very high vswr ($|S_1| \approx 1$).

6.2 The lossy symmetrical 3-port-circulator

For a lossy 3-port equation (6.3) is not valid. We have to replace it by

$$(E - S^{t*} \cdot S) \quad \textit{positive semidefinite} \qquad (6.7)$$

That means for a lossy symmetrical 3-port-circulator that the permissible combinations of e.g. $|S_1|$ and $|S_3|$ values can lie also a bit outside of the curved triangle of figure 25, depending on the value of the loss. E.Schwartz and H.Bex calculated the new boundaries in [7]. Figure 26 presents the results for the region of high isolation (low $|S_1|$) and low vswr (low $|S_3|$ values).
From figure 26 we can see, that the permissible area for the vswr and isolation is not restricted to the small region of the lossless 3-port-circulator given in figure 25 but broadens with increasing insertion loss. For example for a vswr of 1.2 and an insertion loss of 0.2 dB in the isolation can lie between 19 and 24 dB while in the lossless case it is around 21 dB.
Figure 26 gives the theoretical limits of the relationships between vswr and isolation. In practice the values measured are closer to the lossless case.

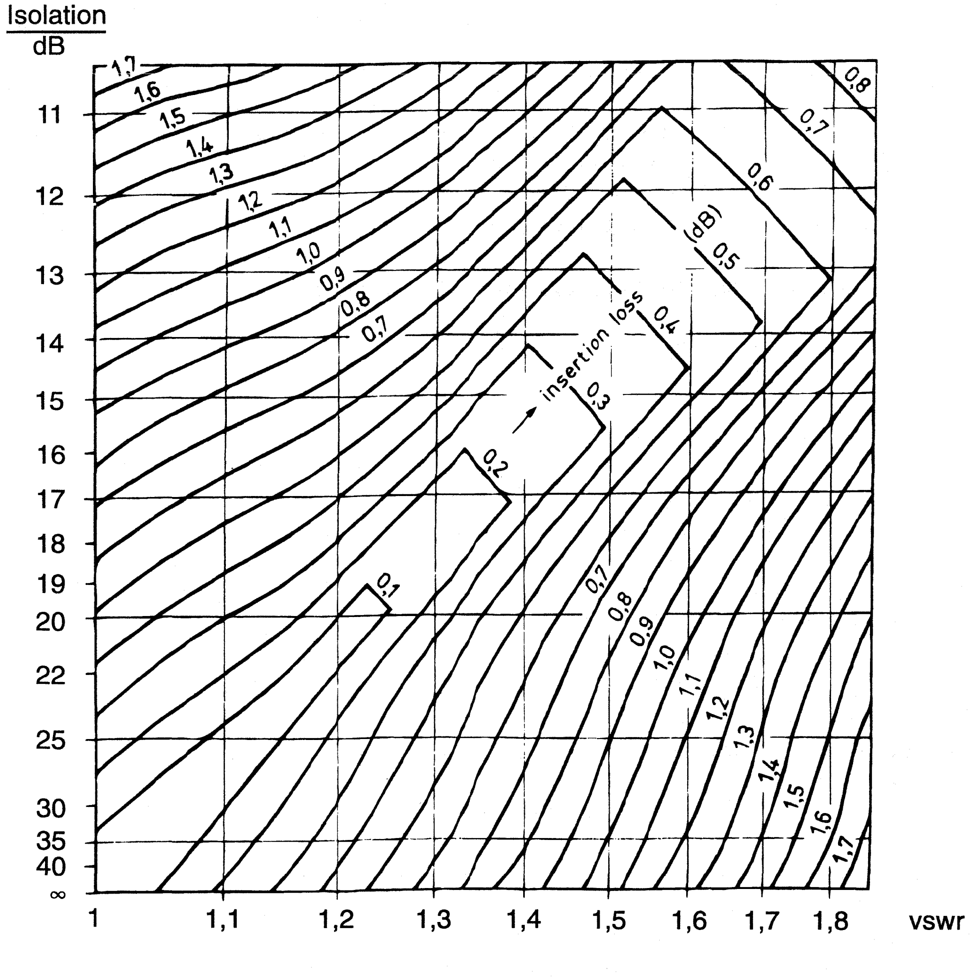


Fig. 26: Permissible combinations for a lossy symmetrical 3-port-circulator with low vswr and high isolation with the insertion loss as a parameter

7. Application

Circulators and isolators can be used

for

◇ decoupling - of generator and load of amplifier stages

◇ reducing
- intermodulation caused by other transmitters
- load return loss and vswr

◇ combining
- two and more transmitters
- transmitters and receivers on the same antenna
- amplifier stages in solid state transmitters

◇ operating one-port-amplifiers

◇ duplexing

◇ locking and priming of oscillators

in
- broadcast and TV - transmitters
- radio links and navigation
- air traffic control
- radar systems
- military equipment
- car telephone systems
- measurement systems
- industrial microwave heating applications
- magnetic resonance tomography

7.1 Decoupling of generator and load

Generators are influenced by their loads resulting in frequency shift (pulling), instabilities, and, if a long line connects generator and load, even frequency jumping under certain conditions (long line effect). To avoid this we can put an attenuator of e.g. 10 dB between generator and load to attenuate the reflected signal by 20 dB (see figure 27a). This will result in high losses in this attenuator.

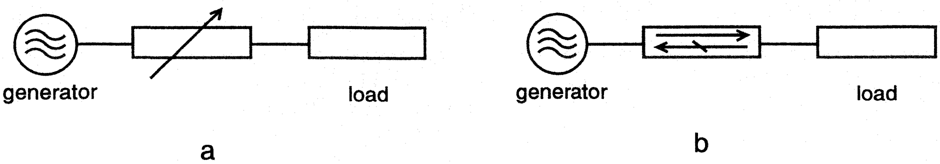


Fig. 27: Decoupling of generator and load
a. with a variable attenuator
b. with an isolator

An isolator of 20 dB isolation instead of the attenuator will do the same job (figure 27b). But the attenuation is now only the insertion loss of the isolator, normally less then 0.5 dB.

7.2 Decoupling of amplifier stages

The different stages of an amplifier influence each other, especially if they are small-banded. If they are decoupled by isolators (see figure 28) each stage can be tuned and adjusted without affecting the others. And if one stage fails, the others will not be overloaded. Also the time interval for readjusting power transmitters can be extended very much in this way. Especially between the driver stages and klystrons or inductive output tubes (IOT's) as final amplifiers isolators are highly recommended for decoupling them.

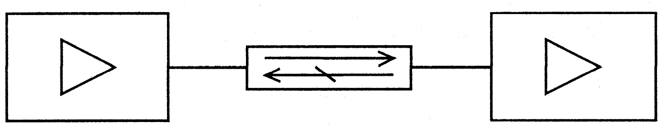


Fig. 28: Decoupling of amplifier stages

7.3 Decoupling of a transmitter or receiver from its antenna

If a transmitter is connected to an antenna it may be influenced by impedance changes of the antenna caused e.g. by snow or near-by obstacles. This can be avoided by an isolator with an isolation of about 20 dB (figure 29).
Furthermore other antennas in the neighbourhood may couple signals into the antenna, which travel to the amplifier. The final stage operates in class B or C to

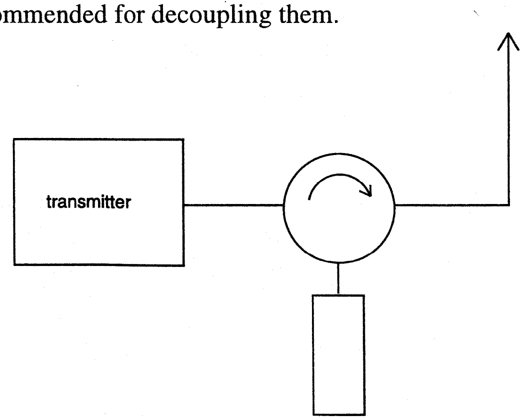


Fig. 29: Decoupling of a transmitter from its antenna

give high efficiency resulting in very non-linear behaviour. Therefore the induced signal will mix with the signal of the amplifier giving intermodulation.
The intermodulation can be reduced by an isolator. But here often a normal isolator with an isolation of 20 dB is not sufficient. To reduce the level of the intermodulation products to the desired value normally double isolators with an isolation of about 50 dB are required.
The input stage of a receiver is often a low noise amplifier which input impedance is chosen to give a very low noise figure but no match to the antenna. An isolator between the antenna and the input of the receiver will get rid of this problem.

7.4 Transmitter and receiver on the same antenna

If we operate one transmitter and one receiver on the same antenna tuned to different frequencies, normally we use two sharp and expensive filters to avoid interaction between them (see figure 30a). Using a circulator for branching, only one inexpensive filter is necessary at the input of the receiver, for the power of the transmitter at the input of the receiver branch is reduced by more than 10 dB by the circulator, depending on the impedance of the antenna (figure 30b).

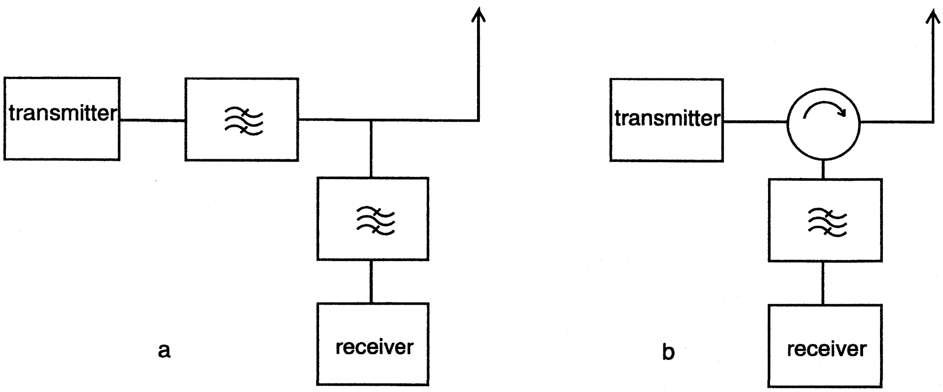


Fig. 30: Transmitter and receiver on the same antenna
a. conventional solution
b. solution with a circulator

7.5 Combiner for 2 or more transmitters in the VHF- and UHF-bands

Combining 2 or more transmitters e.g. for the operation on one antenna is done conventionally in the following way (see figure 31a): each 2 transmitters are connected to a 3-dB-hybrid. One output arm is terminated to a matched load, the other goes to the antenna, if we have to combine 2 transmitters only, or to the next 3-dB-hybrid. If we have to combine 4 transmitters as in figure 31, we have to use three 3-dB-hybrids, and the signal of each transmitter passes two of them. The losses in this coupling circuit are high: we have about 0.5 dB losses in the 3-dB-hybrid and convert half of the power in the matched load into heat. For our combiner for 4 transmitters this results in a loss of about 7 dB. If we have to combine more than 4 transmitters the losses are even higher. The frequency spacing of the transmitters is limited only by the bandwidth of the 3-dB-hybrids.

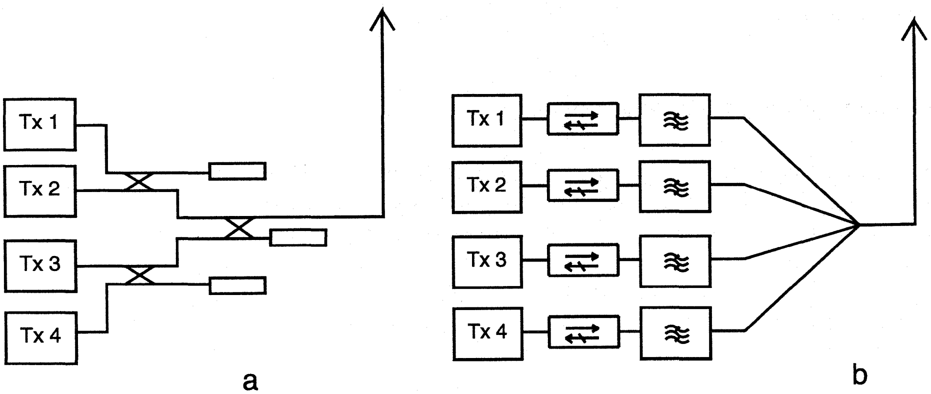


Fig. 31: Combiner for 4 transmitters in the VHF- or UHF-bands
a. conventional solution
b. solution with isolators

Using isolators we can build a completely different combiner (see figure 31b): the transmitter is connected to a cavity, which is tuned to its signal, via a double-isolator. Cables with a length of λ/4 or odd multiples of it or λ/2 or multiples of it, depending of the coupling of the cavity, connect the different cavities with a star point, which leads to the antenna.

The signal of transmitter 1 passes the isolator, which has an insertion loss of about 0.5 dB, and the cavitiy 1 and travels to the star point. The other transmitters are on different frequencies, therefore the cavities are tuned to different frequencies too, and the cables transform their impedances to a high impedance at the star point. This let the signal of the transmitter 1 travel to the antenna, attenuated about 1.5 dB by cavity 1 and losses in the cables and the other cavities. The losses in the other cavities depend on the frequency spacing, the coupling and the Q-factors of the cavities. The total loss of the signal in the combining network for the 4 transmitters of our example is typically 2 dB and does not increase significantly if we increase the number of transmitters. Up to 18 transmitters are combined in this way in the UHF-band.

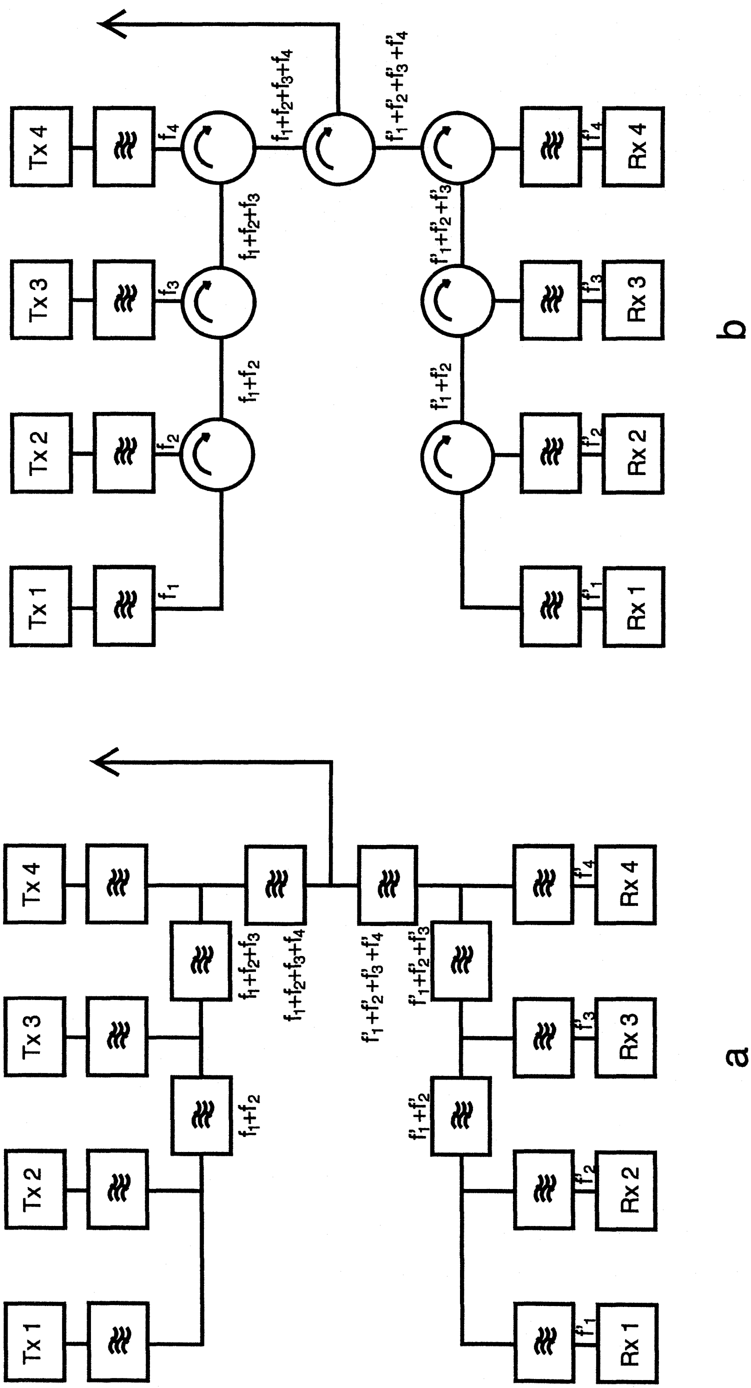


Fig. 32: Combining networks for radio links

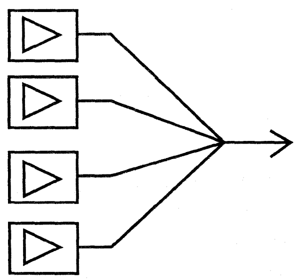
We need the double-isolators to attenuate the signals of the other transmitters leaking through the cavities. Otherwise we would run into intermodulation problems caused by the non-linearity of the final stages of the transmitters.

7.6 Combiner for radio links

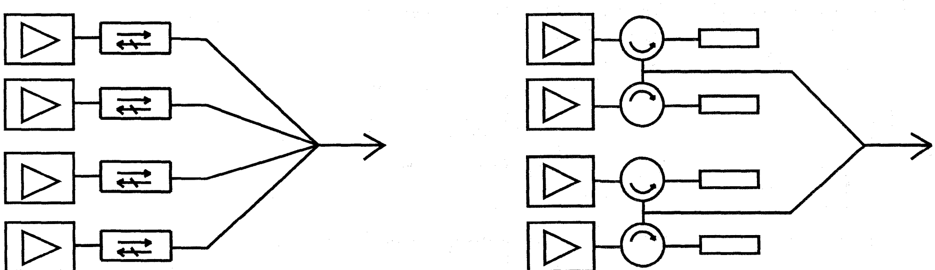
For radio links operating at 2 GHz and higher the combining technique of chapter 6.5 is difficult to realize, for the line length will be very short. Here we find other solutions. Conventionally an array of sharp filters form the combiner for a station of e.g. 4 transmitters and 4 receivers (see figure 32a), resulting in relatively high losses especially for transmitter 1 and receiver 1. Unfortunately tuning of one filter influences the neighbouring ones, making tuning a difficult task.
If we replace some of the filters by circulators (see figure 32b) we can reduce the losses and avoid influencing other filters by tuning. The circulator combining the transmitter branch and the receiver branch has to fulfill stringent requirements for intermodulation. Therefore we should use it only in waveguide systems. In coaxial systems filters are preferred in this stage.

7.7 Combining amplifier stages in a solid-state transmitter

In solid-state transmitters for high power output several transistor amplifiers operate



a



b

c

Fig. 33: Combining amplifier stages in solid state transmitters
a. by a simple star combiner
b. by using isolators
c. by combining isolators

in parallel and have to be combined. To do this with a minimum of losses often star point combiners are used, see figure 33a. But also 3-dB-hybrids can be chosen. In normal operation the transistors see the right load and work well.
But if one of the transistor amplifiers fails a big reflection is transformed to the other amplifiers. If they cannot tolerate this, they will fail too. To avoid this we can use isolators at each amplifier output, see figure 33b.
Another solution is the use of special combining isolators as given in figure 33c. Such a combining isolator consists of two isolators. The amplifiers being combined are connected to the inputs which have an impedance of 50Ω. The output of each isolator has an impedance of 100Ω, and they are connected in parallel. Therefore the output of the combiner has 50Ω again.
For proper operation of all of these combining networks the insertion phase of the amplifiers and isolators or circulators must be equal within ±5 degrees.

7.8 Operation of one-port-amplifiers

If we want to use a one-port-amplifier e.g. varactors, Gunn-amplifiers, masers, we have to construct an input and an output port for the signal being amplified. The only possibility to do it is to use a circulator as given in figure 34. The isolation of the circulator must be higher than the amplification of the amplifier to give stable operation. An isolator between circulator and receiver avoids detoriation by the input impedance of the receiver.

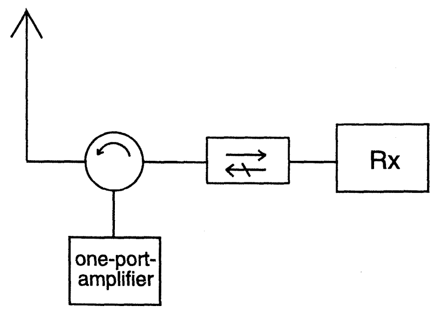


Fig. 34: Operation of a one-port-amplifier

7.9 Locking and priming of oscillators

Oscillators e.g. magnetrons can be stabilized in frequency by a circuit as in figure 35. The signal of a small master oscillator goes through two circulators to the magnetron, and the output power of the magnetron travels through the second circulator to the load or antenna.

For injection locking the frequency of the master oscillator is about the frequency of the magnetron and its power about 30 dB below the level of the magnetron output. The magnetron will lock at the frequency of the master oscillator and will follow it also in phase within certain limits. In case of a pulse magnetron the start up of the pulse is phase correlated to the master oscillator.

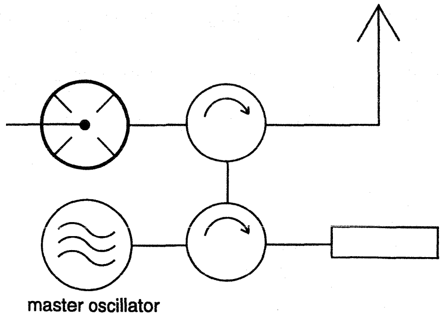


Fig. 35: Circuit for locking and priming of oscillators

Pulse magnetrons are very noisy when starting up at each pulse. We can improve this by "priming": Using the circuit of figure 35 the level of the signal of the master oscillator is about 60 dB below the magnetron output and a bit lower than the magnetron frequency, for magnetrons start up with a slightly lower frequency. This priming signal helps the magnetron to start the oscillation. Therefore the noise is reduced drastically and the shape of the hf pulse improved. For priming it is not necessary to operate the master oscillator in cw, a short pulse covering the leading edge of the magnetron pulse is sufficient.

7.10 Variable attenuator and phase shifter for laboratory use

For the adjustment of a signal to the right level normally we use variable attenuators. But if we do not have the right device in our lab we can use a circulator with a load on one port which can be short circuited by a stub partly or totally, see figure 36. Depending on the length of the stub more or less power is absorbed by the load, the rest travels to the output of the circulator.

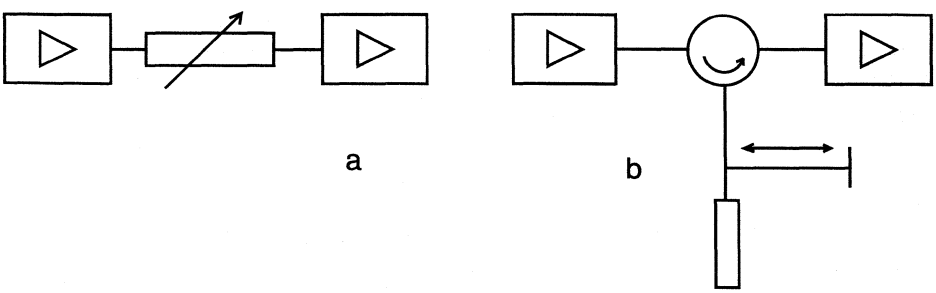


Fig. 36: Adjustment of the level of a signal
a. by a variable attenuator
b. by a circulator with load and stub

For adjusting the phase of a signal normally we use a line stretcher. Instead of that we can use a circulator with a stub on one port, see figure 37. With the length of this stub we can adjust the phase of the signal at the output of the circulator.

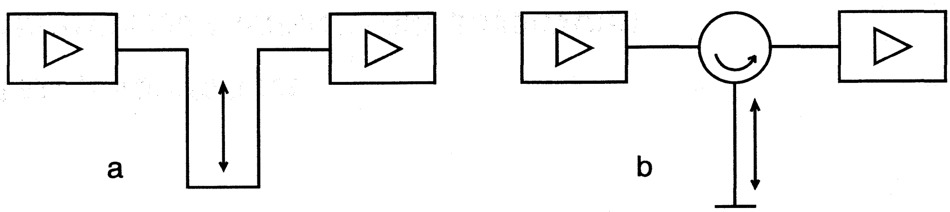


Fig. 37: Adjustment of the phase of a signal
a. by a line stretcher
b. by a circulator and a stub

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BROADCAST AND GENERAL APPLICATIONS

APPLICATION NOTES

Two-stage wideband HF linear amplifier for 400 W PEP using BLW96 and BLW50F

Application note
AN98030

SUMMARY

This report is in three parts, each numbered separately.

Part 1 shows that a wideband power amplifier module providing up to 400 W PEP from 1.6 to 30 MHz can be made using two BLW96 transistors. Operating from a 50 V supply, the IMD at 400 W PEP over the band is better than –26 dB when loaded with a 50 Ω wideband load.

Part 2 describes a suitable drive amplifier using two BLW50F transistors in class A (at the same supply voltage (50 V). The IMD of the drive amplifier is better than –40 dB into a 50 Ω load.

Part 3 describes a complete design in which the driver and main amplifiers are combined using direct inter-stage impedance transformation.

1 PART 1
SINGLE-STAGE WIDEBAND (1.6 – 30 MHz) LINEAR AMPLIFIER FOR 400 W PEP USING TWO BLW96 TRANSISTORS

1 INTRODUCTION

The design of this amplifier was to exploit the performance of the BLW96 in a wideband circuit to provide up to 400 W PEP from 1.6 to 30 MHz.

2 CIRCUIT DESCRIPTION

Figure 1 shows the circuit diagram; Fig.2a shows the circuit board layout, and Figs 2b and 3 show the component lay-out.

It will be noted that baluns are used in input and output circuits. This improves the balance of the collector currents over the frequency range, offsetting any capacitive unbalance in the impedance matching transformers.

Cross neutralisation has been found to be detrimental with these devices, the practical application of neutralisation results in excessive phase changes and results in higher intermodulation distortion over parts of the band.

The input matching network which was designed with aid of a computer program is primarily intended to provide a constant overall gain with frequency and reasonably constant load impedance to a driver circuit.

In practice, a capacitive centre tap (C_4 and C_5) at the secondary of the input impedance matching transformer T_1 is desirable, which is earthed via a 2.2 Ω resistor.

It is preferable in realising C_4 and C_5, to employ three capacitors of 470, 470 and 390 pF in parallel for both, leaving the centre connection such that alternative connections of R_1 can be selected, as shown in Fig.1. This technique allows the best compromise to be found for the intermodulation distortion peaks which typically occur between 14 and 20 MHz, and which can be undesirably high at spot frequencies. A separate, temperature compensated, bias control circuit is necessary to give adjustable constant class-AB bias condition in the BLW96 transistors. The bias circuit diagram is shown in Fig.1.

3 DESIGN DETAILS

To obtain the best performance from the amplifier over the complete range 1.6 – 30 MHz, the quality of the matching transformers used is very important as accurate impedance transformation and low losses are essential. Low losses can be achieved by using toroids of 4C6 material. To obtain accurate matching it is essential to make transformers with very low leakage reactance at 30 MHz combined with sufficient primary inductance at 1.6 MHz (Refs 1 and 2).

3.1 The output transformer

The load impedance required by the transistors is 9.6 Ω, collector to collector. A transformer is required to match to the 50 Ω load. To handle the expected power of 400 W, the transformer must be wound using two 4C6 cores each of 36 × 23 × 15 mm. The best results were obtained using two separate transformers, each on one core, and connecting primary and secondary windings in parallel to give an acceptable value of leakage reactance at 30 MHz.

The complete transformer, wound as detailed in the parts list had a secondary reactance (50 Ω winding) of 200 Ω at 1.6 MHz (20 μH) and a leakage reactance of 50 Ω at f = 30 MHz (265 nH).

3.2 The input transformer

The design impedance of the gain correction network is 5.55 Ω, so a transformer is required to match the input network to a 50 Ω drive source.

The required drive input power assuming a minimum gain of 13 dB is about 20 W which requires two 4C6 toroids 14 × 9 × 5 mm. Again, the best results were obtained by the parallel connection of two transformers each using a separate core.

The complete transformer, wound as detailed in the parts list, had a primary reactance (50 Ω winding) of 220 Ω at 1.6 MHz (22 μH) and a leakage reactance of 50 Ω at 30 MHz (265 nH).

3.3 The bias unit

The circuit uses a BD433 as the temperature sensor and a BD203 emitter follower. The unit can supply a maximum bias current of 800 mA, dependent on the value of resistor in the collector of the BD203. The bias unit should be thermally connected to the amplifier by mounting on the heatsink close to the BLW96s. The collector load resistor (three 17 W wire-wound resistors in parallel) can be mounted separately on stand-off insulators at any convenient part of the heatsink.

3.4 The centre tapped choke

The collector DC supply to each BLW96 is fed via a centre-tapped coil arrangement which consists of a ferrite aerial rod (4A10 grade or equivalent) and has an inductance of 4.6 μH which forms part of the total collector load.

4 PERFORMANCE OF THE AMPLIFIER

4.1 General

The measured performance of the amplifier i.e. intermodulation distortion, gain and input VSWR is given in Figs 4 to 7. A water-cooled heatsink was used for all measurements, and a wideband 50 Ω load was used in conjunction with a thermal power measurement system. The PEP was assumed to be twice the RMS power indicated, ignoring the harmonic content of the output signal.

4.2 Harmonic output

The amplifier was driven with C.W. signals at specific frequencies to 400, 300 and 200 W. The driving signal had a harmonic content lower than –45 dB. Harmonic component measurements are shown in Table 1.

Table 1 Harmomonic output v. frequency

LOAD POWER (W)	TEST FREQUENCY (MHz)	HARMONIC CONTENT (dB)								
		f_2	f_3	f_4	f_5	f_6	f_7	f_8	f_9	f_{10}
400	1.6	−31	−20	−37	−34	−39	−44	−43	−46	−52
	3.5	−36	−21	−45	−34	−63	−40	−48	−49	−47
	7	−38	−17	−47	−29	−45	−34	−64	−64	
	10	−45	−15	−45	−29	−50				
	14	−39	−16	−45	−46					
	20	−48	−24	−50	−44					
	28	−44	−41							
300	1.6	−31	−21	−39	−33	−40	−47	−43	−46	−52
	3.5	−36	−23	−45	−32	−65	−42	−48	−52	−49
	7	−40	−22	−52	−30	−48	−38	−65	−64	
	10	−48	−16	−45	−29	−50				
	14	−42	−18	−48	−47					
	20	−42	−25	−50	−46					
	28	−45	−42							
200	1.6	−32	−22	−40	−33	−42	−49	−44	−47	−55
	3.5	−35	−24	−46	−33	−65	−43	−50	−53	−50
	7	−40	−23	−62	−30	−59	−39	−65	−64	
	10	−50	−19	−45	−30	−50				
	14	−44	−19	−47	−47					
	20	−38	−27	−49	−47					
	28	−44	−42							

4.3 Collector efficiency

The collector efficiency varies over the band, and as the output matching was designed for 400 W, reduced efficiency is apparent at reduced levels of output. Typical efficiencies are:

Two-tone signals between 1.6 and 30 MHz

PEP LOAD (W)	BEST COLLECTOR EFFICIENCY (%)	WORST COLLECTOR EFFICIENCY (%)
400	50	37.7
300	44	32

Taking the worst case and assuming equal sharing and zero circuit losses, each transistor would dissipate 170 W.

C.W. signals between 1.6 and 30 MHz

P LOAD (W)	BEST COLLECTOR EFFICIENCY (%)	WORST COLLECTOR EFFICIENCY (%)
400	65.5	47.5

Taking the worst case and assuming equal sharing and zero circuit losses, each transistor would dissipate 220 W.

The published RF thermal resistance of the BLW96 is 0.65 K/W (junction-heatsink) and the maximum permissible junction temperature is 200 °C. Therefore the maximum possible heatsink temperature for continuous C.W. operation is 200 – (220 × 0.65) = 57 °C.

5 BIAS ADJUSTMENT

The zero signal collector currents should be adjusted by the bias potentiometer to 2 × 100 mA when operating from a 50 V supply.

6 CONCLUSIONS

- A single stage amplifier using 2 × BLW96s in class-AB can deliver up to 400 W PEP with intermodulation distortion better than –26 dB over the band 1.6 – 30 MHz.
- Measurements indicate that when used under C.W. conditions at the frequencies where the maximum collector dissipations occurs, the devices should be capable of operation with heatsink temperatures up to 57 °C.

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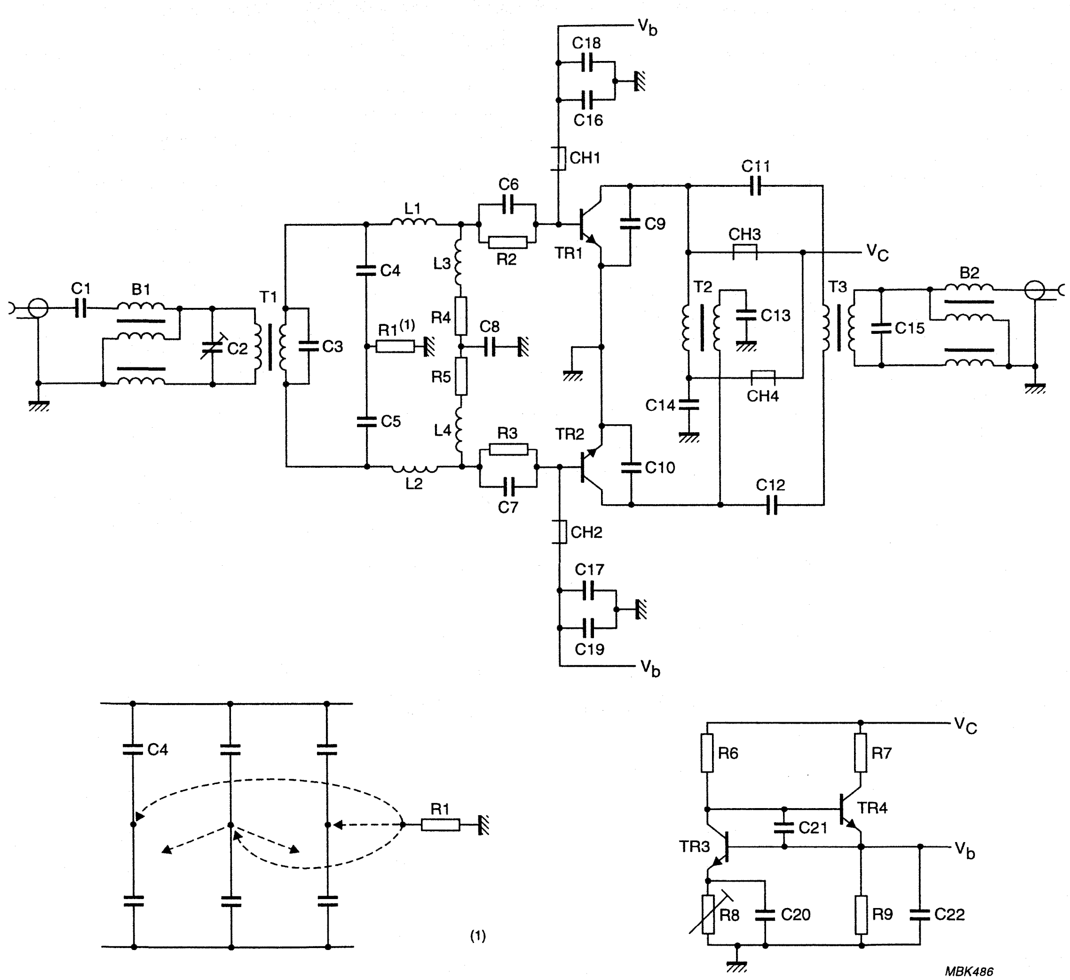


(1) See note in Chapter 2.

Fig.1 Circuit diagram of BLW96 power amplifier for 1.6 – 30 MHz, 400 W PEP, see Table 2 for parts list.

Table 2 Parts list for Fig.1

Transistors and resistors			
TR1 = TR2	BLW96		
TR3	BD433		
TR4	BD203		
R1	2.2 Ω	CR 37, ±5%	2322 212 13228
R2 = R3	18 Ω	PR 37, ±5%	2322 191 31809
R4 = R5	2 × 12 Ω, in parallel	PR 37, ±5%	2322 191 31209
	2 × 15 Ω, in parallel	PR 37, ±5%	2322 191 31509
R6	1.5 kΩ	PR 37, ±5%	2322 191 31502
R7	3 × 180 Ω, in parallel	EH 15, ±5%	2306 330 03181
R8	3.3 Ω adjustable	TPW22	2322 011 02338
R9	22 Ω	CR 37, ±5%	2322 212 13229
Capacitors			
C1	10 nF	polyester, ±20%	2222 342 44103
C2	60 pF	trimmer	2222 809 08003
C3	330 pF, in parallel	polystyrene, ±1%	2222 426 43301
	300 pF, in parallel		2222 426 43001
C4 = C5	2 × 470 pF, in parallel	polystyrene, ±1%	2222 426 44701
	1 × 390 pF, in parallel		2222 426 43901
C6 = C7	2 × 1 000 pF, in parallel	polystyrene, ±1%	2222 426 44102
	1 × 820 pF, in parallel		2222 426 48201
C8	3 × 100 nF, in parallel	polyester, ±20%	2222 342 44104
C9 = C10	2 × 47 pF, in parallel	ceramic, ±2%	2222 650 34479
	2 × 56 pF, in parallel		2222 650 34569
C11 = C12	5 × 10 nF, in parallel	polyester, ±20%	2222 342 44103
C13 = C14	3 × 100 nF, in parallel	polyester, ±20%	2222 342 44104
C15	33 pF	ceramic, ±2%	2222 650 34339
C16 = C17	3.3 μF	±10%	2222 344 21335
C18 = C19	220 μF	4 V, electrolytic	2222 016 2221
C20 = C21	100 nF	polyester, ±20%	2222 342 44104
C22	220 μF	10 V, electrolytic	2222 016 4221
Inductors			
L1 = L2	12.9 nH; consists of ¾ turn of 1.3 mm Cu wire 5 mm diameter		
L3 = L4	21 nH; consists of 1 turn of 1.3 mm Cu wire 7.5 mm diameter		
Ch1 = Ch2	2.5 turns through 6 hole ferrite bead grade 3B		4312 020 31500
Ch3 = Ch4	3 parallel turns through 6 hole bead grade 3B		4312 020 31500

Transformers	
T1	Two transformers with parallel connected primary and secondary windings. Each transformer wound on 4C6 toroids 14 × 9 × 15 mm, (4322 020 91020). Primary winding consists of 10 turns of copper tape approximately 1.5 mm wide. Secondary winding consists of 30 turns of 0.45 mm chain enamelled Cu wire. Windings separated by a layer of PTFE tape approximately 0.025 mm thick.
T2	4 turns of 2 × 1.0 mm enamelled Cu wire twisted, on a 50 mm length of 4A10 or equivalent grade aerial rod 10 mm diameter, (4311 020 55390).
T3	Two transformers with parallel connected primary and secondary windings. Each transformer wound on 4C6 toroids 36 × 23 × 15 mm, (4322 020 91090). Primary winding consists of 6 turns copper tape 8.0 mm wide. Secondary winding consists of 14 turns of 4 × 0.5 mm diameter Cu wire in parallel. Windings separated by a layer of PTFE approximately 0.025 mm thick.
B1	11 turns of 50 Ω co-axial cable approximately 3 mm external diameter with PTFE dielectric and 11 turns of 0.5 mm enamelled Cu wire wound on 4C6 toroid 23 × 14 × 7 mm, (4322 020 91070).
B2	8 turns of 50 Ω co-axial cable approximately 4 mm external diameter with PTFE dielectric and 8 turns of 1 mm enamelled Cu wire wound on two 4C6 toroids 36 × 23 × 15 mm, (4322 020 91090).

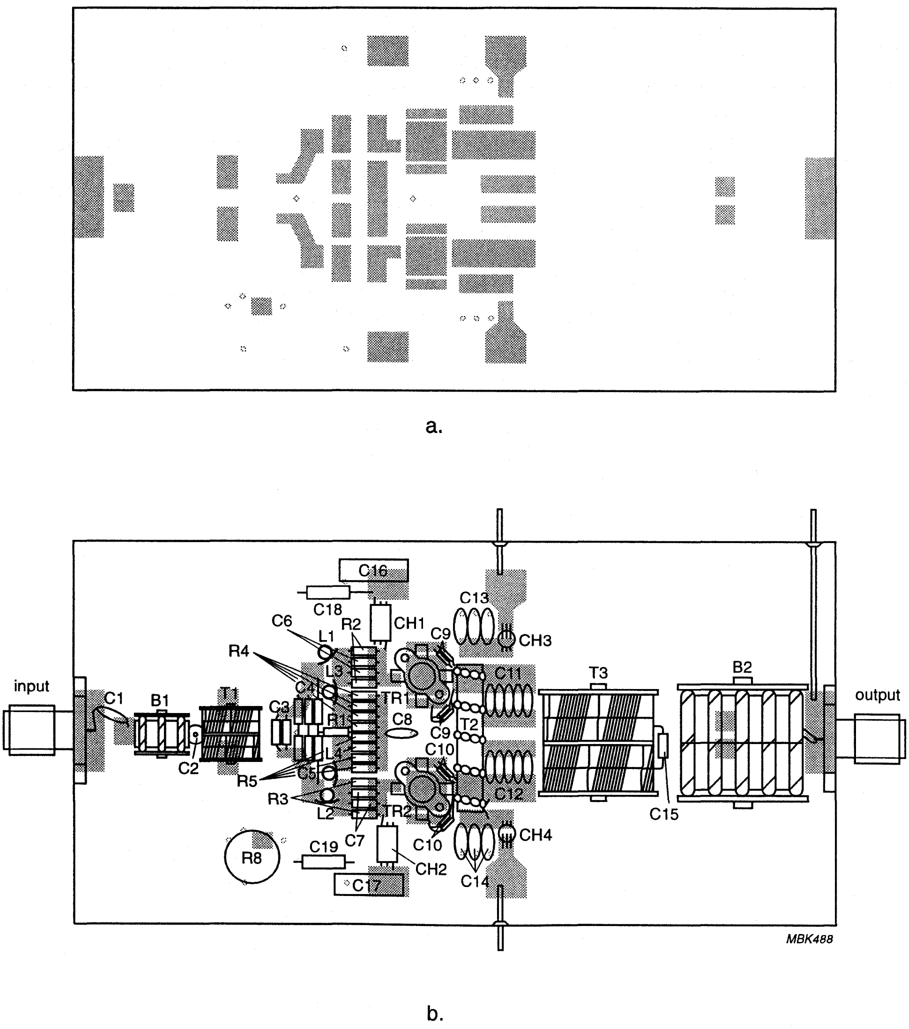


Fig.2 BLW96 power amplifier circuit board (a) and component lay-out (b).

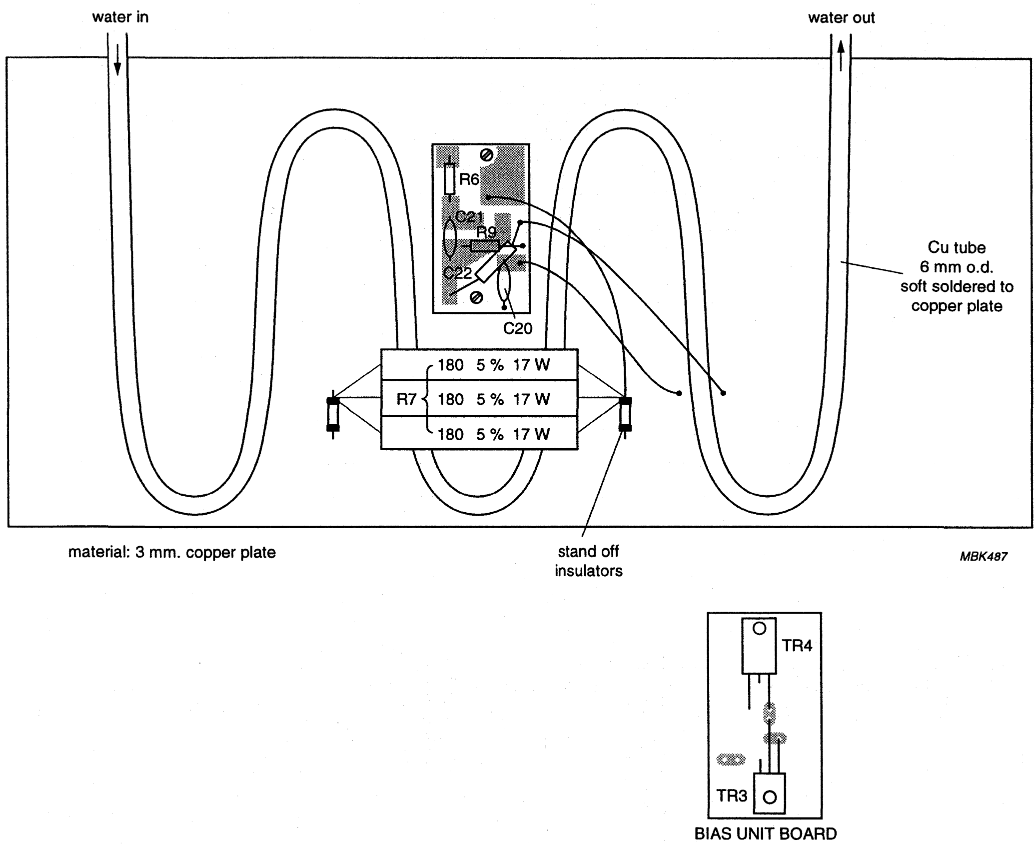


Fig.3 BLW96 power amplifier component lay-out, underside of heatsink.

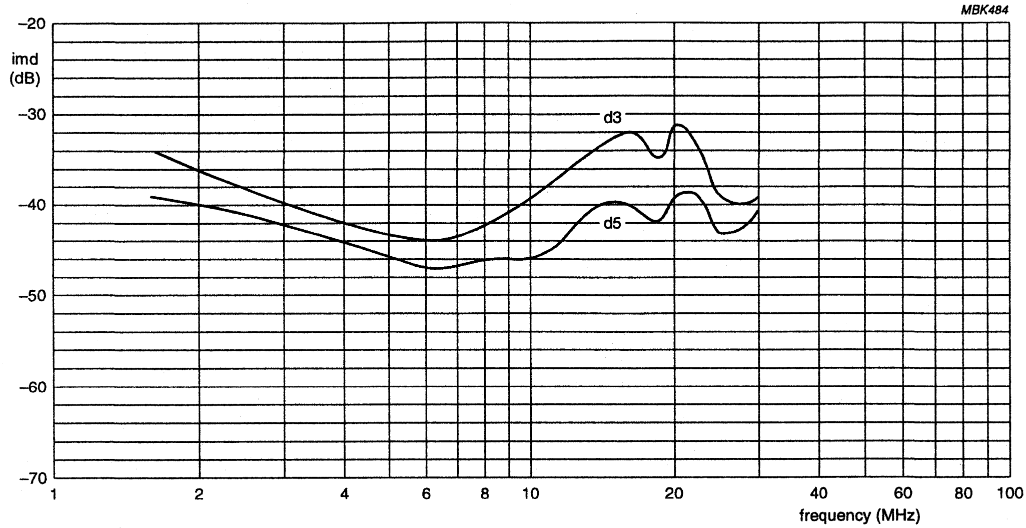


Fig.4 Intermodulation performance of BLW96 amplifier at 200 W PEP.

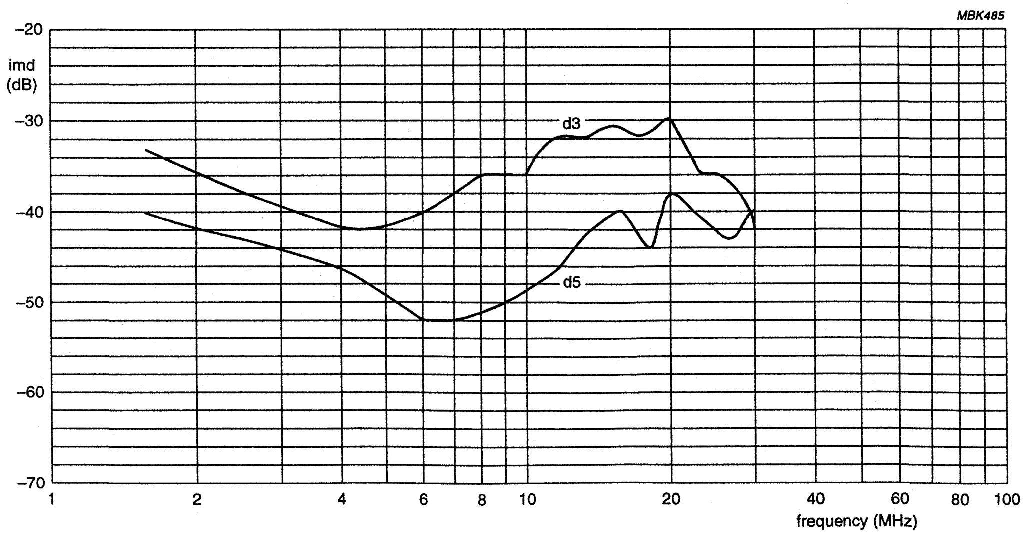


Fig.5 Intermodulation performance of BLW96 amplifier at 300 W PEP.

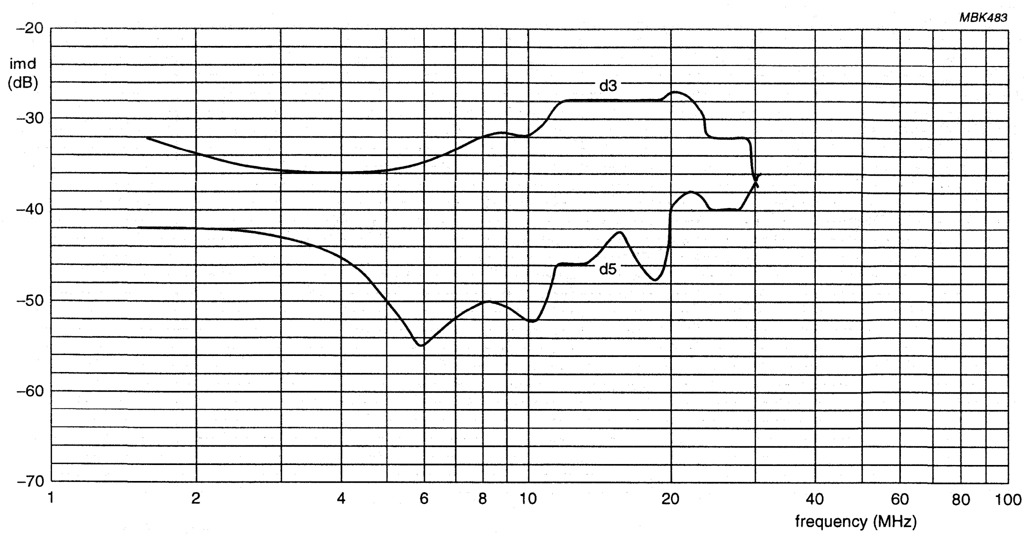


Fig.6 Intermodulation performance of BLW96 amplifier at 400 W PEP.

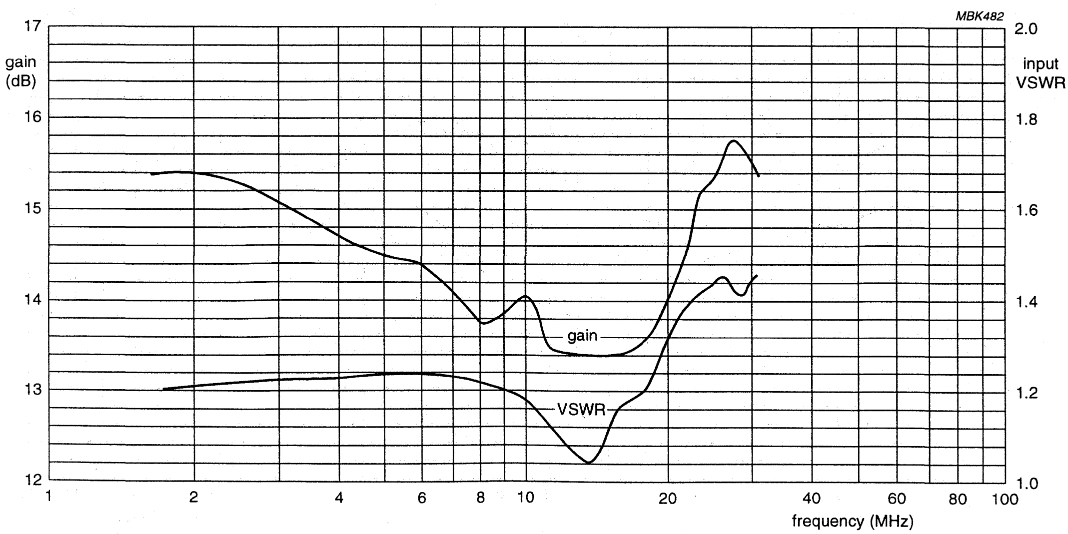


Fig.7 Gain and input VSWR of BLW96 at 400 W C.W.

2 PART 2
A SINGLE-STAGE WIDEBAND (1.6 – 30 MHz) LINEAR AMPLIFIER FOR 25 W PEP USING BLW50F TRANSISTORS IN CLASS A

1 INTRODUCTION

This amplifier was developed to drive a 400 W linear amplifier using BLW96 transistors in class AB and to provide data for future development of a two stage amplifier for the same power with both driver and p.a. stages working from a nominal 50 V supply.

The driver amplifier described herein was designed to give 25 W PEP into a 50 Ω load sufficient to drive the amplifier described in Chapter 2. Class A operation is necessary because the required intermodulation distortion of the driver circuit alone should be substantially less than that of the p.a., the driver circuit distortion being somewhat degraded when working into the non-linear input impedance of the p.a. A target figure of intermodulation products < –40 dB over the frequency band 1.6 to 30 MHz was therefore required.

As with the BLW96 p.a., 50 Ω input and output impedances were assumed initially, but direct inter-stage impedance matching is used in the two stage amplifier which will be reported subsequently.

2 GENERAL CIRCUIT DESCRIPTION

The circuit diagram of the amplifier is given in Fig.8, and follows conventional class-A push-pull linear HF amplifier design practice.

Some shunt and series feedback is applied: the shunt feedback resistors are also used to determine bias conditions.

The design and construction of the broadband input and output impedance matching transformers is critical in overall amplifier performance.

Details of these and other construction features are given in Chapter 3.

3 DESIGN AND CONSTRUCTION

3.1 Bias condition

In the design of linear class-A amplifiers, in order to arrive at the best intermodulation performance, a suitable starting point is to assume maximum bias current and voltage permitted by the maximum anticipated heatsink temperature.

In this design, therefore, a practical maximum operating heatsink temperature of 70 °C was assumed. At this heatsink temperature, the practical bias conditions for the BLW50F of V_{CE} = 44 V, I_C = 1 A are permissible.

Note that the BLW96 amplifier of Part 1 shows a worst case gain of about 13.5 dB and a worst case VSWR of about 1.45 (these two conditions do not occur at the same frequency however). But, conservatively, we may say that a suitable driver should be capable of about 18.7 W in a 50 Ω load.

In addition, if this power (18.7 W) is to be available at intermodulation products d3, d5, < –40 dB, experience has shown that the maximum available power from the amplifier (class A) into a linear resistive load should approach 35 W, at which power intermodulation products will of course exceed –40 dB.

Further, with the circuit configuration chosen (Fig.8), it will be seen that appreciable power is dissipated in the shunt feedback resistors.

We expect about 15% of the available power will be so dissipated; therefore the maximum available power requirement becomes about 40 W from the transistors.

The projected initial bias conditions, V_{CE} = 44 V, I_C = 1 A correspond to a collector dissipation of 44 W per transistor. Under class-A operation, the maximum output power would then be 22 W per transistor, 44 W total.

There is therefore some margin compared with the estimated capability requirement of 35 W and this is reasonable, in part because some further degradation of intermodulation performance may be expected when directly driving into the somewhat non-linear input impedance of the p.a., instead of the linear, non reactive design load (50 Ω).

Having chosen V_{CE} = 44 V, a further voltage drop of 2 V may be assumed across the external emitter resistor for bias stabilisation.

3.2 Components and lay-out

Figure 9 gives details of the circuit board and component lay-out. The parts list in Table 3 includes details of wound components including the two wideband matching transformers.

A suitable heatsink must be provided, sufficient to limit the junction temperature to <200 °C under DC (bias) conditions.

The total current required at 46 V is about 2.25 A, which includes base bias current flowing in the feedback resistors.

The total dissipation of the BLW50F transistors is, however approximately 44 × 2 = 88 W.

The feedback resistors and external emitter resistors together dissipate a further 14 W approximately.

If these resistors are mounted so that they do not contribute to the heatsink surface temperature close to the transistors, then the required heatsink thermal resistance, $\theta_{h\text{-}amb}$, which determines a heatsink temperature of 70 °C in a 25 °C laboratory ambient, for example is given by: $\theta_{h\text{-}amb} \leq \frac{70-25}{88}$

i.e. <0.51 °C/W.

To obtain the best compromise between input VSWR and gain, particularly between 26 and 30 MHz, C_2 is made adjustable; this accommodates the inevitable spread of leakage reactance of the input transformer T_1.

Similarly, to allow for leakage reactance spreads in T_2, C_3 is also made adjustable.

4 AMPLIFIER PERFORMANCE

Figures 10 and 11 show the measured amplifier performance.

Figure 11 shows 3rd and 5th order intermodulation products relative to the amplitude of each tone (6.25 W) under standard 2-tone drive conditions.

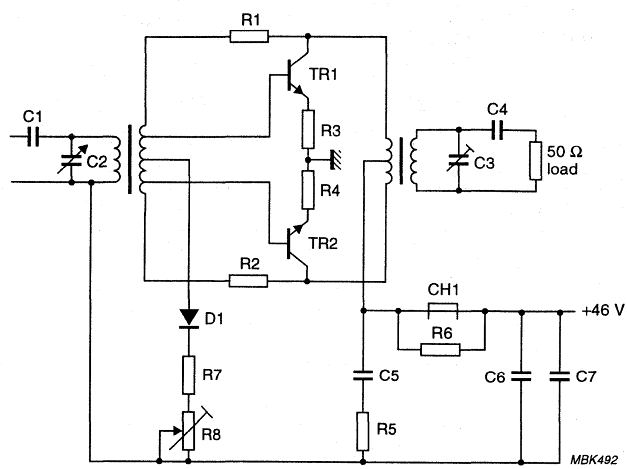
Figure 10 shows amplifier gain and input VSWR under single tone drive at P_{load} = 25 W.

Note that d_3 is substantially < −40 dB over the frequency range of interest; the minimum gain and worst case VSWR are 15.7 dB, 1.36 respectively, both occurring at the lower frequencies.

5 CONCLUSIONS

A wideband linear HF amplifier has been designed and constructed, using BLW50F transistors in class A which can give up to 25 W PEP over the band 1.6 to 30 MHz with 3rd and 5th order intermodulation better than −40 dB between 2 and 28 MHz.

Amplifier gain and input VSWR are better than 15.7 dB and 1.4:1 respectively over the frequency range. The amplifier should be suitable to drive a further linear amplifier using BLW96s in class AB to 400 W PEP.



D1 = BY206;
TR1, TR2 = BLW50F.

Fig.8 Circuit diagram of 25 W linear amplifier.

Table 3 Parts list for Fig.8

Resistors			
R1 = R2	2 × 200 Ω, in series	PR52, ±5%	2322 192 32001
R3 = R4	5 × 12 Ω, in parallel	CR25, ±5%	2322 211 13129
R5	6.8 Ω	CR25, ±5%	2322 211 13688
R6	22 Ω	CR37, ±5%	2322 211 13229
R7	15 Ω	CR25, ±5%	2322 211 13159
R8	3.3 Ω, adjustable	TPW22	2322 011 02338
Capacitors			
C1 = C4	10 nF	polyester, ±20%	2222 352 44103
C2 = C3	60 pF	trimmers	2222 809 08003
C5	22 nF	polyester, ±20%	2222 352 44223
C6 = C7	2 × 47 nF, in parallel	polyester, ±20%	2222 352 44473
Transformers			
T1	1 : 1.5 turns ratio, wound on twin hole bead Philips grade 4B1, (4312 020 31525). Primary 4 turns of 2 × 0.45 mm enamelled Cu wire in parallel, tapped at centre and 2 × 1 turn from centre.		
T2	1 : 1.4 turns ratio, wound on a Philips 4C6 toroid 23 × 14 × 7 mm, (4322 020 91070). Primary 22 turns of 2 × 0.45 mm enamelled Cu wire centre tapped. Secondary 16 turns of copper tape approx. 1.5 mm wide. Primary wound on top of secondary winding and insulated by PTFE tape approximately 0.025 mm thick.		
Ch1	2.5 turns on 6 hole bead grade 3B, (4312 020 31500).		

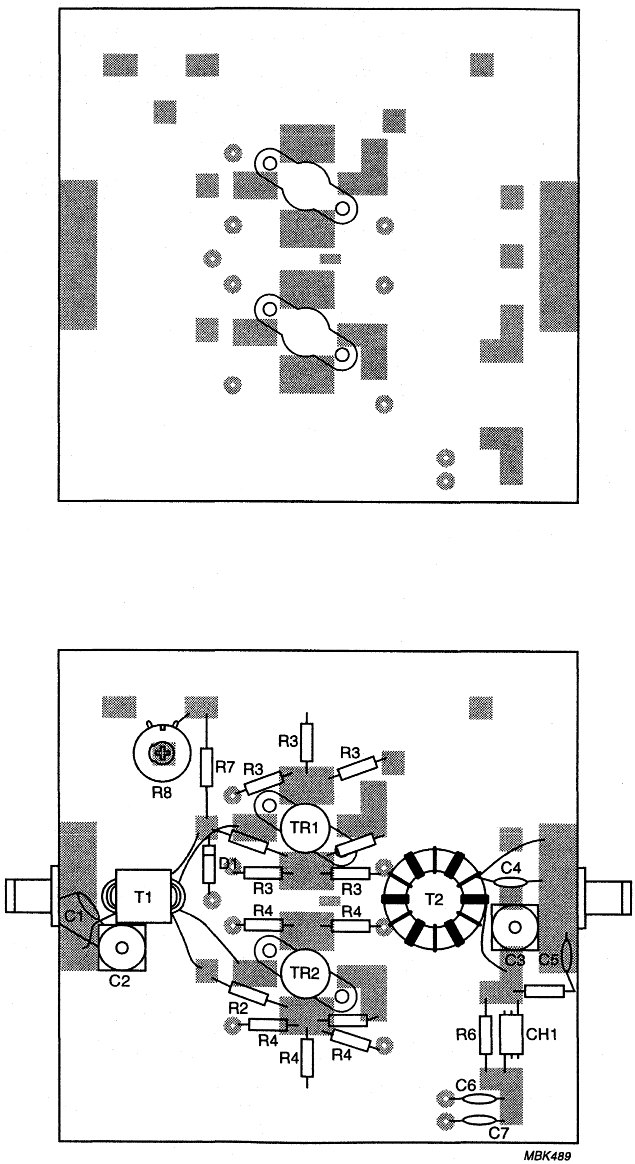


Fig.9 Printed circuit board and lay-out.

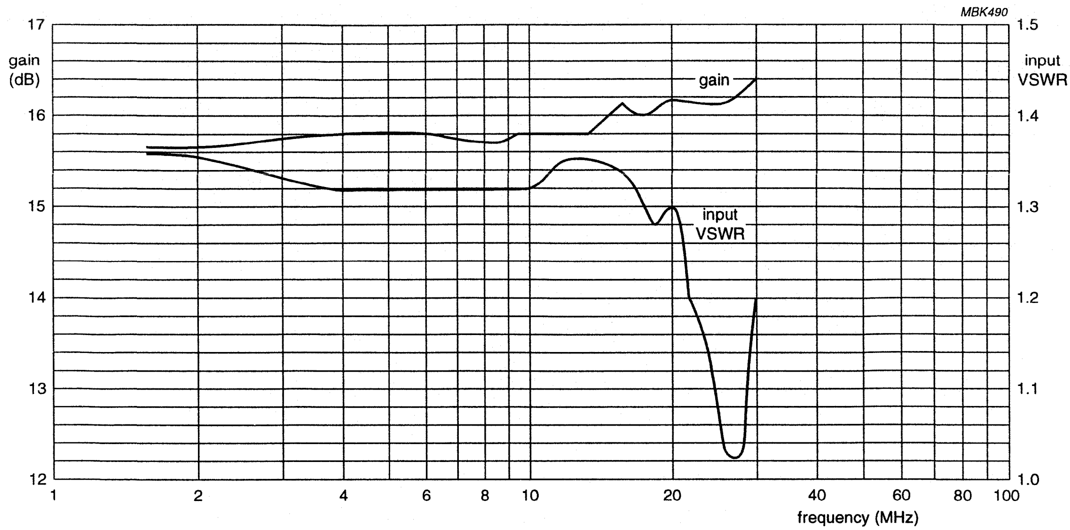


Fig.10 BLW50F linear amplifier gain and input VSWR versus frequency.

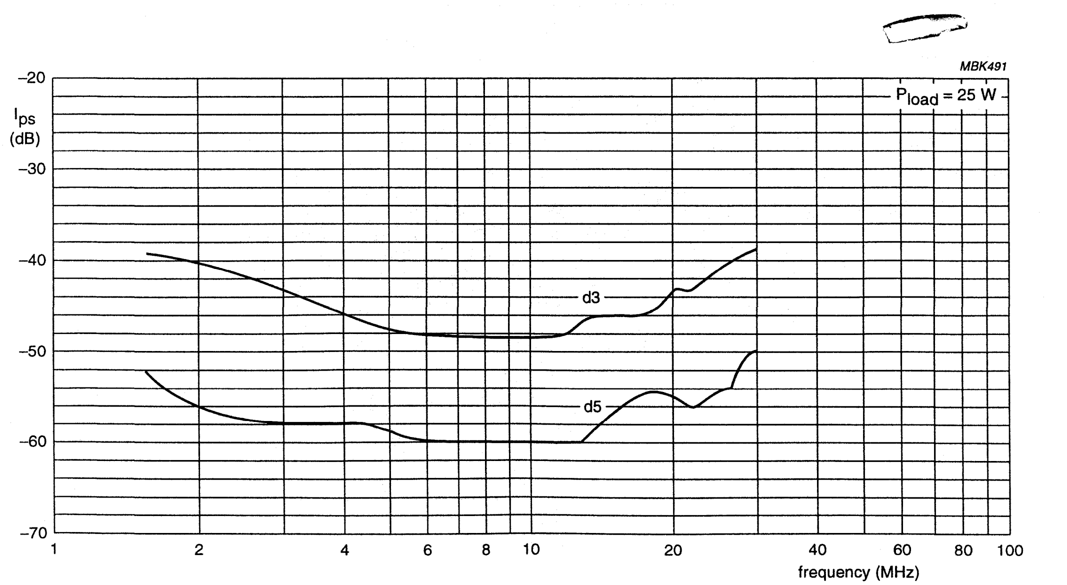


Fig.11 BLW50F linear amplifier-intermodulation products versus frequency.

3 PART 3
A TWO-STAGE WIDEBAND H.F. LINEAR AMPLIFIER FOR 400 W PEP USING TWO BLW96 AND BLW50F TRANSISTORS

1 INTRODUCTION

It has been shown in Part 1 that two BLW96 transistors in a wideband class-AB push-pull amplifier can give 400 W PEP under two-tone drive with intermodulation products < –26 dB in the band 1.6 – 30 MHz.

Part 2 described a suitable drive amplifier using two BLW50F transistors in class-A at the same supply voltage (50 V nominal). The intermodulation performance of the drive amplifier is < –40 dB into a 50 Ω load.

The two amplifiers have been combined using direct inter-stage impedance transformation and the overall design is described here in Part 3.

2 CIRCUIT DESCRIPTION

The circuit diagram of the complete amplifier is shown in Fig.12.

Standard design practice for the individual BLW96 and BLW50F push-pull linear amplifiers has been closely followed. The differences are:

1. Direct impedance matching between the driver stage output (100 Ω) and the p.a. input (5.5 Ω).
2. Replacement of adjustable capacitors by fixed-value capacitors, because it is considered impractical to have the complication of adjustments in a two-stage circuit.

   The fixed capacitors are chosen to compensate for leakage reactance of cricital transformers towards the higher frequency limit of the band, assuming good winding and mounting technique.
3. Omission of the balun and adjustable centre-tap arrangement in the p.a. input circuits, which are unnecessary with balance provided by a push-pull driver.

3 CONSTRUCTIONAL DETAILS

Figure 14 shows the printed circuit board and component layout.

Figure 15 shows the general arrangement of a water-cooled copper heatsink on the underside of which the temperature compensated p.a. bias unit is mounted.

The parts list (Table 5) includes winding instructions and inductors and transformers.

4 AMPLIFIER PERFORMANCE

The separate performance of the basic driver and p.a. circuits with 50 Ω terminations is summarised below

	DRIVER	P.A.
Bias		
V_{CE}	44 V	50 V
I_C	2 × 1 A	2 × 100 mA (zero signal)
Single tone 1.6 – 30 MHz		
P_L	25 W	400 W
Gain		
(mid band)	15.8 dB	13.4 dB
(min., max.)	15.7 dB, 16.4 dB	13.4 dB, 15.8 dB
Input VSWR		
(mid band)	1.35 : 1	1.1 : 1
(max)	1.36 :1	1.45 : 1
Two tone 1.6 – 30 MHz		
P_L (PEP)	25 W	400 W
Efficiency		37.7% (min)
3rd order intermodulation		
(mid band)	–46 dB	–28 dB
(max)	–39 dB	–27 dB

4.1 GAIN, VSWR and INTERMODULATION

The overall performance of the two stage amplifier is shown in Figs 16 to 20.

Figure 16 shows gain and input VSWR under single tone drive with 50 V supply and P_{load} = 400 W. Minimum gain and VSWR are seen to be 25 dB and 2 : 1 respectively. Figures 17 to 19 show 3rd and 5th order intermodulation under two tone drive conditions with 50 V supply and P_{load} 200, 300 and 400 W PEP.

It is seen that at 400 W PEP, $d_3 < -26$ dB, and at 300 W PEP, $d_3 < -30$ dB.

In addition, Fig.20 shows intermodulation performance at 300 W PEP, but with 45 V supply. It is seen that d_3 is still < -30 dB.

4.2 Harmonic content

The amplifier was driven to 400 W C.W. and the amplitude of the harmonics measured relative to the fundamental signal in the wideband load.

Table 4

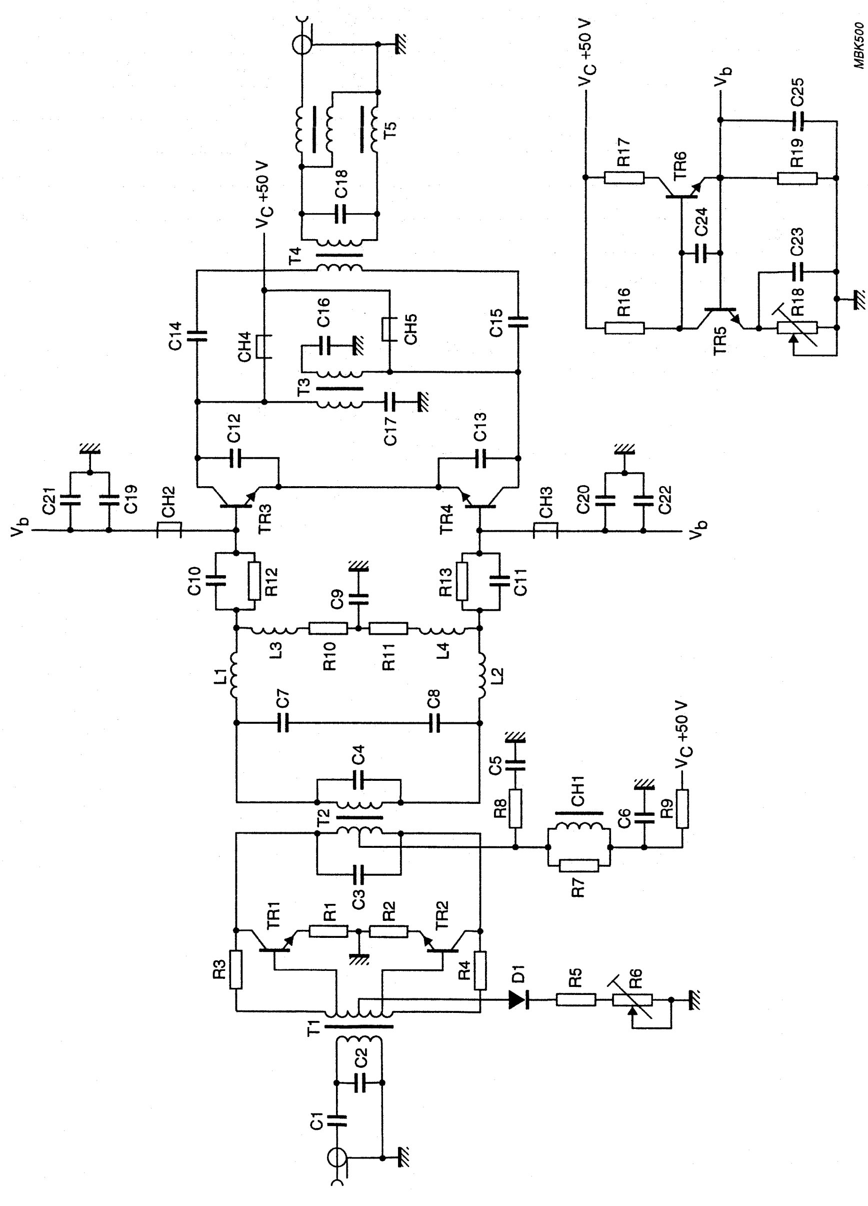
TEST FREQUENCY (MHz)	f_2 (dB)	f_3 (dB)	f_4 (dB)	f_5 (dB)	f_6 (dB)	f_7 (dB)	f_8 (dB)	f_9 (dB)	f_{10} (dB)
1.6	−46	−19	−56	−34	−48	−48	−50	−45	−59
3.5	−45	−19	−50	−33	−58	−44	−56	−45	−60
7	−54	−18	−50	−29	−48	−40			
10	−48	−17	−45	−32	−55	−50			
14	−43	−16	−50	−44					
20	−34	−25							
28	−40	−45							

5 CONCLUSION

A wideband linear HF amplifier has been designed using BLW96 output and BLW50F driver transistors. The overall amplifier gain is in the range 25 – 29 dB over the band 1.6 – 30 MHz and the input VSWR is less than 2:1.

When operated at 400 W PEP, the (2-tone) intermodulation products are < −26 dB.

An intermodulation product of < −30 dB may be obtained at 300 W PEP even with the supply rail reduced to 45 V.



L1, L2 = 1 turn 1.3 mm Cu wire 5 mm dia.
L3, L4 = 1 turn 1.3 mm Cu wire 7.5 mm dia.

Fig.12 Circuit diagram of the complete amplifier.

Table 5 Parts list for Fig.12

Resistors			
R1, R2	5 × 12 Ω, in parallel	CR25, ±5%	2322 211 13129
R3, R4	2 × 200 Ω, in series	PR52, ±5%,	2322 192 32001
R5	15 Ω	CR25, ±5%	2322 211 13159
R6 = R18	3.3 Ω, adjustable	TPW22	2322 011 02338
R7 = R14 = R15	22 Ω	CR25, ±5%	2322 211 13229
R8	6.8 Ω	CR25, ±5%	2322 211 13688
R9	1.8 Ω	AC10, ±10%	2322 329 10188
R10 = R11	18 Ω	PR37, ±5%	2322 212 31209
R12 = R13	2 × 12 Ω, in parallel	PR37, ±5%	2322 212 31209
	2 × 15 Ω, in parallel		2322 212 31509
R16	1.5 kΩ	PR37, ±5%	2322 212 31502
R17	3 × 180 Ω, in parallel	EH15, ±5%	2322 330 03181
R19	22 Ω	CR37, ±5%	2322 212 13229
Capacitors			
C1 = C23 = C24	10 nF	polyester, ±20%	2222 352 44103
C2	39 pF	ceramic, ±2%	2222 632 10399
C3	27 pF	ceramic, ±2%	2222 632 10279
C4	680 pF	polystyrene, ±2%	2222 426 6801
C5	22 nF	polyester, ±20%	2222 352 44223
C6	2 × 47nF, in parallel	polyester, ±20%	2222 352 42473
C7 = C8	2 × 470 pF, in parallel	polyester, ±2%	2222 426 4701
	1 × 390 pF, in parallel	polyester, ±2%	2222 426 3901
C9 = C10	2 × 1000 pF, in parallel	polyester, ±2%	2222 426 1002
	1 × 820 pF, in parallel	polyester, ±2%	2222 426 8201
C11	100 nF	polyester, ±20%	2222 352 44104
C12 = C13	2 × 47 pF, in parallel	ceramic, ±2%	2222 632 34479
	2 × 56 pF, in parallel	ceramic, ±2%	2222 632 34569
C14 = C15	5 × 10 nF, in parallel	polyester, ±20%	2222 352 44103
C16 = C17	3 × 100 nF, in parallel	polyester, ±20%	2222 352 54104
C18	60 pF	trimmer	2222 809 08003
C19 = C20	3.3 µF	polyester, ±10%	2222 344 21335
C21 = C22	220 µF	4 V, electrolytic	2222 016 2221
C25	220 µF	10 V, electrolytic	2222 016 4221
Inductors			
Ch1 = Ch2 = Ch3	2.5 turns through 6 hole ferrite bead grade 3B		4312 020 31500
Ch4 = Ch5	3 parallel loops through 6 hole ferrite bead grade 3B		4312 020 31500
L1 = L2	13.9 nH; see diagram on Fig.12		
L3 = L4	21 nH; see diagram on Fig.12		

Transformers	
T1	1:1.5 turns ratio, wound on twin hole bead Philips grade 4B1 (4312 020 31525). Primary: 4 turns of 2 × 0.45 mm enamelled Cu wire in parallel. Secondary: 6 turns of 2 × 0.45 mm enamelled Cu wire in parallel tapped at centre and at 2 × 1 turns from centre. See Fig.13. Typical primary reactance at f = 1.6 MHz = (secondary o/c) = j160, typical leakage reactance at f = 30 MHz = (secondary s/c) = j25.
T2	4.5 : 1 turns ratio. Consists of two transformers with primary and secondary windings connected in parallel, each wound on twin hole bead Philips grade 4B1 (4312 020 31500). Primary winding 9 turns 0.45 mm enamelled Cu wire centre tapped. Secondary 2 turns of 2 × 0.45 mm enamelled Cu wire in parallel. Typical primary reactance of combination at f = 1.6 MHz (secondary o/c) = j400. Typical leakage reactance of combination at f = 30 MHz (secondary s/c) = j90.
T3	The centre tapped choke, wound on a 50 mm length of 4A10 aerial rod (or equivalent), (4311 020 55390), 4 turns of twisted enamelled Cu wire 1.0 mm, typical total reactance at f = 1.6 MHz = j40.
T4	2.33 : 1 turns ratio, consists of two transformers with primary windings and secondary windings connected in parallel, each wound on 4C6 toroids 36 × 23 × 15 mm (4322 020 91090). Primary winding 6 turns of Cu tape 8 mm wide. Secondary winding 14 turns of 4 × 0.5 mm enamelled Cu wire in parallel. Windings are separated by PTFE tape approximately 0.25 mm thick. Typical primary reactance of combination at f = 1.6 MHz (primary o/c) = j200. Typical leakage reactance of combination at f = 30 MHz (primary s/c) = j50.
T5	Output balun transformer. Wound on two 4C6 toroids 36 × 23 × 15 mm, (4322 020 91090), with 8 turns of 50 Ω coaxial cable having PTFE insulation and approximately 4 mm external diameter and 8 turns of 1 mm enamelled Cu wire for the balancing winding - see diagram

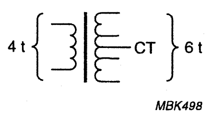


Fig.13 Transformer T_1.

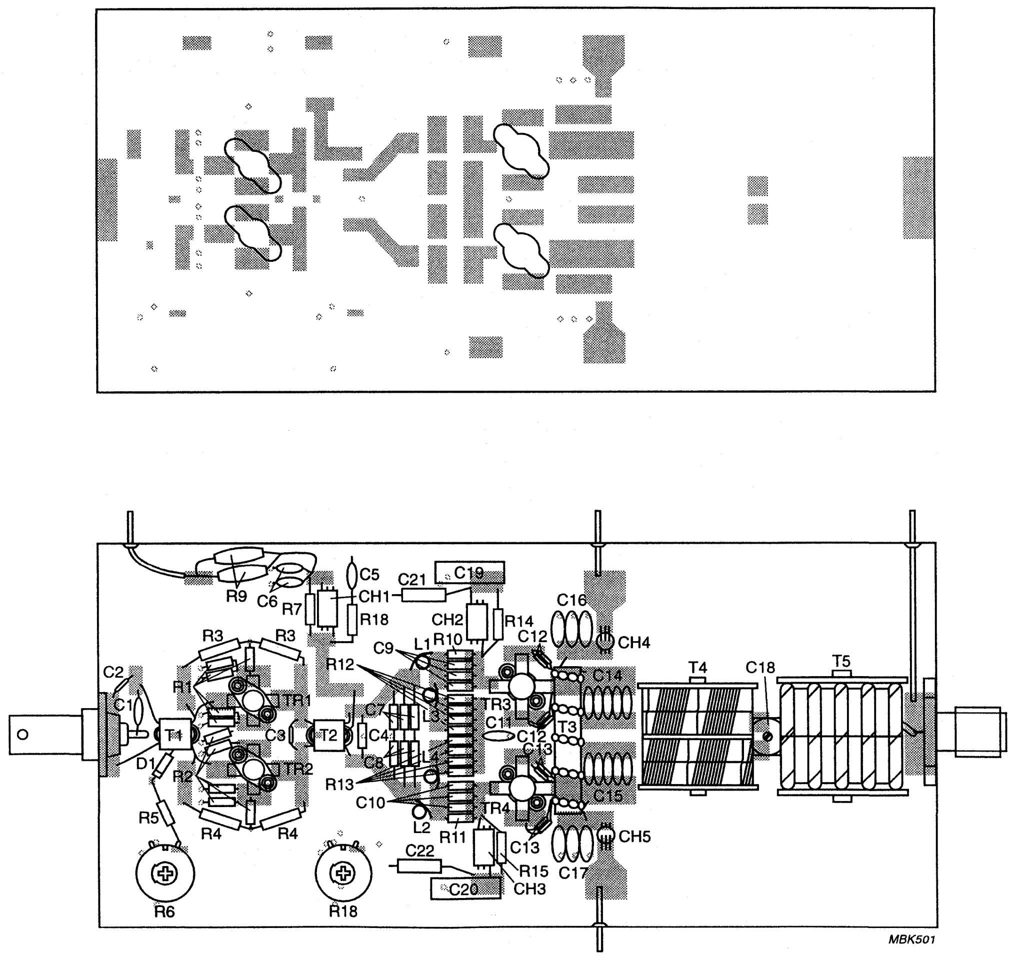


Fig.14 Printed circuit board and lay-out.

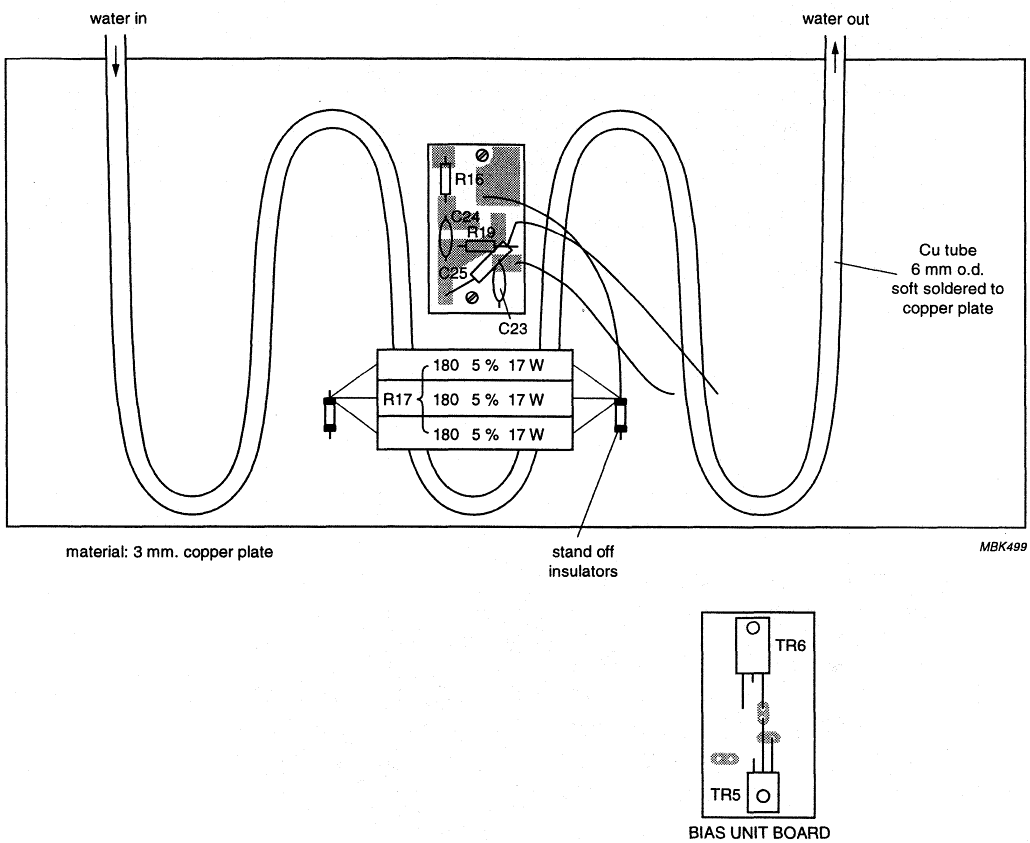


Fig.15 Water cooled heatsink.

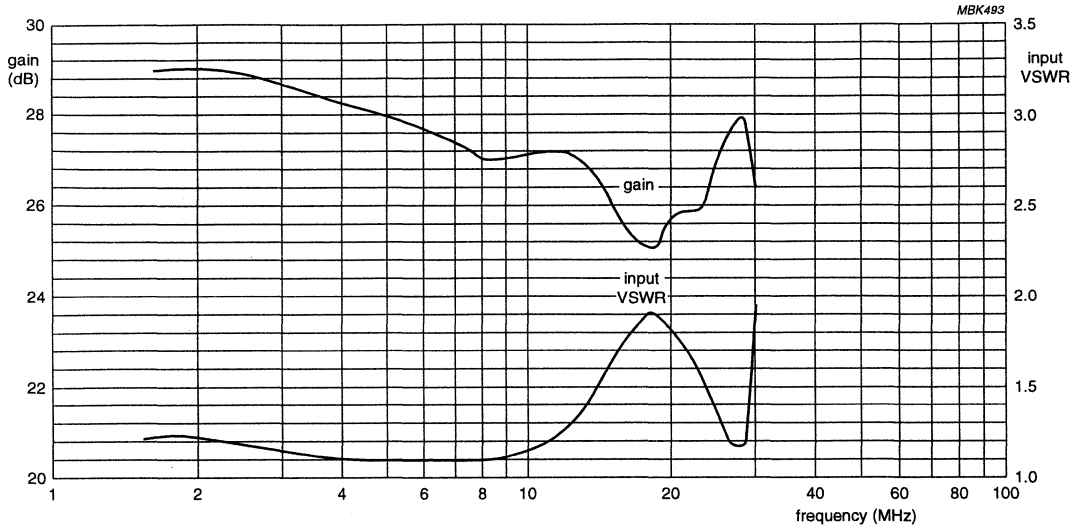


Fig.16 Amplifier gain and VSWR.

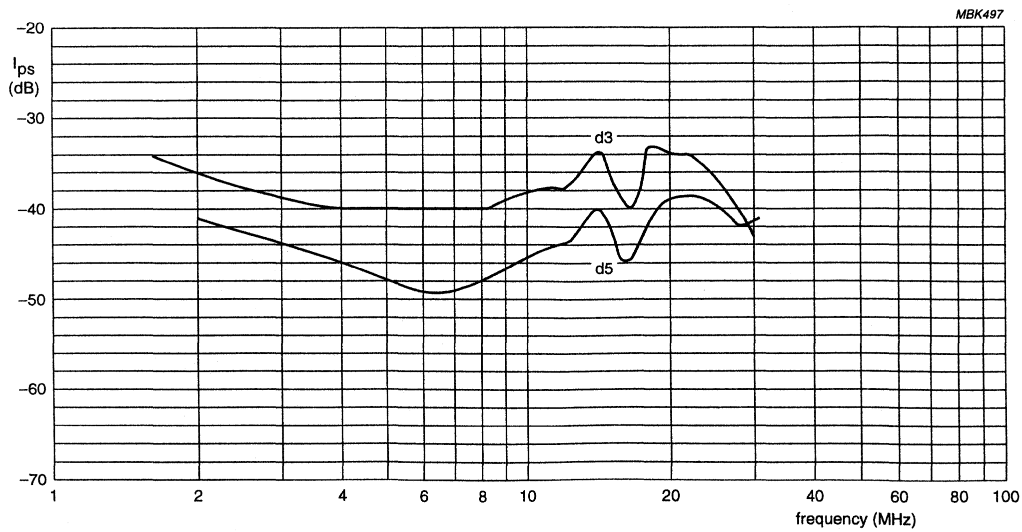


Fig.17 Intermodulation performance (50 V, 200 W PEP).

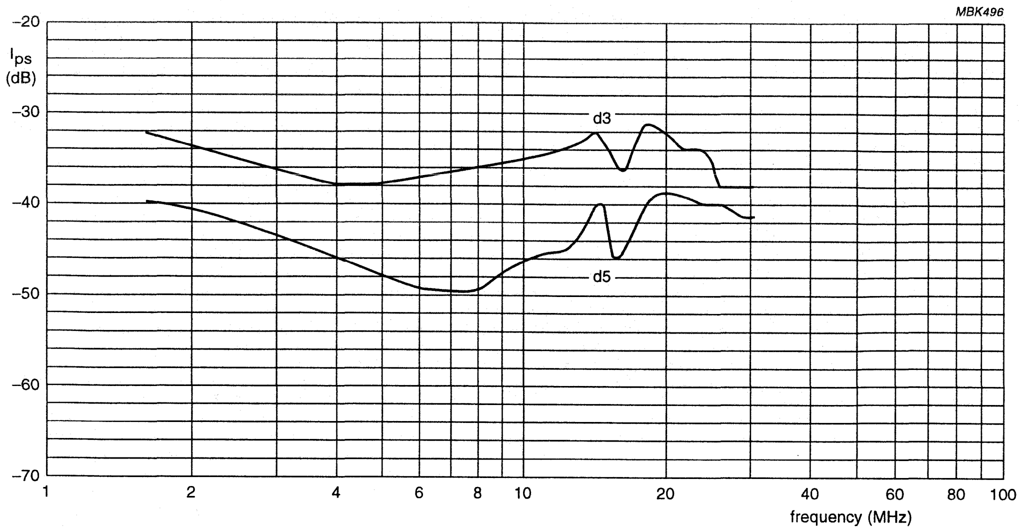


Fig.18 Intermodulation performance (50 V, 300 W PEP).

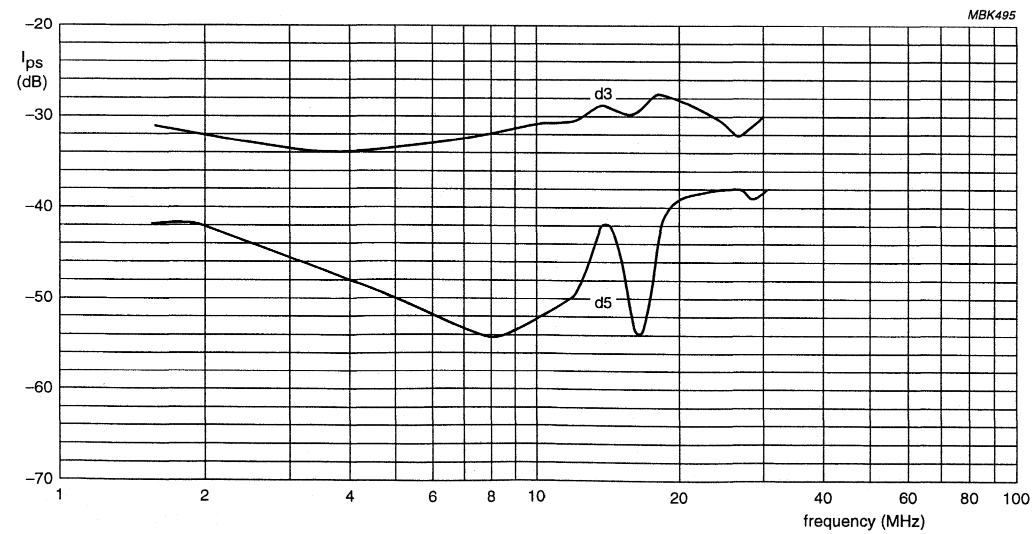


Fig.19 Intermodulation performance (50 V, 400 W PEP).

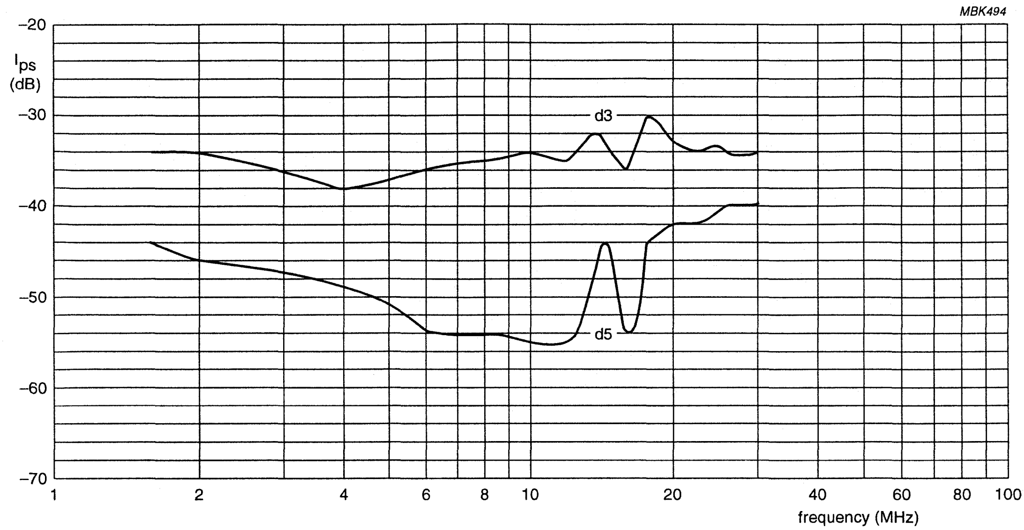


Fig.20 Intermodulation performance (45 V, 300 W PEP).

Combining units for a 1 kW wideband HF amplifier

1 SUMMARY

Based on Philips 4C6 ferrite toroids, input and output combining units are described for combining four 300 W PEP linear wideband amplifiers to produce at least 1 kW PEP in the HF band (1.6 – 30 MHz) with an intermodulation distortion of less than –30 dB.

2 INTRODUCTION

For long-range communication, the HF band from 1.6 – 30 MHz is used. As the modulation method is mainly SSB, linear amplifiers are required with output powers of 1 kW PEP in many cases. However, the best power amplifiers obtainable only have output powers of 300 to 400 W PEP. For example, Report AN98030 describes a push-pull amplifier using two BLW96 bipolar transistors delivering 400 W PEP, while Report NCO8703 describes a push-pull amplifier using two BLF177 MOS transistors delivering 300 W PEP. So four of these amplifiers are required to achieve powers of 1 kW PEP.

This report describes suitable combining units for both the input and output of such amplifiers to achieve the power mentioned above.

3 CIRCUIT DESCRIPTION

All transformers and hybrids used in the combiners are transmission line types as described in report ECO6907. Extensive use is made of Ferroxcube toroids, size: $36 \times 23 \times 15$ mm^3, material: 4C6. Part no.: 4322 020 91090.

3.1 The input power divider

Figs 1 and 2 show the block diagram and circuit diagram of the divider. It consists of four transformers wound on ferrite toroids, each transformer using one 4C6 toroid.

The input transformer provides a 4:1 impedance transformation from 50 Ω unbalanced input to 12.5 Ω unbalanced output. It consists of 7 turns of two parallel 50 Ω cables (3 mm ext. dia.) wound on the toroid.

The second transformer consists of 7 turns of two parallel 50 Ω cables (3 mm ext. dia.) wound on one toroid with the connections arranged as a hybrid to give a transformation from 12.5 Ω to two 25 Ω unbalanced in-phase outputs.

The third and fourth transformers are identical and consist of 8 turns of 50 Ω coaxial cable (3 mm ext. dia.) wound on the toroid with the connections arranged as a hybrid to give a transformation from 25 Ω to two 50 Ω unbalanced in-phase outputs.

Out-of-balance (or power dumping) resistors of 100 Ω are connected across the two 50 Ω output ports of each output transformer, and a 50 Ω resistor is connected across the two 25 Ω output ports of the intermediate hybrid transformer.

Although ideal transmission line transformers operate over a very wide band, in practice, there are inevitable performance degradations due to stray capacitance, stray leakage inductances etc. caused by the construction of such a system. In addition, the relatively large ballast resistors and their connecting leads (stray inductances) must be compensated by capacitors to obtain a near constant impedance throughout the band (1.6 – 30 MHz).

It was found experimentally, using a Hewlett Packard vector impedance meter, that satisfactory impedance compensation could be obtained by using three capacitors (120 pF, 80 pF and 80 pF) connected between the 12.5 Ω terminal and earth and each of the two 25 Ω impedance terminals to earth. The final result gave a maximum VSWR of 1.3 at the input port with all other ports terminated with 50 Ω wideband loads. Figure 3 shows the measured VSWR throughout the band.

The rating of the hybrid resistors is sufficient for fail-safe operation of the system under the worst fault conditions for continuous CW operation without forced air cooling of the resistors.

3.2 The output power combiner

Figs 4 and 5 show the block diagram and a circuit diagram of the combiner. Like the input power divider, it consists of four transformers wound on ferrite toroids.

One pair of amplifiers is coupled through 50 Ω ports to a common 25 Ω port (as is the other pair). Each transformer is wound with 5 turns of PTFE dielectric coaxial cable (2.5 mm ext. dia.) on a stacked core of two toroids, the connections arranged as a hybrid transformer from 50 Ω plus 50 Ω to 25 Ω. Out-of-balance (or power dumping) resistors of 100 Ω are connected across the two 50 Ω ports of each hybrid transformer.

A third hybrid transformer couples the two 25 Ω outputs to combine the power from these two sources to an impedance of 12.5 Ω. This transformer is wound with 3 turns of two 50 Ω PTFE dielectric coaxial cables (4.0 mm ext. dia.) on a stack of four toroids, the connections being arranged as a hybrid transformer from 25 Ω plus 25 Ω to 12.5 Ω. An out-of-balance (or power dumping) resistor of 50 Ω is connected across the two 25 Ω inputs.

The fourth transformer is a 1:4 impedance transformer which transforms the combined output at 12.5 Ω impedance to the 50 Ω load impedance. This transformer is wound with 4 turns of two parallel 50 Ω PTFE dielectric coaxial cables (4.0 mm ext. dia.) on a stack of five toroids, the connections are arranged for a 1:4 impedance transformer (unbalanced).

To compensate the stray influences (leakage inductance and capacitance etc.) it was found experimentally, using a vector impedance meter, that satisfactory compensation could be obtained using five capacitors connected at the points shown in the circuit of Fig.5. The final result (Fig.6) shows a maximum VSWR of 1.16 on any input port with all other ports terminated with 50 Ω wideband loads.

The rating of the hybrid resistors is sufficient for short-term fault conditions with two-tone signals without forced air cooling. With suitable forced air cooling, continuous CW operation under the most severe fault condition (two units inoperative) is possible.

A parts list for the input and output combiner units is given in Chapter 5.

4 MEASURED RESULTS

The practical performance of the units described was tested with four push-pull amplifiers each using two BLX15 bipolar transistors. The results concerning intermodulation are shown in the graphs of Fig.7 for a total output power of 1 kW PEP. All intermodulation products remained below –30 dB. Note, the BLX15 is no longer in Philips' product program and has been superseded by the BLW96 which has a maximum output power of 200 W PEP (at $d_3 \leq -30$ dB).

To keep the power loss in the hybrid resistors as low as possible, it is desirable to use amplifiers having roughly the same power gain. In the case of bipolar transistors, eight devices should be chosen from the same h_{FE} group, while for MOS transistors, devices should be chosen from the same $V_{GS(th)}$ group.

5 PARTS LIST

Table 1 Input power divider

4	4C6 Ferroxcube toroids (Philips); 36 × 23 × 15 mm; part no.: 4322 020 91090
1	50 Ω resistor, Electrosil type H35, 30 W
2	100 Ω resistor, Electrosil type H33, 15 W
	Miniature 50 Ω coaxial cable windings; external dia. approx. 3 mm (from any suitable manufacturer)
2	82 pF tubular ceramic (or ceramic plate) capacitors (low ε_r)
1	120 pF tubular ceramic (or ceramic plate) capacitor (low ε_r)

Table 2 Output power combiner

13	4C6 Ferroxcube toroids (Philips); 36 × 23 × 15 mm; part no.: 4322 020 91090
2	100 Ω resistors in parallel, Electrosil type H37
2	100 Ω resistors, Electrosil type H37
	50 Ω PTFE dielectric insulated coaxial cable; external dia. approx. 4 mm (from any suitable manufacturer)
2	33 pF ceramic block capacitors (ATC)
2	68 pF ceramic block capacitors (ATC)
1	120 pF ceramic block capacitors (ATC)

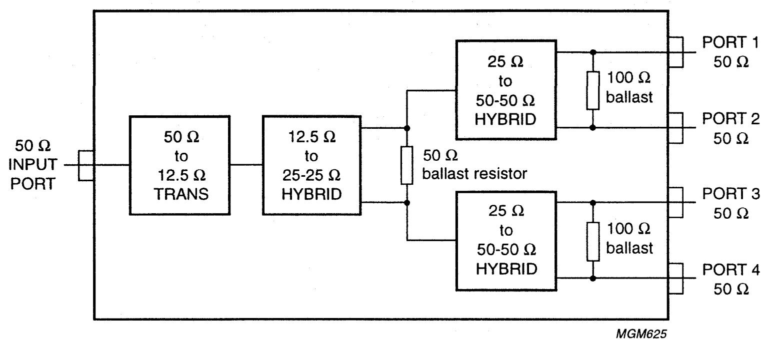


Fig.1 Block schematic of the input power divider.

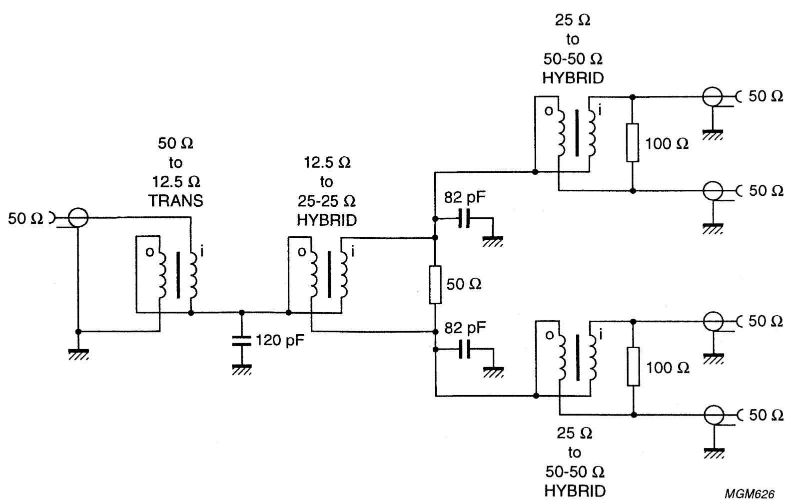


Fig.2 Circuit diagram of the input power divider.

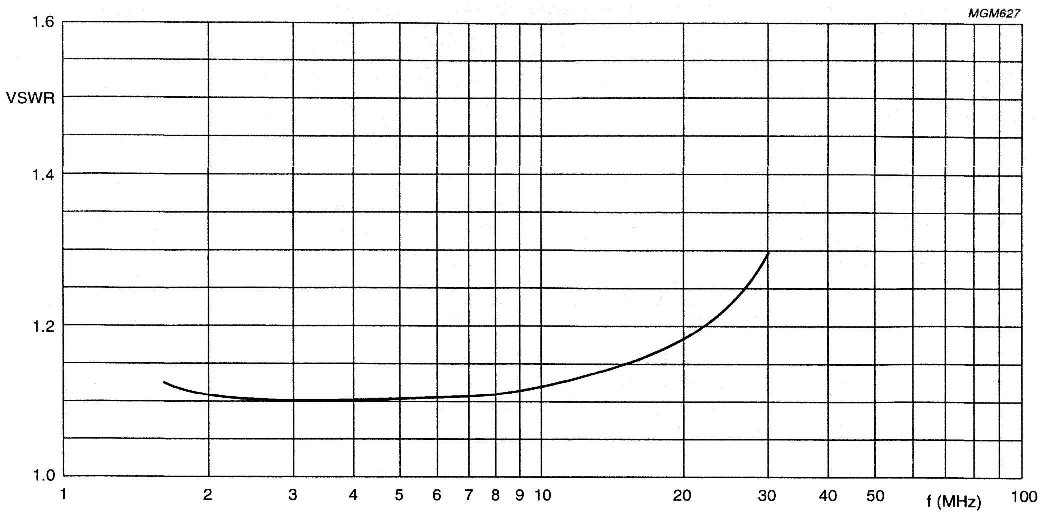


Fig.3 Input VSWR of the hybrid coupler with all output ports loaded by 50 Ω.

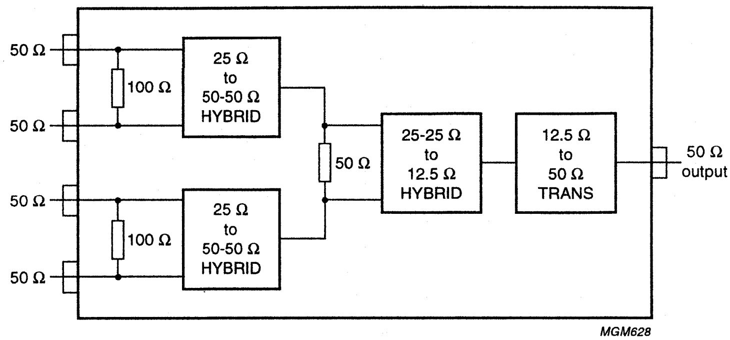


Fig.4 Block schematic of the output power combiner.

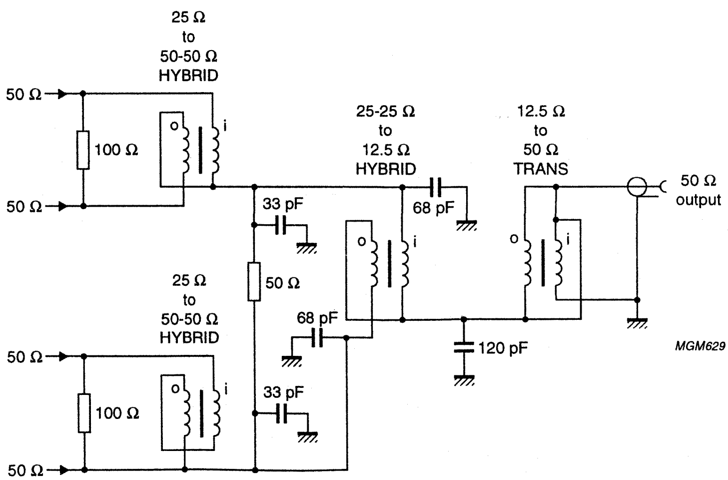


Fig.5 Circuit diagram of the output power combiner.

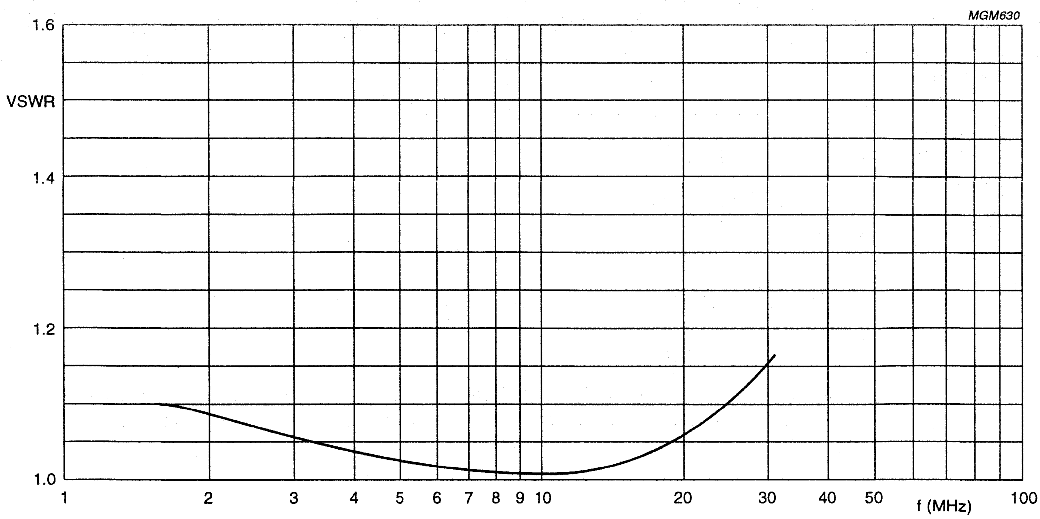


Fig.6 VSWR of any 50 Ω input port with all other ports terminated by 50 Ω.

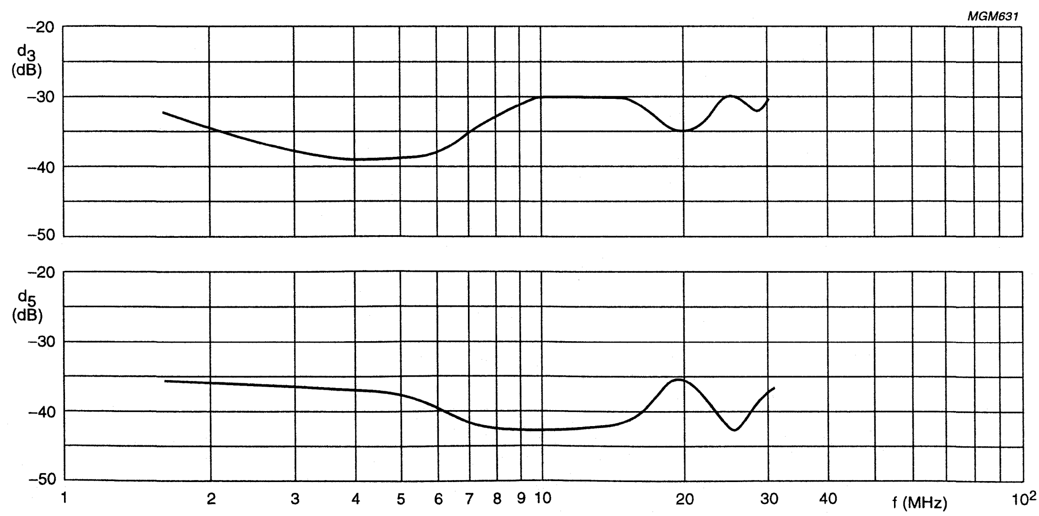


Fig.7 Intermodulation distortion (d_3 and d_5) of the four 300 W amplifiers coupled with hybrid couplers and driven to 1 kW PEP.

A wideband linear power amplifier (1.6 – 28 MHz) for 300 W PEP with 2 MOS transistors BLF177

Application Note
NC08703

1 SUMMARY

This report gives a description of a wideband push-pull amplifier for the frequency range 1.6 – 28 MHz.
The amplifier has been designed around 2 MOS transistors BLF177 which operate in class-AB at V_{DS} = 50 V and I_{DQ} = 0.5 A/transistor.
The main properties at P_O = 300 W are:

- Powergain: 22 to 23 dB
- Efficiency: 52.5 to 61%
- Return losses input: ≤ –15.5 dB
- 2nd harmonics: ≤ –25 dB
- 3rd harmonics: ≤ –16 dB
- IMD at P_O = 300 W PEP: ≤ –33 dB.

2 INTRODUCTION

The BLF177 is an RF Power MOS transistor for the HF and VHF range in a 4 leads flange SOT121 encapsulation. For the frequency range 1.6 – 28 MHz a wideband push-pull power amplifier has been developed with 2 × BLF177 having an output power of 300 W PEP at an intermodulation distortion level below –30 dB.
The transistors operate in class-AB at V_{DS} = 50 V and a quiescent current of 0.5 A each.

3 DESIGN OF THE AMPLIFIER

3.1 General

The schematic set-up is given in Fig.1.

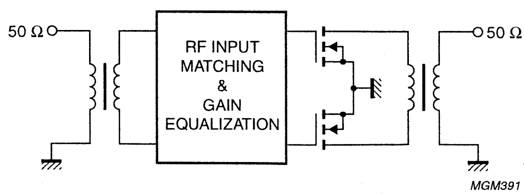


Fig.1 Schematic set-up 2 × BLF177 amplifier.

The two balance to unbalance transformers are applied to split the single ended input into 2 out of phase driving ports and to add the 2 out of phase output ports into one single ended output. The transformers have an impedance transformation ratio of 4 : 1 and match the low-ohmic in- and output impedance of the transistors to the 50 Ω system impedance. At the input a special circuit takes care of a good input matching and a flat powergain over the whole bandwidth.

3.2 Output circuit

3.2.1 LOAD IMPEDANCE

The output impedance of each transistor can be represented as a combination of the output capacitance C_{oss} and the optimum load resistance. Because of the larger drain voltage swing the effective output capacitance C_O is appr. 15% higher than the value of C_{oss}. So $C_O = 1.15 \times 190 \approx 220$ pF. The optimum load resistance for class-AB can be determined with formula:

$R_L = (0.85 \times V_{DS})^2/(2 \times P_O)$

For $V_{DS} = 50$ V and $P_O = 150$ W we get $R_L = 6\ \Omega$. To keep the transformer simple a transformation ratio of 4 or 9 is preferable. A ratio of 4 gives a load impedance of $50/4 = 12.5\ \Omega \rightarrow 6.25\ \Omega$ for each transistor. This is very near to the optimum load resistance.

3.2.2 OUTPUT TRANSFORMER

The output transformer has to transform the 50 Ω asymmetrical impedance to the $2 \times 6.25 = 12.5\ \Omega$ symmetrical load impedance. The reactance (ωL) of the shunting inductance at 1.6 MHz has been chosen at 4 times 50 Ω = 200 Ω. So the inductance is 20 μH. The transformer has been wound on a ferrite toroid of 4C6 material. Dimensions: 36 × 23 × 15 mm (D × d × h) which gives a volume (A.1) = 8.97E-6m^3.
Because the power handling of one toroid is critical two transformers in parallel with an inductance of 40 μH each have been chosen.

n_{sec} = SQR((L.1)/(μo × μr × A))
n_{sec} = SQR((40E – 6 × 9.2E – 2)/(4πE – 7 × 120 × 97.6E – 6)) = 15.8 turns.
So n_{pr} = 8 turns and n_{sec} = 16 turns.

For each transformer V_{max} depends on the power over 100 Ω.
V_{max} = SQR(2 × P_O × R_L) = SQR(2 × 150 × 100) = 173.2 V

B_{max} depends on the parallel loss resistance at 1.6 MHz; for a power loss of 1%: B_{max} = 1.3E – 2T.
The volume A.1 needed per core is:
A.1 = $(V_{max}/(\omega \times B_{max}))^2(\mu_o \times \mu_r)/L$.

A.1 = (1.73.2/(2π × 1.6E + 6 × 0.013))^2(4πE – 7 × 120)/40E – 6 = 6.62E – 6 m^3.

Each of the toroids has a volume of 8.97E – 6 m^3. Figure 7 shows one of the two parallel connected output transformers. On each toroid the primary winding has 8 turns of copperfoil (width 5 mm and thickness 0.05 mm). The secondary winding has 16 turns of 2 enamelled copper wires (0.6 mm) in parallel.
So each primary turn has been covered with 2 secondary turns which means 4 wires of 0.6 mm. Both windings are isolated with PTFE-foil (thickness 0.1 mm). To reduce the stray-inductance the transformer has been wound as follows:

1. The primary has been wound evenly around the periphery of the toroid
2. With the secondary the same has been done with the first 8 turns; the second part of 8 turns has been wound in between the first part. So the secondary has been wound twice around the core.

The measured secondary inductance of each transformer is 38 μH and L_{str} = 300 nH.
With the aid of a network analyser the parallel combination of these 2 transformers has been corrected. For the higher frequencies at the low-ohmic side a parallel capacitor of 240 pF and for the lower frequencies at the high-ohmic side a series capacitor of 10 nF give return losses below –21 dB over the whole frequency range (see Fig.2).

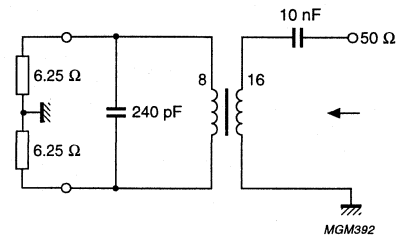


Fig.2 Output transformer with correction.

Replacing the transistors by resistors of 6.25 Ω the return loss can be measured at the 50 Ω side. Figure 11 gives the return losses of the parallel combination of the two transformers before and after the correction.

3.2.3 THE TAPPED CHOKE

The chokes in the drain circuits are wound around a common ferrite rod of 4B1 material. Dimensions: 50 × 10 mm (l × d). Figure 3 gives a schematic electrical circuit of the output.

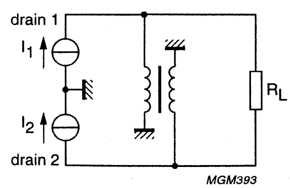


Fig.3 Output with the tapped choke.

Between both drains the impedance for the even harmonics depends on the coupling factor between both windings. If the coupling factor amounts to 1 both drains will be short circuited for the even harmonics.
Because the voltage over one winding is equal to half of the voltage between both drains, the total inductance between both drains is 4 times the inductance of one winding.
The reactance of the shunting inductance at 1.6 MHz has been chosen at 4 times 12.5 Ω = 50 Ω.

So the inductance between both drains is 5 μH, this means for one winding an inductance of 1.25 μH. According to the Philips Data Handbook *"MA01 on soft ferrites of 1996, the effective permeability"* of a rod with 1/d = 5 and μ_r = 250 is appr. 20.
The number of turns can be calculated with:

$n = SQR(L.1/(\mu_o \times \mu_r \times A))$

$n = SQR(1.25E - 6 \times 50E - 3/(4\pi E - 7 \times 20 \times \frac{1}{4}\pi(10E - 3)^2) = 5.6$ turns. In practice 6 twisted turns of the primary and secondary windings have been wound around the rod. Figure 8 shows the tapped choke. To increase the coupling factor each winding consists of 2 enamelled copper wires (0.8 mm) in parallel. The measured inductance is 1.275 μH.

3.2.4 TUNING OF THE OUTPUT CIRCUIT

For an optimum alignment of the output circuit the 2 transistors have been replaced by dummies consisting of the parallel connection of a resistance and a capacitance. The resistance is equal to the optimum load resistance and the capacitance to the output capacitance (see Section 3.2.1).
Tuning of the output circuit has been carried out by measuring the return losses at the output with a network analyser under swept conditions (see Fig.4).

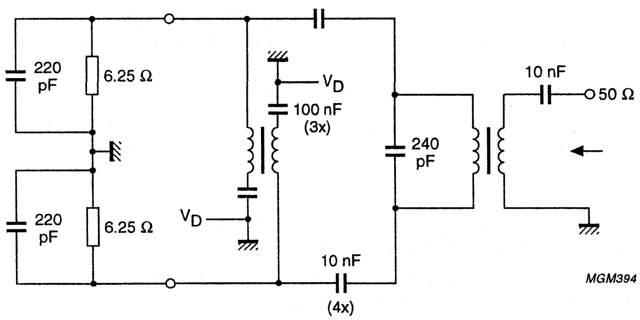


Fig.4 Output circuit before tuning.

The measured return losses should be as low as possible by changing the correction capacitors. Figure 12 shows the return losses of the output before and after tuning. For optimum results the capacitance across the primary winding of the output transformer has been reduced from 240 to 150 pF and the low frequency correction capacitor of 10 nF at the output has been changed to an inductance of 100 nH. The last change can be explained as follows:

1. The low frequency compensation is taken over by the coupling capacitors between the drain choke and the impedance transformer
2. The function of the transformer is not only impedance matching but also transfer from balanced to unbalanced. The latter makes that the interwinding capacitance has more influence. This is so much that a series inductance at the output is needed for high frequency compensation.

3.3 Input circuit

3.3.1 INPUT IMPEDANCE

The input impedance and gain of the transistor can be determined with the aid of a computer model of the BLF177. Table 1 shows the calculated gain and impedances for the frequency range 1.6 to 28 MHz.

BLF177 Vds = 50 V Po = 150 W Class-AB.

Table 1 Calculated gain and impedances of the BLF177

f (MHz)	G (dB)	INP.IMP. (Ω)	LOAD IMP. (Ω)
1.6	54.70	2.29 – j133.58	6.23 + j.07
2.5	50.82	2.29 – j85.50	6.23 + j.12
3.5	47.90	2.29 – j61.09	6.23 + j.16
5.0	44.80	2.29 – j42.78	6.22 + j.23
7.0	41.88	2.29 – j30.58	6.21 + j.32
10.0	38.78	2.29 – j21.45	6.18 + j.46
14.0	35.85	2.29 – j15.37	6.13 + j.64
20.0	32.75	2.29 – j10.84	6.03 + j.89
24.0	31.17	2.29 – j9.09	5.95 + j1.05
28.0	29.83	2.29 – j7.85	5.85 + j1.20

By adding a gate-source resistor of 6.25 Ω the power gain reduces from 29.8 to 23.3 dB at 28 MHz.

3.3.2 INPUT MATCHING CIRCUIT

As mentioned in Section 3.1 a special circuit matches the input impedance of each transistor to the 6.25 Ω of the input transformer. The matching network chosen can be treated as the half of a double π-section as described in Ref.1. Removing the in- and output capacitance the circuit changes in a T-section with C_i as capacitor and 2 inductances with a value of half the inductances of the double π-section (see Fig.5).

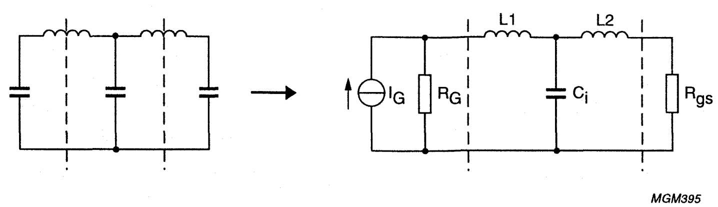


Fig.5 Input matching circuit.

C_i represents the input capacitance of the BLF177 and can be calculated from the input impedance of Table 1.
For 7 MHz: $C_i = 1/(2\pi \times 7E + 6 \times 30.58) = 744$ pF.
Across this capacitor a constant voltage versus frequency from 1.6 up to 28 MHz has to be developed. Provided C_i is an ideal capacitance the dimensioning of this network is as follows:
$R_G = R_{gs}$ must be appr. 6 Ω to obtain low I.M. distortion and good stability. This appeared during the development of the narrow band testcircuit as given in the BLF177 publication data. To judge whether this value is also acceptable for wideband operation we calculate the product:
$W_c \times C_i \times R_{gs}$ in which ω_c is the maximum angular frequency.
Doing so we find:
$2\pi \times 28E + 6 \times 744E - 12 \times 6.25 = 0.818$
R_{gs} has been chosen 6.25 Ω for the ease of transformation. Comparing the value of this product with the one given in Ref.2 we see that with a double π-section we can easily reach a bandwidth of 50 MHz. Therefore we have simplified the network as described above. Continuing the calculation we find:
$L = 0.997\ R_G/\omega_c = 35.4$ nH (So L1 = L2 = 17.7 nH)
With the computer model mentioned in Section 3.3.1 a gain of 22.3 dB has been calculated with $R_{gs} = 6.25$ Ω.

Starting from this 22.3 dB gain, $L_1 = L_2 = 17.7$ nH and $R_{gs} = 6.25$ Ω the input VSWR and gain deviation have been calculated (see Table 2).

Initial results
Rs = 6.250 Ω; Gs = 22.300 dB
Par.LR: L = 17.700 nH; R = 6.250 Ω
Ser.Ind.: L = 17.700 nH

Table 2 Results before optimization

f (MHz)	VSWR	dG (dB)
1.6	1.010	1.440
2.5	1.016	1.435
3.5	1.023	1.431
5.0	1.032	1.419
7.0	1.046	1.402
10.0	1.068	1.354
14.0	1.100	1.265
20.0	1.161	1.075
24.0	1.214	.910
28.0	1.281	.703

Before optimization the maximum VSWR = 1.28 and the gain = 22.7 dB ± 0.37 dB. To achieve a maximally flat gain and a low input VSWR a computer optimization program has been used. This optimization results in a gain of 23.3 dB with a maximum ΔGain = ±0.09 dB and a VSWR ≤1.09, see Table 3. For these results L_1 has been changed from 17.7 nH to 9 nH and L_2 from 17.7 nH to 21.1 nH. the R_{gs} has been decreased from 6.25 Ω to 5.7 Ω.
Final results
Rs = 6.250 Ω; Gs = 23.300 dB
Par.LR: L = 21.079 nH; R = 5.749 Ω
Ser.Ind.: L = 8.950 nH

Table 3 Results after optimization

f (MHz)	VSWR	dG (dB)
1.6	1.087	.072
2.5	1.087	.071
3.5	1.087	.074
5.0	1.086	.076
7.0	1.085	.084
10.0	1.082	.087
14.0	1.076	.086
20.0	1.059	.056
24.0	1.047	.006
28.0	1.044	–.087

3.3.3 INPUT TRANSFORMER

The input transformer is simular to the output transformer. It transforms the asymmetrical system impedance to the $2 \times 6.25\ \Omega = 12.5\ \Omega$ symmetrical source impedance. However the lower power handling (<3 W) justifies a toroid of 4C6 material with smaller dimensions: $14 \times 9 \times 5$ mm ($D \times d \times h$) which gives a volume A.1 = 0.445E – 6 m^3. As described in Section 3.2.2 the primary winding can be calculated for L = 20 μH.

$n_{pr} = SQR((L.1)/(\mu_o \times \mu_r \times A))$

$n_{pr} = SQR((20E-6 \times 3.55E-2)/(4\pi E-7 \times 120 \times 12.54E-6) = 19.4$ turns. With $n_{pr} = 20$ turns and a transformation ratio of 4 : 1 the $n_{sec} = 10$ turns.
$V_{max} = SQR(2 \times P_i \times R_S) = 17.3$ V and $B_{max} = 0.013$T.

The needed core volume A.1 is:

$A.1 = (V_{max}/(\omega \times B_{max}))^2 \times (\mu_o \times \mu_r)/L$

$A.1 = (17.3/(2\pi \times 1.6E+6 \times 0.013)^2 \times (4\pi E-7 \times 120)/20E-6 = 0.14E-6\ m^3$

The core used has a volume of 0.445E – 6m^3.
Figure 9 shows the input transformer. The secondary winding has 10 turns of copperfoil (width 2 mm, thickness 0.05 mm). The primary winding has 20 turns of enamelled copper wire (0.5 mm). Each secondary turn has been covered with 2 primary turns with a PTFE foil of 0.1 mm thickness as isolation between the 2 windings. The method of winding is the same as described for the output transformer in Section 3.2.2. The measured inductance is 20.95 μH and $L_{str} = 250$ nH.
The correction method used for the input transformer is the same as described already in Section 3.2.2 (see Fig.6).

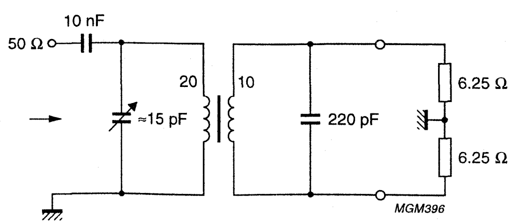


Fig.6 Inputtransformer with correction.

The transformer has been corrected with parallel capacitors for the higher frequencies and a series capacitor for the lower frequencies. Figure 13 gives the return losses before and after the correction.

3.3.4 TUNING OF THE INPUTCIRCUIT

For the practical tuning of the inputcircuit each transistor has been adjusted at V_{DS} = 50 V and a quiescent current of 0.5 A.
The gain and input return losses have been measured in the frequency range 1.6 up to 35 MHz. The best results have been achieved by changing the secondary correction capacitor of the inputtransformer from 220 to 30 pF and the primary correction trimmer from ≈ 15 pF to ≈ 20 pF. The low frequency correction capacitor at the input has been removed. The inductance in serie with R_{gs} has been increased from 21.6 to 35 nH. Figure 14 gives the complete circuit diagram of the wide band amplifier with 2 BLF177 transistors. Table 5 gives the corresponding parts list.

4 CONSTRUCTION OF THE AMPLIFIER

For the printed circuit board double Cu-clad epoxy fibre glass has been used with a thickness of 1/16" and ε_r = 4.5. The position of the components is on one side and the other side serves as a groundplane. Connections to the groundplane have been made with rivets and with straps under the source leads and at the edges of the PC-board on the in- and output side.
The printed circuit board has been attached to a solid copper plate (145 × 120 × 10 mm) which functions as a heatsink. Around the position of both transistors a tube has been soldered in the copper plate to controle the temperature by means of a watercooling system. For a good thermal contact between heatsink and transistors heatsink compound has been used.
Figure 15 shows the lay-out of the amplifier. The transformers have been fastened above the printed circuit board by means of accessories of Delrin material.
These accessories have been attached through the PC-board in the copper plate.

5 MEASURED PERFORMANCE

5.1 Single tone measurements

Figures 16 to 20 show at a constant outputpower of 300 W at 2 heatsink temperatures the gain, efficiency, input return losses, 2nd and 3rd harmonics at the output as a function of the frequency. In the range 1.6 to 28 MHz the gain is 22 to 23 dB, the efficiency 52.5 to 61%, the input return losses are below −15.5 dB, the second harmonics better then −25 dB and the third harmonics below −16 dB.
At a heatsink temperature of 70 °C the gain decreases about 1.5 dB. The heatsink temperature has only little influence on the other parameters. Figures 21 to 23 shows at 4 frequencies the output power as a function of the input power and the gain and efficiency versus outputpower.
Above 10 MHz the efficiency decreases about 6%. At 20 MHz the gain decreases above P_O = 200 W. At other frequencies this decrease starts at P_O = 300 W.

5.2 Two tone measurements

The two tone measurements have been carried out with 2 carriers with a frequency distance of 1 KHz. Figure 24 to 27 give as a function of the frequency the gain, efficiency, 3rd order distortion and 5th order distortion at 4 output levels. Over the whole frequency range the gain variation is less than 1 dB at each power level. At P_O = 300 W PEP the efficiency is at least 40%, the 3rd order distortion ≤–33 dB and the 5th order distortion ≤–38 dB.
Figures 28 and 29 give the 3rd and 5th order distortion versus output power at 4 frequencies.
To verify the choice of I_{DQ} = 1 A the 2nd and 3rd order distortion have been measured versus I_{DQ}. These measurements have been carried out at the most critical frequency and output level of 20 MHz and 30 W PEP resp.
Figure 30 shows that I_{DQ} = 1A for both transistors together was a good choice.

6 BALANCED CIRCUIT

As shown in Table 4 there is a certain amount of unbalance between both drain currents at RF operation. It is possible to improve this by using baluns in front of the input transformer and after the output transformer.

Table 4 Drain currents at P_O = 300 W

f (MHz)	I_{D1} (A)	I_{D2} (A)
1.6	5.2	4.8
5	5.1	4.75
10	5.25	4.8
15	5.3	4.95
20	5.7	5.3
25	6.2	5.25
30	5.85	5.15

7 CONCLUSIONS

This report shows that it is possible to design a wideband push-pull amplifier with 2 BLF177 MOS transistors having a very good performance.
The main properties are:

- Bandwidth: 1.6 to 28 MHz
- V_{DS}: 50 V
- I_{DQ}: 1 A
- Gain at P_O = 300 W: 22 to 23 dB
- Efficiency at P_O = 300 W: 52.5 to 61%
- Return losses input at P_O = 300 W: ≤–15.5 dB
- 2nd harmonics output at P_O = 300 W: ≤–25 dB
- 3rd harmonics output at P_O = 300 W: ≤–16 dB
- IMD at P_O = 300 W PEP: ≤–33 dB.

8 REFERENCES

G. Lukkassen
Application report NCO8602
A wideband power amplifier (25 to 110 MHz) with the MOS transistor BLF245.

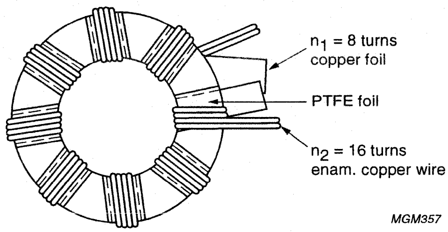


Fig.7 Output transformer.

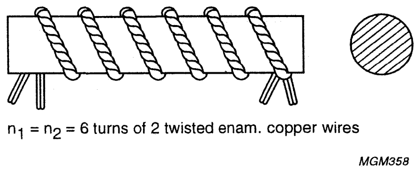


Fig.8 Tapped drain choke.

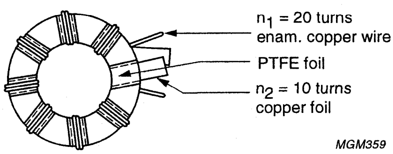


Fig.9 Input transformer.

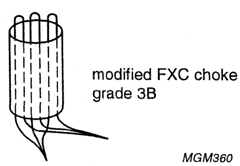


Fig.10 Decoupling choke.

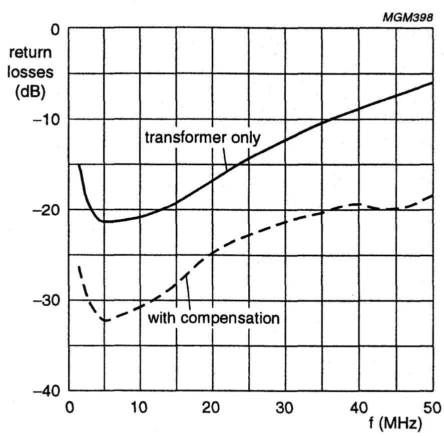


Fig.11 Output transformer correction.

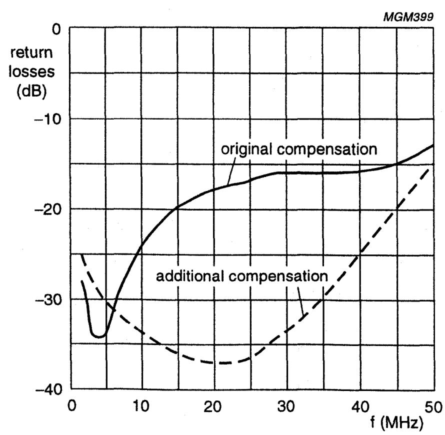


Fig.12 Return losses output circuit.

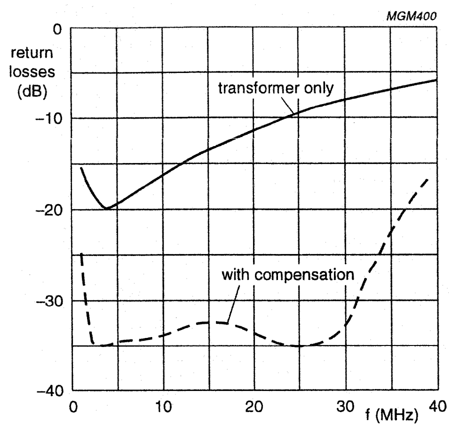


Fig.13 Input transformer correction.

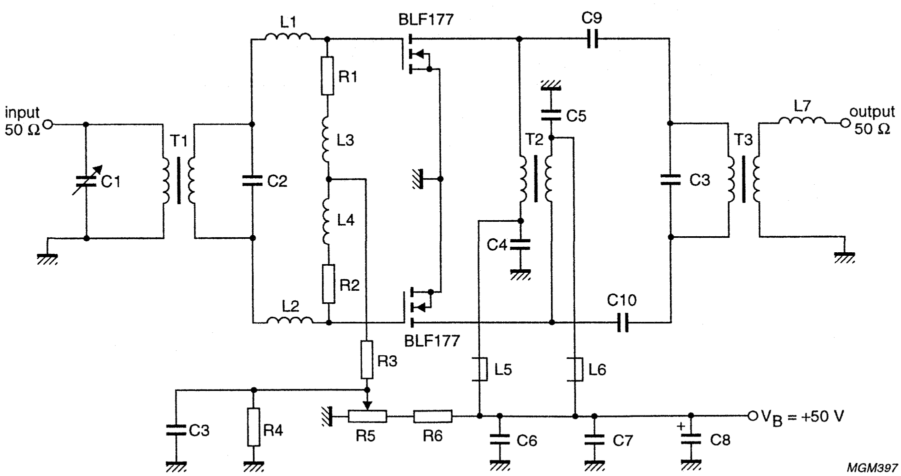


Fig.14 Circuit diagram of the 2 × BLF177 amplifier.

Table 5 Parts list of the wide band push-pull amplifier with 2 × BLF277 (1.6 to 28 MHz); note 1

C1	5 – 60 pF film dielectric trimmer (cat.nr.: 2222 809 08003)
C2	30 pF multilayer chip capacitor; note 2
C3	2 × 100 nF multilayer chip capacitor (cat.nr.: 2222 852 47104)
C4 = C5	3 × 100 nF metallized film capacitor (car.nr.: 2222 368 21104)
C6 = C7	100 nF multilayer chip capacitor (cat.nr.: 2222 852 47104)
C8	10 µF (63 V) electrolytic capacitor (cat.nr. 2222 030 28109)
C9 = C10	4 × 10 nF metallized film capacitor (cat.nr. 2222 368 51103)
C11	2 × 75 pF multilayer chip capacitor; note 2
L1 = L2	≈ 9 nH, printed inductance; l = 47 and w = 6 mm
L3 = L4	35 nH, 3 turns enamelled Cu-wire (0.7 mm) int.dia.: 3 mm, l = 2.35 mm
L5 = L6	2.2 µH, 1 turns through modified Ferroxcube choke grade 3B (cat.nr.: 4312 020 36642); see Fig.10
L7	100 nH, 5 turns enamelled Cu-wire (0.8 mm) int.dia.: 5 mm, 1 = 6.1 mm
R1 = R2	5.9 Ω; 4 metal film resistors of 23.7 Ω (0.4 W) in parallel (cat.nr.: 2322 151 72379)
R3	1 kΩ, metal film resistor (0.4 W) (cat.nr.: 2322 151 71002)
R4	1 MΩ, metal film resistor (0.4 W) (cat.nr.: 2322 151 71005)
R5	500 Ω, Cermet potentiometer (0.75 W)
R6	5.6 kΩ, metal film resistor (1 W) (cat.nr.: 2322 153 55622)
T1	input transformer: n_{pr} = 20 turns enamelled Cu-wire (0.5 mm) n_{sec} = 10 turns copper foil (width 2 mm), thickness 0.05 mm) wound around toroidal core, grade 4C6, dimensions: 14 × 9 × 5 mm (cat.nr. 4322 020 97181) see Fig.9
T2	drain choke: 6 turns of twisted pairs of 0.8 mm Cu-wires (each winding consists of 2 wires in parallel) wound on a Ferroxcube rod, grade 4B1, dimensions 10 × 50 mm, see Fig.8
T3	n_{pr} = 8 turns copper foil (width 6 mm, thickness 0.05 mm) n_{sec} = 16 turns of 2 enamelled Cu-wires (0.6 mm) in parallel wound around toroidal core, grade 4C6, dimensions: 36 × 23 × 15 mm (cat.nr. 4322 020 97201) see Fig.7; 2 of these transformers in parallel form the complete outputtransformer

Notes

1. PC-board: double Cu-clad, 1/16” epoxy fibre glass (ε_r = 4.5)
2. American Technical Ceramics type 100B or capacitor of same quality.

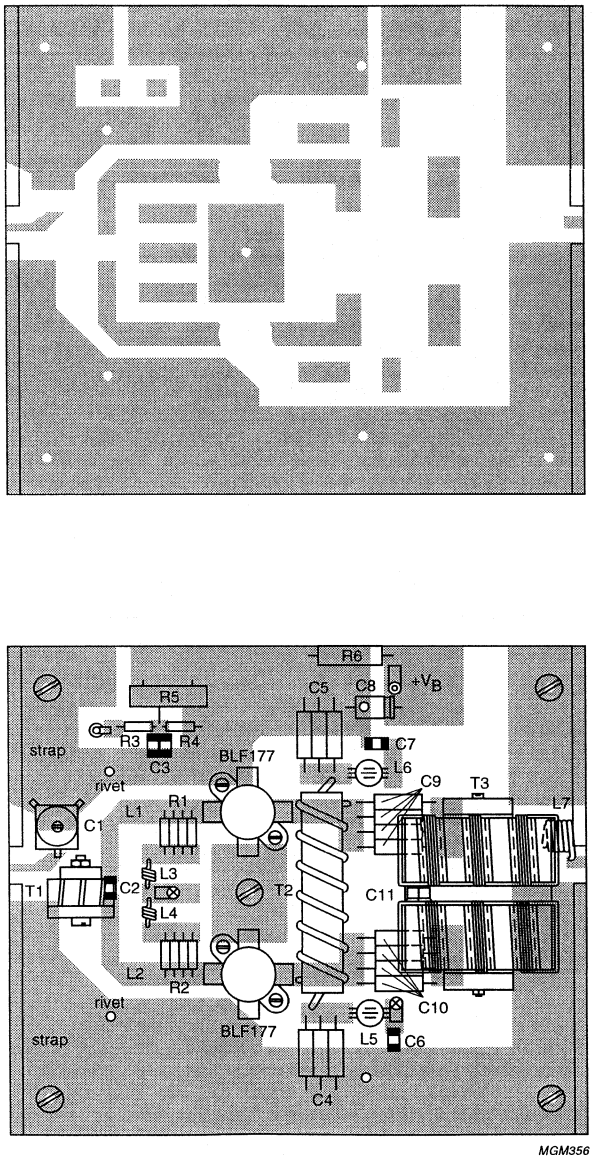
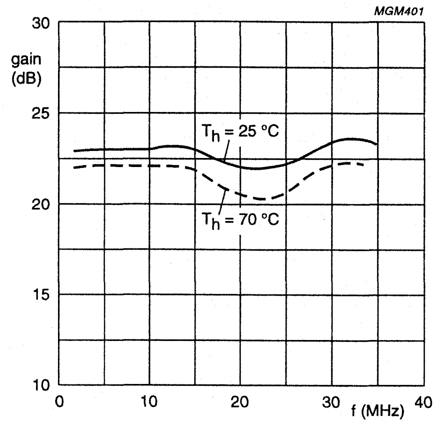
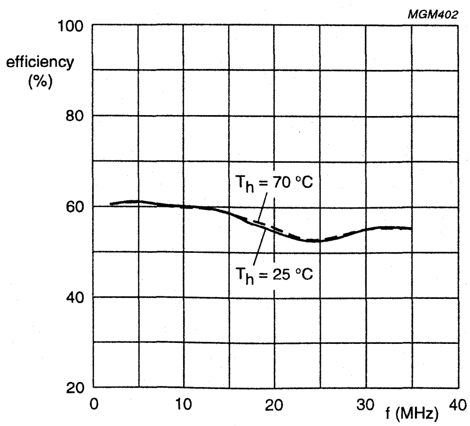


Fig.15 Lay-out of the 2 × BLF177 amplifier.



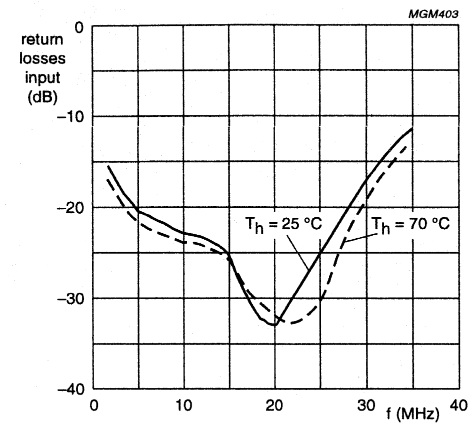
2 × BLF177
V_{DS} = 50 V
I_{DQ} = 1A
P_O = 300 W

Fig.16 Gain versus frequency.



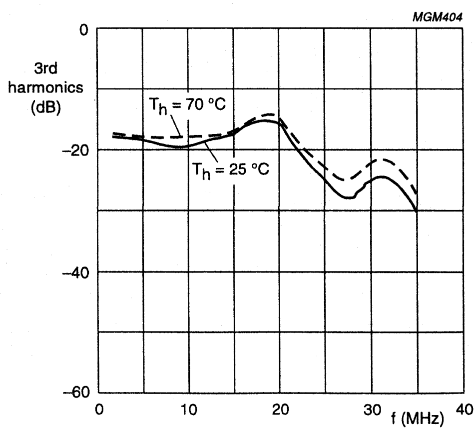
2 × BLF177
V_{DS} = 50 V
I_{DQ} = 1A
P_O = 300 W

Fig.17 Efficiency versus frequency.



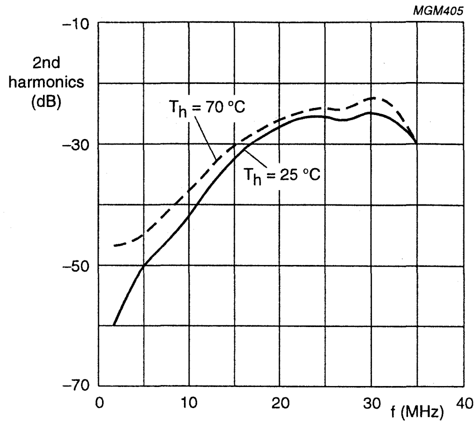
2 × BLF177.
V_{DS} = 50 V.
I_{DQ} = 1A.
P_O = 300 W.

Fig.18 Input return losses versus frequency.



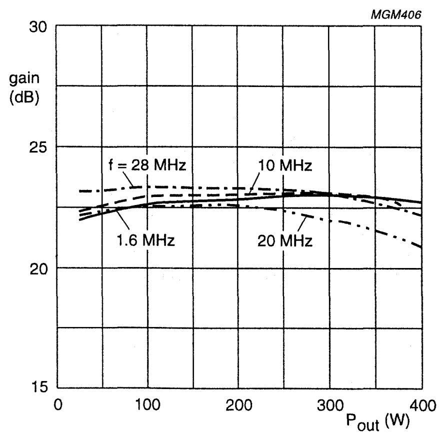
2 × BLF177.
V_{DS} = 50 V.
I_{DQ} = 1A.
P_O = 300 W.

Fig.19 3rd harmonics versus frequency.



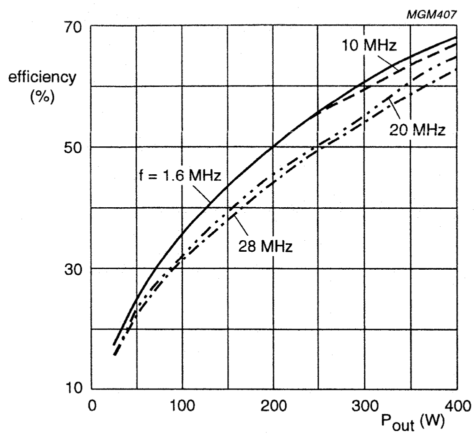
2 × BLF177.
V_{DS} = 50 V.
I_{DQ} = 1A.
P_O = 300 W.

Fig.20 2nd harmonics versus frequency.



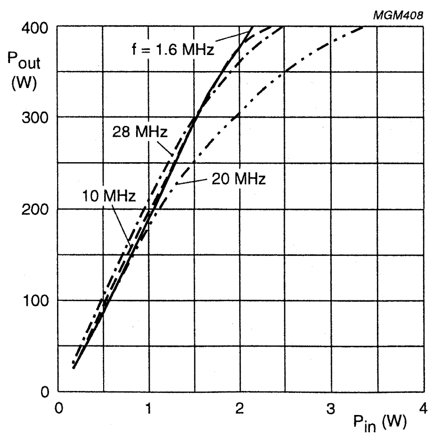
2 × BLF177.
V_{DS} = 50 V.
I_{DQ} = 1A.

Fig.21 Gain versus outputpower.



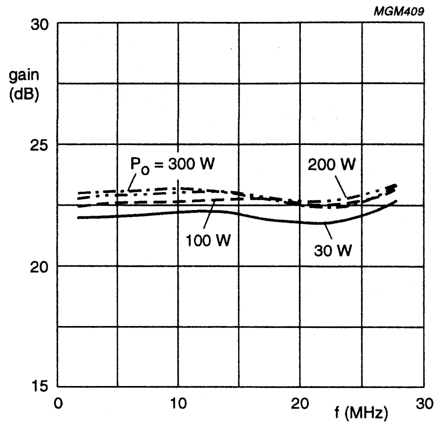
2 × BLF177.
V_{DS} = 50 V.
I_{DQ} = 1A.

Fig.22 Efficiency versus outputpower.



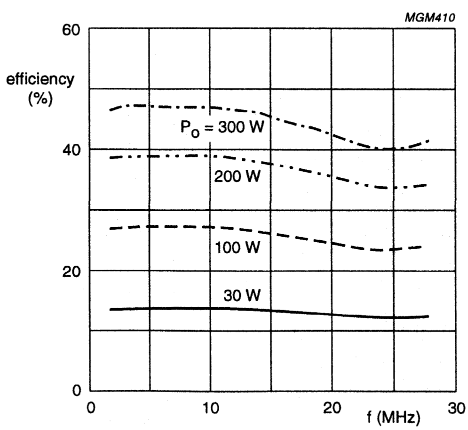
2 × BLF177.
V_{DS} = 50 V.
I_{DQ} = 1A.

Fig.23 Outputpower versus inputpower.



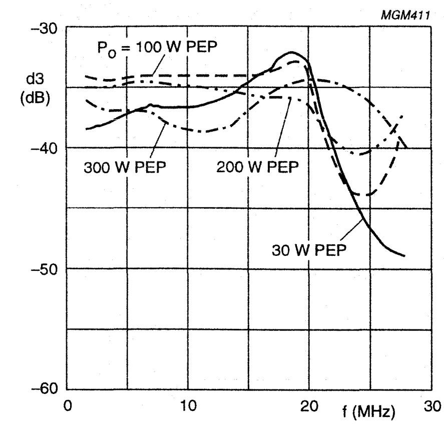
2 × BLF177.
V_{DS} = 50 V.
I_{DQ} = 1A.
$f_p - f_q$ = 1 kHz.

Fig.24 Gain versus frequency.



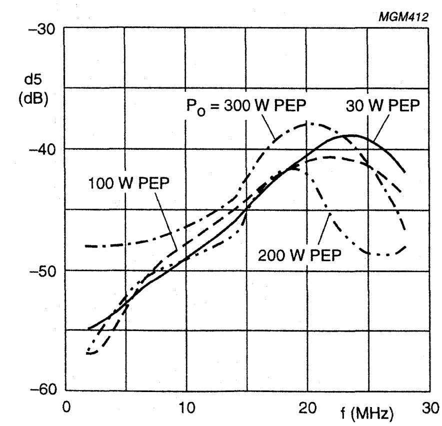
2 × BLF177.
V_{DS} = 50 V.
I_{DQ} = 1A.
$f_p - f_q$ = 1 kHz.

Fig.25 Efficiency versus frequency.



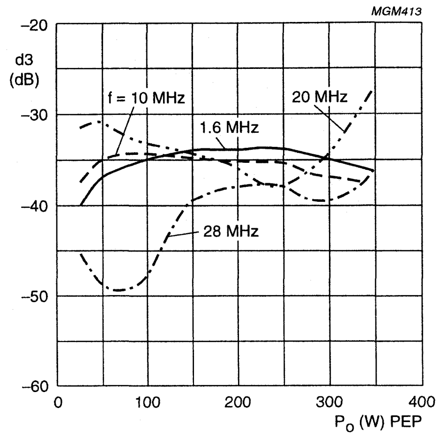
2 × BLF177.
V_{DS} = 50 V.
I_{DQ} = 1A.
$f_p - f_q$ = 1 kHz.

Fig.26 Third order dist. versus frequency.



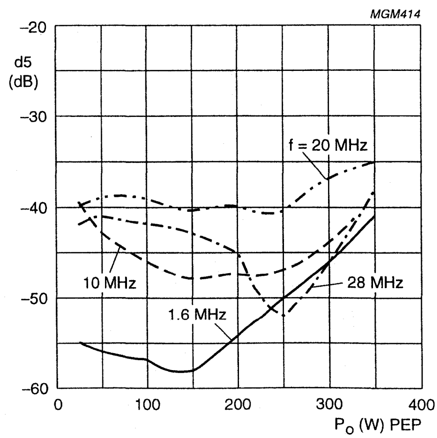
2 × BLF177.
V_{DS} = 50 V.
I_{DQ} = 1A.
$f_p - f_q$ = 1 kHz.

Fig.27 Fifth order dist. versus frequency.



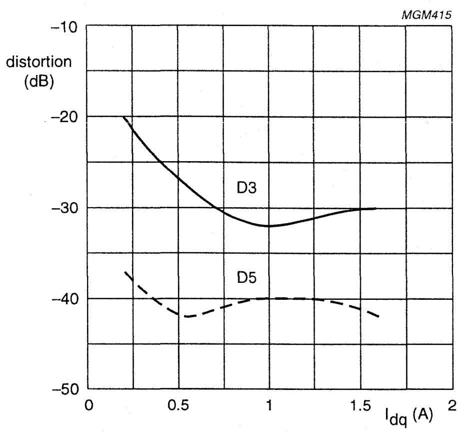
2 × BLF177.
V_{DS} = 50 V.
I_{DQ} = 1A.
$f_p - f_q$ = 1 kHz.

Fig.28 3rd order distortion versus P_O.



2 × BLF177.
V_{DS} = 50 V.
I_{DQ} = 1A.
$f_p - f_q$ = 1 kHz.

Fig.29 5th order distortion versus P_O.



2 × BLF177.
V_{DS} = 50 V.
$f_p - f_q$ = 1 kHz.
f_p = 20 MHz.
P_O = 30 W PEP.

Fig.30 Distortion versus quiescent current.

Linear performance of BLF244 in S.S.B. class-A operation

1 INTRODUCTION

This report contains results of measurements carried out on the BLF244 in S.S.B. Class-A operation. Linear measurements have been performed on six transistors from batch R150C (ass. nr. 3030). Each transistor was taken from a different slice.

2 TESTCIRCUIT

Measurements have been done in a wideband amplifier designed for the frequency range 1.6 – 28 MHz. The circuit diagram and component list are given in Fig.6 and Table 1. Negative feedback (R2) has been employed to attain a flat gain of the amplifier. A shunt resistor (R1) between gate and source takes care of stable operation and also decreases the input resistance to 12.5 Ω. Matching to 50 Ω is accomplished with a 4 : 1 broadband transformer.

At the output side a broadband load of 50 Ω is provided to the transistor. A more detailed description of this kind of amplifiers is given in application report NCO8705.

3 TESTCONDITIONS

The quiescent drain current for class-A operation is set to 0.6 A at a supply voltage of 28 V. This is below the maximum allowable DC-current for a heatsink temperature of 70 °C which is 0.9 A for this device.

Linearity measurements have been performed with two tones of equal amplitude with a frequency seperation of 1 kHz. The intermodulation distortion products d3 and d5 are referred to the amplitude of one of the two tones.

The transistors have been tested at a nominal output power of 4 W PEP, with a heatsink temperature of 25 °C.

4 TESTRESULTS

The table below contains results of measurements at f = 28 MHz of 6 devices.

Conditions: V_{ds} = 28 V; Idq = 0.6 A; Pout = 4 W PEP; Ths = 25 °C.

Batch RI50C (ass.nr.3030)

DEV.NO.-SLICENO.	PIN (mW)	GP (dB)	D3 (dB)	D5 (dB)	INPUT RET.LOSS (dB)
2 – 2	9.0	23.5	–40.5	–60	–20.5
18 – 3	9.0	23.5	–41.0	–60	–22.0
27 – 10	8.8	23.6	–40.5	–60	–24.5
32 – 12	8.9	23.5	–40.5	–60	–22.5
44 – 19	8.8	23.6	–40.5	–60	–24.0
52 – 21	8.8	23.6	–40.5	–60	–23.0

Measurements have also been performed versus output power at f = 28 MHz. Figures 1 and 2 show the powergain and IMD (d3) of a typical device (dev.no.52 from slice 21). Pout is varied between 0.5 W and 8 W P.E.P which resulted in a gain variation of approximately 0.5 dB. IMD (d3) exceeds the level of –40 dB for an output power greater than 4.3 W PEP The amplifier performance versus frequency has also been measured at Pout = 4 W PEP with the same device. Figures 3, 4 and 5 show the powergain, IMD (d3) and input return loss versus frequency. The measuring frequency extends from 1.6 to 32 MHz. The resulted powergain is 24 dB ±0.4dB and IMD (d3) varies between –48 and –40.5 dB while the input return loss is better than –20 dB.

5 CONCLUSION

The BLF244 is suited for linear operation in Class-A in the HF-band. It has an IMD (d3) of better then –40 dB up to an output power of 4 W PEP throughout the band at Vds = 28 V and Idq = 0.6 A.

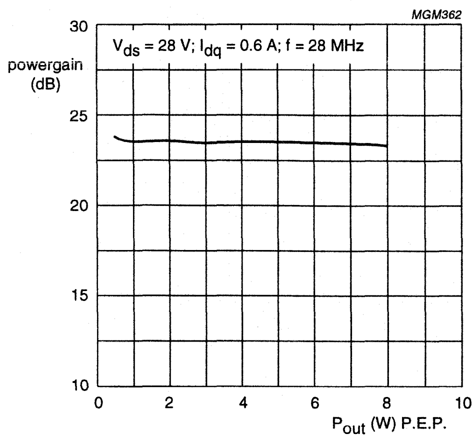


Fig.1 Powergain versus Pout.

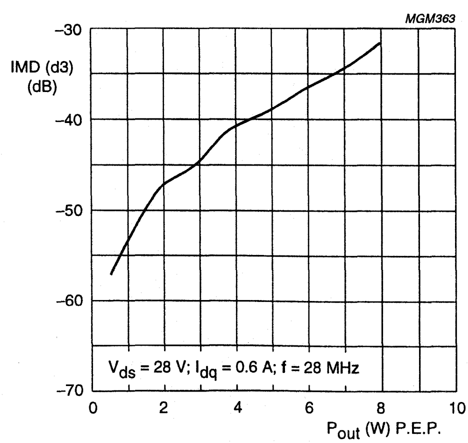


Fig.2 IMD (d3) versus Pout.

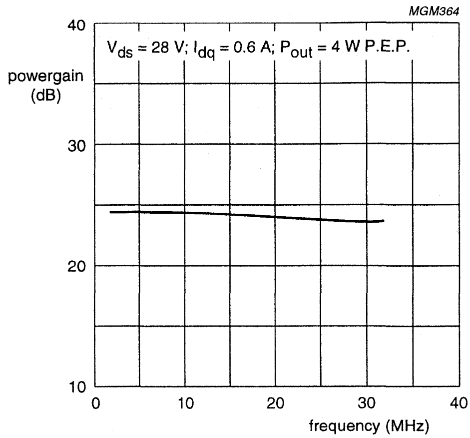


Fig.3 Powergain versus frequency.

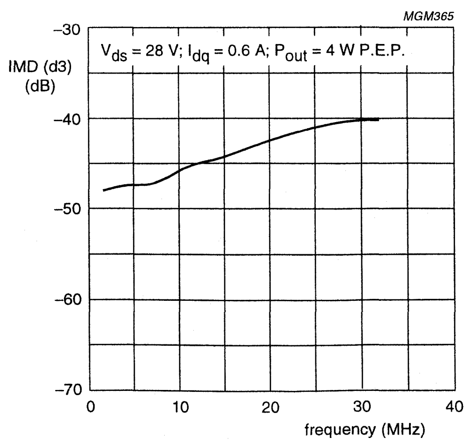


Fig.4 IMD (d3) versus frequency.

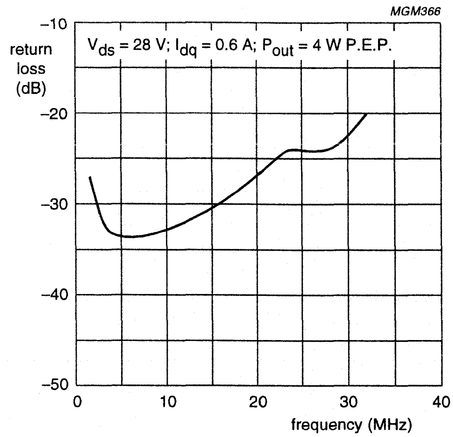


Fig.5 Input return loss versus frequency.

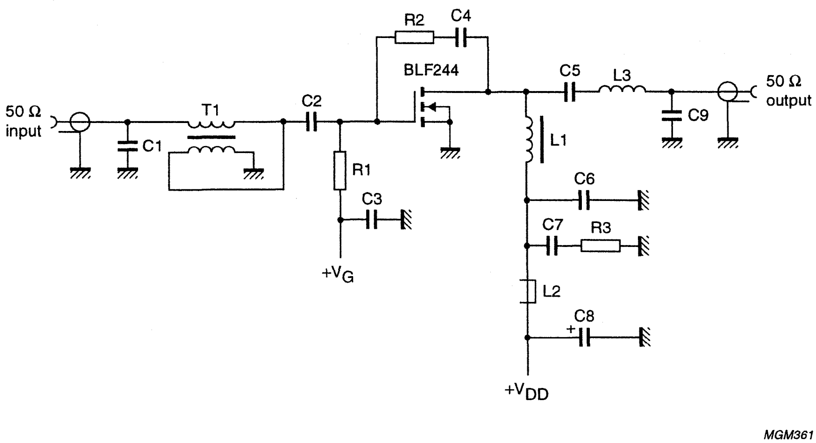


Fig.6 Circuit diagram of the wide band amplifier for BLF244.

Table 1

LIST OF COMPONENTS	
Capacitors	
C1 = 3.9 pF;	multilayer ceramic chip capacitor; note 1
C2 = 3 × 10 nF;	multilayer ceramic chip capacitor; (cat. nr. 2222 852 47103)
C3 = C4 = C6 = 100 nF;	multilayer ceramic chip capacitor; (cat. nr. 2222 852 47104)
C5 = 10 nF;	multilayer ceramic chip capacitor; (cat. nr. 2222 852 47103)
C7 = 3 × 100 nF	multilayer ceramic chip capacitor; (cat. nr. 2222 852 47104)
C8 = 10 µF (63 V);	Aluminium electrolytic capacitor; (cat. nr. 2222 030 28109)
C9 = 24 pF;	multilayer ceramic chip capacitor; note 1
Inductors	
L1 = 20 µH	drain choke, 36 turns enamelled Cu-wire (0.7 mm) wound on a Ferroxcube rod grade 4B1, dimensions (5 × 30) mm
L2 = Ferroxcube RF choke, grade 3B (cat. nr. 4312 020 36640)	
L3 = 189 nH;	8 turns enamelled Cu-wire (1.0 mm); int.dia. = 5.0 mm, length = 9.5 mm; leads 2 × 3.0 mm
Resistors	
R1 = 16 Ω;	metal film resistor; 0.4 W
R2 = 1500 Ω;	metal film resistor; 0.4 W
R3 = 10 Ω;	metal film resistor; 0.4 W
Transformer	
T1 – 4 : 1 transformer	18 turns of twisted pair of 0.25 mm enamelled Cu-wire (10 twists per cm) wound on a toroidal core grade 4C6, dimensions (9 × 6 × 3) mm; (cat. nr. 4322 020 97171)
Printed circuit board: double sided Cu-clad epoxy fibreglass laminate (ε_r = 4.5). Thickness 1/16 inch.	

Note

1. American technical ceramics capacitors type 100B.

A linear amplifier (1.6 – 28 MHz) for 8 W PEP in class-A with the BLF175

Application Note NCO8705

1 SUMMARY

In this report a description is given of a wideband linear amplifier intended for driver applications in SSB transmitters for the frequency range 1.6 to 28 MHz. It employs a MOS-transistor BLF175 suited for a supply voltage of 50 V.
The transistor is adjusted in class-A with a quiescent drain current of 800 mA. The main properties at P_o = 8 W PEP are:

Powergain: 28.3 – 28.6 dB

IMD (d3): ≤ –41 dB

IMD (d5): ≤ –60 dB

Input return loss: ≤ –26 dB.

2 INTRODUCTION

The amplifier that will be discussed in this report concerns a wideband linear amplifier, designed for driver applications is SSB transmitters in the HF band. This design is based on the RF power MOS-transistor BLF175 which is primarily designed for communication purposes in the HF-band. This device can deliver 8 W PEP in class-A at an IMD (d3) < –40 dB, when operated from a supply voltage of 50 V. It is encapsulated in a SOT123 four-lead flange type with a ceramic cap.

3 GENERAL CONSIDERATIONS

One of the most important factors to be considered in the design of driver stages for SSB transmitters is intermodulation distortion. The major cause for intermodulation distortion is the non-linear transfer characteristic of the transistor.
A generally accepted IM distortion figure is < –40 dB. To achieve this, driver stages must be operated in class-A. One of the properties of a class-A amplifier is its low efficiency, which for pre-drivers is of less importance.

The amplifier must have a flat gain response, within a few tenths of a dB. Its response should preferably be superiour to that of the final amplifier of a SSB transmitter. The input return loss versus frequency must be low because, it will possibly form the load of a pre-driver.

4 DESIGN OF THE AMPLIFIER

4.1 Circuit description

Figure 1 shows the basic circuit of this broadband amplifier. Negative feedback combined with parallel input compensation has been applied to obtain flat gain and low input return loss.

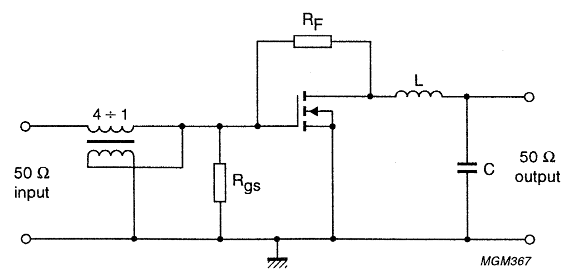


Fig.1 Basic circuit of the wideband amplifier.

Matching of the input to 50 Ω is accomplished with a 4 ÷ 1 broadband transformer of the transmission line type. At the output side a LC-section compensates the output capacitance of the transistor for the frequency range of interest in order to provide the transistor with a constant resistive load.

4.2 Design procedure

The amplifier will be designed for a supply voltage of 50 V and a system impedance of 50 Ω.

First the DC-operating point must be determined. The most important factor that restricts the DC-current in MOS-transistors is the maximum allowable power dissipation in the transistor. For a maximum operating junction temperature of 200 °C and a maximum allowable heatsink temperature of 70 °C the maximum dissipation with R_{thj-h} = 2.9 K/W equals to 44.8 W. This corresponds with a drain current of 0.9 A at V_{ds} = 50 V. In order to keep the dissipation within safe limits I_{ds} is set to 0.8 A.

Second the optimum load resistance is determined. For class-A amplifiers this is given by the relation:

$$R_L = \frac{V_{ds}}{I_{ds}} \qquad (1)$$

In this case R_L equals to $\frac{50}{0.8}$ = 62.5 Ω. In order to avoid an output transformer R_L is chosen to be 50 Ω.

Now the load resistance has been established, the input resistance can be determined. This resistance is formed by the input shunt resistance and that part of the feedback resistance reflected to the input. Several properties of this amplifier are determined by this resistance, viz.:

1. The power gain
2. The cut-off frequency.

In the next sections a brief analysis will be given of this amplifier in order to determine the input resistance and the powergain.

4.2.1 POWERGAIN

For class-A amplifiers small signal analysis produces sufficiently accurate results. The small-signal equivalent circuit of the amplifier is shown in Fig.2. All transistor package parasitics are neglected for this frequency range.

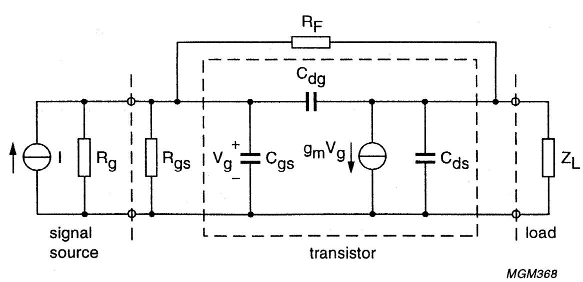


Fig.2 Small signal equivalent circuit of amplifier.

The Y-parameters of the transistor with feedback resistor R_F and shunt resistor R_{gs} are:

$$Y_{11} = G_{gs} + G_F + j\omega(C_{gs} + C_{gd}) \tag{2}$$

$$Y_{12} = -j\omega C_{gd} - G_F \tag{3}$$

$$Y_{21} = g_m - G_F - j\omega C_{gd} \tag{4}$$

$$Y_{22} = G_F + j\omega(C_{ds} + C_{dg}) \tag{5}$$

The general expression for powergain of any linear amplifier is:

$$G_p = \frac{P_o}{P_i} = \frac{G_L |Y_{21}|^2}{|Y_{22} + Y_L|^2 \times \mathrm{Re}(Y_{in})} \tag{6}$$

In which:

$$Y_{in} = Y_{11} - \frac{Y_{12} \times Y_{21}}{Y_{22} + Y_L} \tag{7}$$

The load admittance is:

$$Y_L = G_L - j\omega(C_{ds} + C_{dg}) \tag{8}$$

After substitution of equation (2) to (5) and (7), (8) into (6) we obtain:

$$G_p = \frac{G_L\left[(g_m - G_F)^2 + \omega^2 C_{gd}^2\right]}{(G_L + 2G_F)\left[G_{gs}(G_L + 2G_F) + G_L G + G_F^2 + \omega^2 C_{gd}^2\right]} \tag{9}$$

In which:

$$G = G_F\left(1 + \frac{g_m}{G_L}\right) \tag{10}$$

If G_F and ωC_{gd} are assumed very small with respect to G_L and G_m we get the simple expression:

$$G_p = \frac{g_m^2}{G_L(G_{gs} + G)} \tag{11}$$

4.2.2 CUT-OFF FREQUENCY

The cut-off frequency of this amplifier is dominated by the input circuit. The output circuit has a much higher cut-off frequency and is therefore not relevant. Figure 3 shows the unilaterised small-signal equivalent circuit of Fig.1.

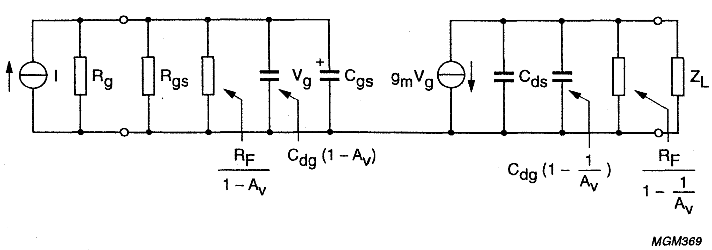


Fig.3 Unilaterised small-signal equivalent circuit.

Av is the voltage gain between drain and gate which is assumed to be a real number. The total input resistance is:

$$R_i = R_{gs} // \frac{R_F}{1 - Av} \tag{12}$$

And the input capacitance is:

$$C_i = C_{gs} + C_{gd}(1 - Av) \tag{13}$$

The 3 dB cut-off frequency of this RC-combination is given by:

$$f_c = \frac{1}{2\pi R_i C_i} \tag{14}$$

So, if C_i is known we can determine R_i for a certain bandwidth.

4.3 Calculation

Calculations are based on transistors from one batch of the BLF175. The mean values of the transistor parameters were taken. These are:

$g_m = 1.5$ S; (Vds = 10 V; Id = 1 A)

$C_{gs} = 145.1$ pF

$C_{ds} = 34.4$ pF; ($V_{ds} = 50$ V; $V_{gs} = 0$ V; f = 28 MHz)

$C_{gd} = 3.42$ pF.

The transconductance (g_m) of this device is determined by a pulse measurement. Under normal operating conditions g_m will be lower due to the higher junction temperature. The reduction is approximately 25% for normal operating conditions. The effective transconductance is therefore:

$g_{me} = 1.5 \times 0.75 = 1.1$ S

The capacitors C_{ds} and C_{gs} are voltage-dependent. Due to RF-excitation the effective capacitance in class-A will be 10% higher, so:

$Cds_e = 1.1 \times C_{ds} = 37.8$ pF
$Cgd_e = 1.1 \times C_{gd} = 3.76$ pF

The voltage gain between drain and gate in Fig.1 can be calculated with:

$$A_V = -g_{me} \times R_L \tag{15}$$

For a load resistance of 50 Ω this amounts to:

$A_v = -1.1 \times 50 = -55$

According to eq. (13) the total input capacitance amounts to:

$C_i = 145.1 + 3.76 \times (1 + 55) = 355.7$ pF

The total input resistance can now be determined with eq. (14). For f = 28 MHz this amounts to:

$$R_i \le \frac{1}{2 \times \pi \times 28 \times 10^6 \times 355.7 \times 10^{-12}} = 16\ \Omega$$

For the ease of transformation a value of 12.5 Ω has been chosen. The cut-off frequency therefore increased to 35.8 MHz.

R_i consists of the parallel connection of R_{gs} and $R_F/(1-A_v)$ see Fig.3. First the feedback resistance R_F will be calculated. The only restriction that holds for the feedback resistance is the power dissipation in it. This must be kept low in order to prevent deterioration in IMD performance. The dissipation allowed, is set to ≈3% of the RMS output power. According to Fig.3 the total reflected feedback resistance to the output side is:

$$R_F' = \frac{R_F}{1 - \frac{1}{A_v}} \tag{16}$$

Because $A_v >> 1$, $R'_F \approx R_F$ and amounts to:

$R_F = 1500\ \Omega$

Now, R_{gs} can be calculated for $R_i = 12.5\ \Omega$. With $R_F/(1 - A_v) = 26.8\ \Omega$ we find for R_{gs} a value of 23.4 Ω. The closest practical value is 24 Ω.

The powergain in dB can be determined with eq. (9), and is calculated to be:

$G_p = 10 \log (636.6) = 28.4$ dB

When the approximate equation is used (11) we get:

$G_p = 10 \log (756.3) = 28.8$ dB

So, a good estimation is obtained when eq. (11) is used.

4.4 Output matching

The output impedance of the transistor can be represented by a parallel connection of a resistance and a capacitance. The resistance has a value of 50 Ω, see Section *"Design procedure"*, and the capacitance is equal to $1.1 \times (C_{ds} + C_{dg}) = 41.6$ pF due to R_F-excitation. This output capacitance is compensated by a LC-section for the frequency range of interest in order to obtain a constant resistive load, see Fig.4.

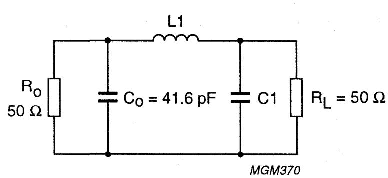


Fig.4 Output matching.

According to Ref. [1] the component values of L_1 and C_1 for a cut-off frequency of 28 MHz are:

$L_1 = 189$ nH and $C_1 = 41.6$ pF with VSWR = 1.05.

The output section contains two additional components, viz.:

1. A drain choke for biasing
2. A dc-blocking capacitor.

For RF-signals the drainchoke is connected in parallel with the output impedance, see Fig.5, and must therefore be large enough, in order to avoid performance degradation at the low end of the band. For the lowest frequency of interest (1.6 MHz) the choke inductance must be at least:

$$L_{ch} = \frac{4R_o}{2\pi f_{min}} \tag{17}$$

In this case L_{ch} amounts to 20 μH. In practice this is obtained by winding 36 turns of enamelled copper-wire (0.7 mm) on a ferroxcube rod, grade 4B1, with a length of 30 mm and a diameter of 5 mm. Because of the open magnetic circuit saturation due to DC-current will hardly occur.

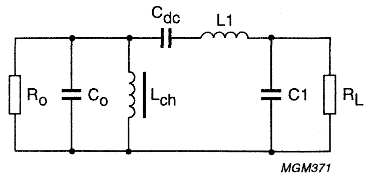


Fig.5 Output section.

The dc-blocking capacitor can be used to compensate the choke inductance for low frequencies. According to [1] this capacitor must be 8 nF for f = 1.6 MHz with $VSWR_{max}$ = 1.03. In practice a chip capacitor was used of 10 nF.

The matching performance of the output section was verified with an impedance analyzer. The transistor was first replaced by a dummy transistor which consisted of a resistor of 50 Ω and a capacitor of 42 pF in a SOT123 header. The return loss was measured at the load connection. It appeared that the return loss improved when C_1 was replaced by a capacitor of 24 pF. This was due to parasitics introduced by the printed circuit board and the additional components like the drainchoke and the blocking capacitor. The return loss was better than –20 dB throughout the band.

4.5 Input matching

The input section is shown in Fig.6.

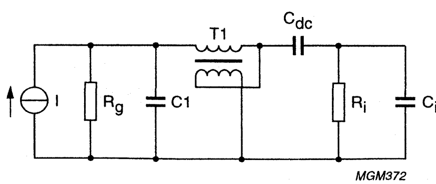


Fig.6 Input section.

A 4 : 1 broadband transformer is applied of the transmission line type. It utilizes a twisted-wire-pair transmission line wound on a toroidal core. The windings are uniformly distributed around the toroid. Figure 7 shows the electrical circuit diagram and constructional details of this transformer.

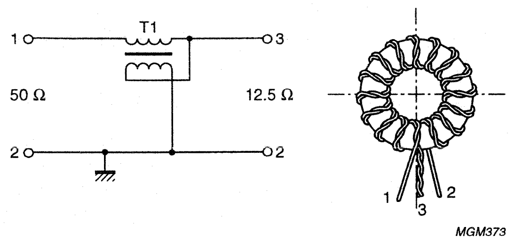


Fig.7 Input transformer.

The required characteristic impedance of the transmission line is:

$$Z_0 = \sqrt{R_g \times R_i}$$

For this case Z_0 equals to $\sqrt{50 \times 12.5} = 25\ \Omega$. In practice Z_0 will deviate from the required value and compensation will be necessary to improve the broadband performance of the transistor. The characteristic impedance of 25 Ω has been obtained by twisting two enamelled copper wires of 0.25 mm-bare diameter. The wire diameter with isolation included was 0.27 mm. Approximately 10 twists per cm were applied and the total wire length was 25 cm.

A ferroxcube toroid, grade 4C6, has been applied with dimensions (9 × 6 × 3) mm. Here the size is not primarily determined by the power handling capabilities, but the required number of turns needed to establish the parallel inductance between the transformer terminals. On the other hand this inductance must not be higher than necessary, because the broadband performance of the transformer will degrade if the transmission line becomes longer than λ/8. A good practical value is that given by equation (17). This means for the inductance at the 50 Ω side a value of 20 μH and for the 12.5 Ω side a value of 5 μH. The number of turns needed is that which is required to make 5 μH. According to the design information in ref. [2], 13 turns for this toroid were required to make 5 μH. From measurements it appeared to be too low. Therefore the number of turns had to be increased to 18. This is due to deviation in material properties which for smaller toroids is larger.

The dc-blocking capacitor compensates the parallel inductance of 5 μH. For 1.6 MHz, 31.8 nF is necessary according to ref. [1]. Three chip capacitors in parallel were used of 10 nF each.

High frequency compensation for deviation in Z_0 is accomplished by parallel capacitors between the transformer terminals. At the low ohmic side a part of C_i provides the required capacitance while at the high ohmic side C_1 provides this. Its value is determined by tuning a variable capacitor for optimum return loss at f = 28 MHz under nominal operating conditions. The required value was 3.9 pF.

5 AMPLIFIER ALIGNMENT

The amplifier was constructed according to the design procedure given in the previous chapter. Measurements were performed throughout the band at an output power of 8 W PEP The results are given below.

Powergain = 27.5 – 28.6 dB

IMD(d3) ≤ –41 dB

IMD(d5) ≤ –60 dB

Input return loss ≤ –18.5 dB.

The highest powergain occurred at f = 1.6 MHz. The total variation in gain of 1.1 dB was found to be relatively large. In order to improve this compensation measures were considered. There were two possibilities, viz.:

1. Parallel input compensation; an inductance in series with the input shunt resistance which increases the effective shunt resistance at high frequencies and hence the gain
2. Feedback compensation: an inductance in series with the feedback resistance witch decreases the feedback at high frequencies and hence improves the gain.

The drawback of the latter is the relatively large inductance required for compensation, a few μH. The former is more elegant because of the low value of the required inductance. Calculation of the optimum inductance for maximally flat response is complicated. Therefore its value was determined in an empirical way. An inductance of 86 nH was found, which reduced the total variation to 0.3 dB for an average gain of 28.4 dB. An additional advantage of this compensation measure was the improvement of the input return loss, which became better than –26 dB.

6 AMPLIFIER CONSTRUCTION

6.1 Construction notes

The circuit diagram and component list are given in Fig.8 and Table 1. The circuit board of this amplifier design is made of two-sided copper clad epoxy fibreglass laminate with a thickness of 1/16 inch and a dielectric constant of 4.5. A full sized pattern of the printed circuit board is shown in Fig.9. The other side is fully metallized and used as ground plane. The ground planes on each side of the board are connected together by means of copper straps at the source leads and the N-connectors and the mounting screws. Figure 9 shows the component layout.

The unavoidable strip in the feedback path represents an inductance of 12 nH and a capacitance of 5.5 pF which can be neglected with respect to the feedback resistance. C4 is a dc-blocking capacitor and should have a low reactance for all frequencies. To prevent low frequency spurious oscillation, a network comprising C7 and R3 is applied. At low frequencies R3 serves as a series loss for choke L2 and thus avoids a high Q factor. C3 and C6 are small bypass capacitors for the carrier frequency. L3 needs to be as large as possible and still be able to handle the required current. C8 must provide a solid bypass at all frequencies including the very low ones.

6.2 Heatsink

The circuit board is attached to a solid brass plate, which is provided with a circular hole for cooling purposes. A water cooling system controls the heatsink temperature.

7 AMPLIFIER PERFORMANCE

7.1 General

Performance measurements were carried out under the following conditions:

Supply voltage: V_{dd} = 50 V

Quiescent drain current: I_{dq} = 0.8 A

Heatsink temperature: T_{hs} = 25 °C

The measuring frequency extends from 1.6 to 32 MHz. Two tones of equal amplitude were used with a frequency separation of 1 KHz. The distortion products were measured with respect to one of the two tones.

7.2 Performance at constant output power

The measurements were done at an output power of 8 W PEP. The results obtained are:

Powergain = 28.3 – 28.6 dB, see Fig.10

IMD (d3) = –41.4 – –47.4 dB, see Fig.11

IMD (d5) = ≤–60 dB

Input return loss ≤–26 dB, see Fig.12.

7.3 Performance at constant frequency

As shown in Fig.11 the worst third order IMD products occurs at the highest end of the band. Therefore, measurements versus output power were only carried out at f = 28 MHz. The results obtained are:

Powergain = 28.1 – 28.4 dB, see Fig.13;

IMD (d3) = –60 – –33.9 dB, see Fig.14 –40 dB is exceeded for $P_o \geq 9.5$ W PEP;

IMD (d5) ≤ –58 dB;

Input return loss ≤ –21.5 dB.

8 CONCLUSION

The design and construction of a wideband linear amplifier has been presented, with the MOS-transistor BLF175, for the frequency range 1.6 – 28 MHz. The transistor is adjusted in class-A and shows good linearity, IMD (d3) ≤ –40 dB, up to an output power of 9.5 W. It is suited for driver applications in SSB transmitters.

9 REFERENCE

[1] H.Nielinger; *"Optimale dimensionering von Breitbandanpassungsnetwerken"*; NTZ 1968, Heft 2, pp. 88–91.
[2] Philips Data handbook; *"Soft Ferrites"*; Book MA01, 1996.

9.1 Circuit diagram of the wideband linear amplifier

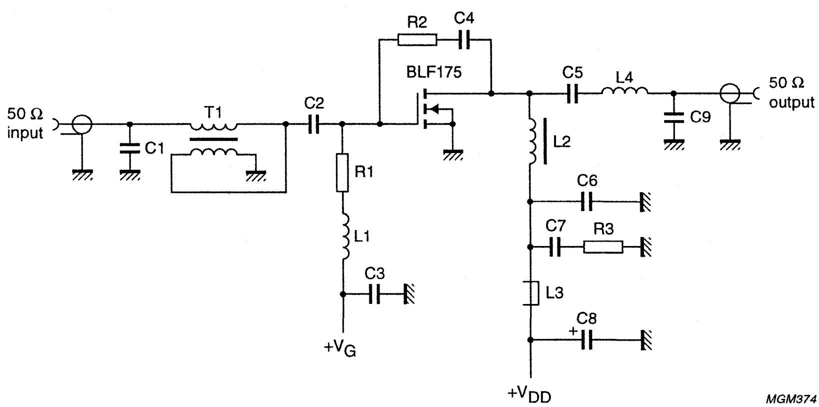


Fig.8 Circuit diagram of the wideband linear amplifier.

Table 1 List of components

Capacitors	
C1 = 3.9 pF	multilayer ceramic chip capacitor; note 1
C2 = 3 × 10 nF	multilayer ceramic chip capacitor; (cat. nr. 2222 852 47103)
C3 = C4 = C6 = 100 nF	multilayer ceramic chip capacitor; (cat. nr. 2222 852 47104)
C5 = 10 nF	multilayer ceramic chip capacitor; (cat.nr. 2222 852 47103)
C7 = 3 × 100 nF	multilayer ceramic chip capacitor; (cat.nr. 2222 852 47104)
C8 = 10 μF (63 V)	Aluminium electrolytic capacitor; (cat.nr. 2222 030 28109)
C9 = 24 pF	multilayer ceramic chip capacitor; note 1
Inductors	
L1 = 86 nH	4 turns enamelled Cu-wire (0.6 mm); int. dia. = 5.0 mm, length = 3.3 mm; leads 2 × 2.0 mm
L2 = 20 μH	drain choke, 36 turns enamelled Cu-wire (0.7 mm) wound on a Ferroxcube rod grade 4B1, dimensions (5 × 30) mm
L3 =	Ferroxcube RF choke, grade 3B (cat.nr. 4312 020 36640)
L4 = 189 nH	8 turns enamelled Cu-wire (1.0 mm); int.dia. = 5.0 mm, length = 9.5 mm; leads 2 × 3.0 mm
Resistor	
R1 = 24 Ω	metal film resistor; 0.4 W
R2 = 1500 Ω	metal film resistor; 0.4 W
R3 = 10 Ω	metal film resistor; 0.4 W
Transformer	
T1 – 4 : 1 transformer	18 turns of twisted pair of 0.25 mm enamelled Cu-wire (10 twists per cm) wound on a toroidal core grade 4C6, dimensions (9 × 6 × 3) mm. (cat.nr. 4322-020-97171)
Printed circuit board: double sided Cu-clad epoxy fibreglass laminate (ε_r = 4.5), thickness 1/16 inch	

Note

1. American technical ceramics capacitor type 100B.

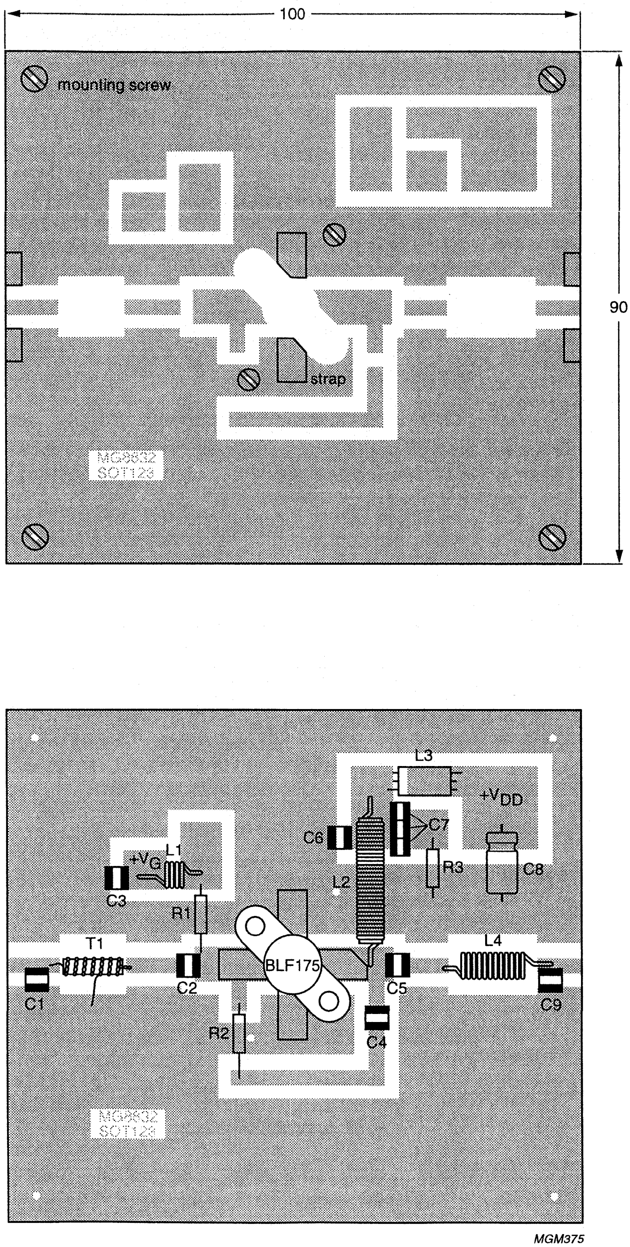
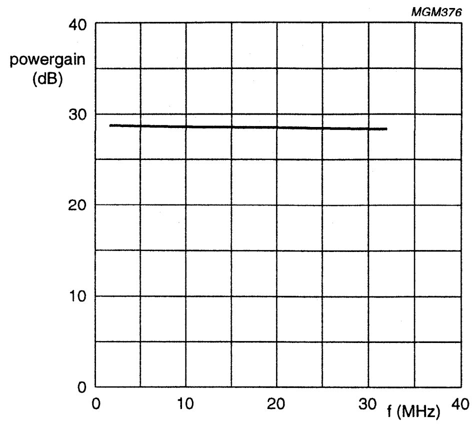


Fig.9 Printed circuit board and component layout.



Conditions:
V_{ds} = 50 V
I_{dq} = 800 mA
P_o = 8 W PEP
T_h = 25 °C.

Fig.10 Powergain versus frequency.

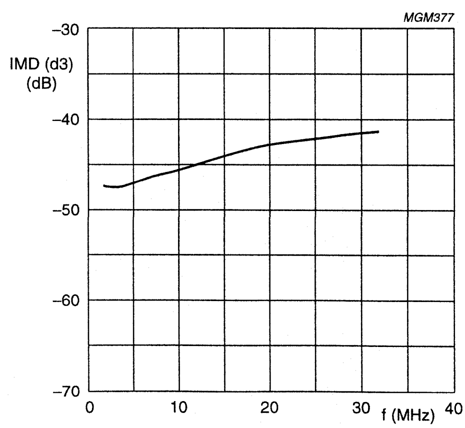
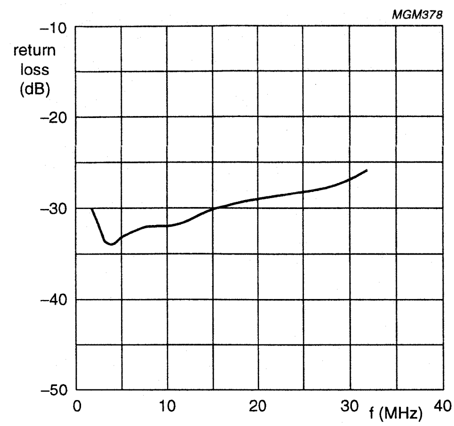


Fig.11 3rd order IMD versus frequency.



Conditions: V_{ds} = 50 V, I_{dq} = 800 mA, Po = 8 W PEP, Th = 25 °C
Tone separation = 1 kHz.

Fig.12 Input return loss versus frequency.

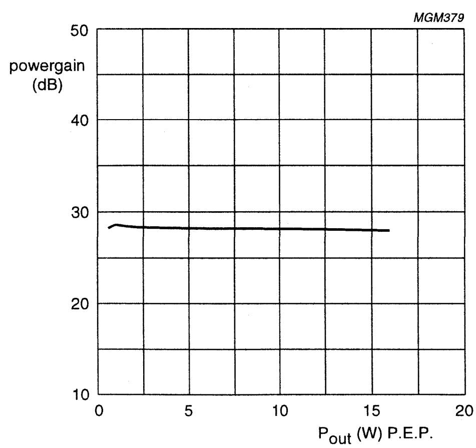
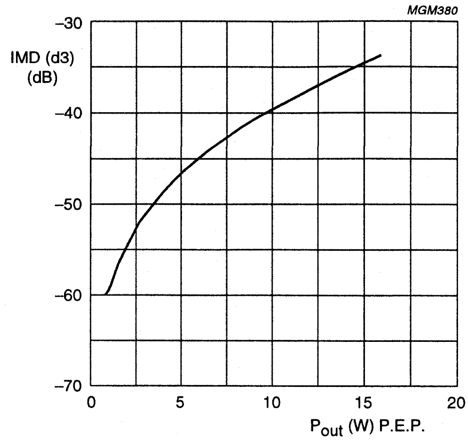


Fig.13 Powergain versus output power.



Conditions: V_{ds} = 50 V, I_{dq} = 800 mA, Th = 25 °C, f = 28 MHz (p–q = 1 kHz).

Fig.14 3th order IMD versus output power.

The BLF246 as an H.F.-S.S.B. amplifier

Application Note
NCO8801

1 SUMMARY

This report gives information on the BLF246 as a linear amplifier at 28 MHz for S.S.B. signals.

Typically the device produces an output power of 80 W P.E.P. at an I.M. distortion of –34 dB.
At a supply voltage of 28 V the power gain is 20 dB and the 2-tone efficiency 40%.

For the design of wideband amplifiers in the range of 1.5 – 30 MHz additional information is presented showing that the power gain drops to appr. 19 dB with a variation of ±0.4 dB.

2 INTRODUCTION

The BLF246 is an R.F. power MOS-transistor in SOT121 package specified at a frequency of 108 MHz and a supply voltage of 28 V for an output power of 80 W C.W.

During the development period this device has also been tested in a class-AB amplifier at 28 MHz to investigate its behaviour as a linear amplifier for possible application in the H.F. band (1.5 – 30 MHz) with S.S.B. modulation.
In that case the 3rd and 5th order intermodulation products are of special interest.

3 NARROW BAND TEST AT 28 MHz

The R.F. circuit used for this purpose is depicted in Fig.1. The optimum drain quiescent current for linear operation of this device in class-AB in 0.6 A.
This is achieved with a Vgs which is appr. 0.48 V higher than the specified Vgs(th).

The output circuit has been aligned with a dummy load consisting of the parallel connection of a 3.5 Ω resistor and a 400 pF capacitor. This results in a load seen by the transistor of appr. 3.3 Ω with a negligible reactive part.

The capacitors C9 and C10 are used to reduce the second harmonic voltage at the drain.
In a wideband amplifier this is not necessary because the same effect is obtained by other means like a centre-tapped drain choke in a push-pull amplifier.

The input circuit is aligned for minimum reflection at 50% of the maximum output power.

The gate-source damping resistors R1 and R2 are needed for 2 reasons:

1. Stability i.e. to prevent oscillation when the output circuit is detuned
2. Low intermodulation distortion. In general it can be said that I.M. distortion is improved by lowering the value of these resistors. Of course they will influence the power gain of the amplifier.

The average performance of the BLF246 in this amplifier is shown in Figs 2, 3, 4 and 5.

At an output power of 80 W P.E.P. the average performance is:

Gp = 20 dB

Eff. = 40% (2-tone)

d3 = –34 dB

d5 = –42 dB.

The distortion products have been measured with respect to one tone.

It must be mentioned that the information given here is typical i.e. it is not guaranteed by measurements on individual transistors.

4 WIDEBAND OPERATION

For operation in the H.F. range (1.5 – 30 MHz) it will be necessary to reduce the value of Rgs from 18 Ω as used in the narrow band amplifier down to 12 Ω to obtain a more constant power gain over the band and to achieve a smaller variation in the input impedance to allow an easier matching to a driver stage or a 50 Ω source.

Table 2 shows the results of a computer calculation on this basis. It appears that the power gain is reduced by appr. 1 dB while the gain variation is then ±0.4 dB.

The optimum load impedance is still appr. 3.3 Ω with a negligible reactive part.

It must be mentioned that the figures given for power gain and input impedance include already the effects of an Rgs of 12 Ω.

As mentioned earlier the lowering of Rgs has a positive effect on the intermodulation behaviour.

For the design of a suitable wideband input matching network one is referred to application report nr. NCO8703.

5 ACKNOWLEDGEMENT

The 28 MHz amplifier described in this report was designed and constructed by Mr. G. Lukkassen of our laboratory. He also made the various measurements.

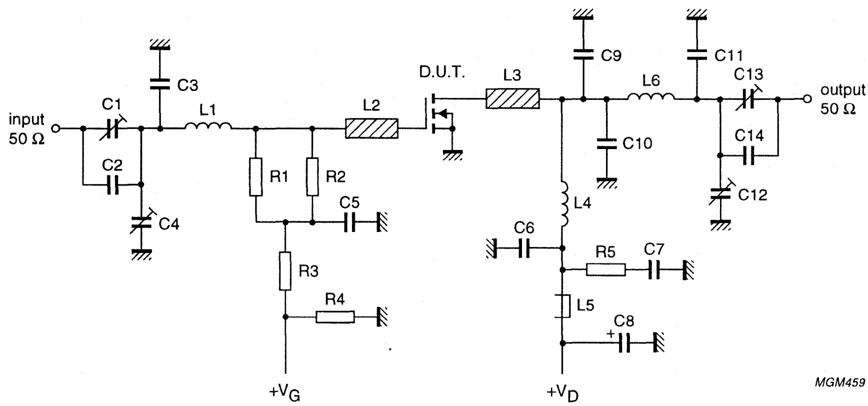


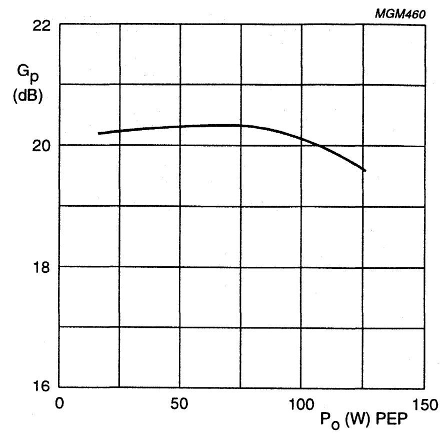
Fig.1 BLF246 Testcircuit at 28 MHz.

Table 1 PC-board: double Cu-clad, 1.6 mm PTFE fibre-glas dielectric (ε_r = 2.2)

C1 = C4	6 to 80 pF	film dielectric trimmer (cat.nr. 2222 809 07013)
C2	62 pF	multilayer ceramic chip capacitor; note 1
C3	150 pF	multilayer ceramic chip capacitor; note 1
C5 = C6	100 nF	multilayer ceramic chip capacitor (cat.nr. 2222 852 47104)
C7	3 × 100 nF	multilayer ceramic chip capacitor (cat.nr. 2222 852 47104)
C8	2.2 µF	electrolytic capacitor
C9 = C10 = C14	75 pF	multilayer ceramic chip capacitor; note 1
C11	100 pF	multilayer ceramic chip capacitor; note 1
C12 = C13	7 to 100 pF	film dielectric trimmer (cat.nr. 2222 809 07015)
L1	184 nH	6 turns enamelled Cu-wire (0.7 mm), int.dia: 6 mm
L2 = L3	41.1 Ω	stripline (10 × 6 mm)
L4	278 nH	7 turns enamelled Cu-wire (1.5 mm), int.dia: 8 mm
L5		Ferroxcube h.f. coke, grade 3B (cat.nr. 4312 020 36642)
L6	131 nH	4 turns enamelled Cu-wire (1.5 mm), int.dia: 8 mm
R1 = R2	34.8 Ω	metal film resistor (cat.nr. 2322 153 53489)
R3	1 kΩ	metal film resistor (cat.nr. 2322 151 71002)
R4	1 MΩ	metal film resistor (cat.nr. 2322 151 71005)
R5	10 Ω	metal film resistor (cat.nr. 2322 153 51009)

Note

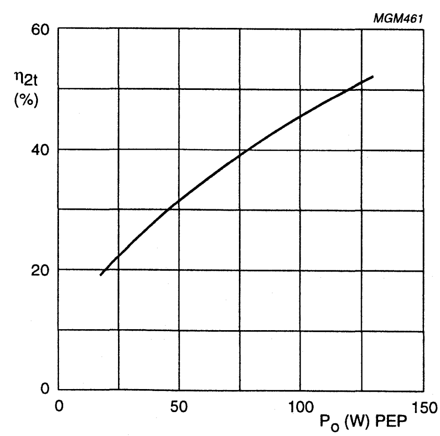
1. American Technical Ceramics type 100B or capacitor of same quality.



Conditions

f = 28 MHz	Idq = 0.6 A	Th = 25 °C
Vds = 28 V	Rgs = 18 Ω	Rth mb-h = 0.2 K/W

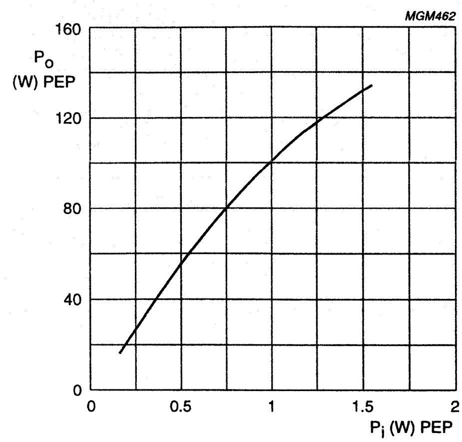
Fig.2 Power gain versus output power.



Conditions

f = 28 MHz	Idq = 0.6 A	Th = 25 °C
Vds = 28 V	Rgs = 18 Ω	Rth mb-h = 0.2 K/W

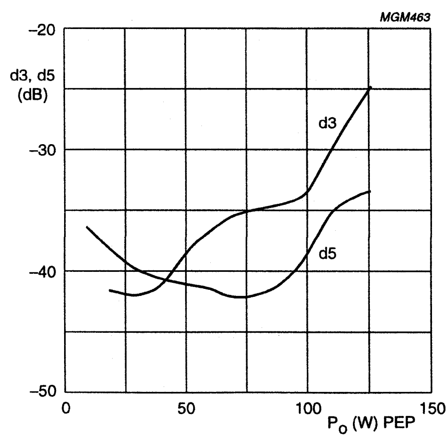
Fig.3 2-tone efficiency versus output power.



Conditions

f = 28 MHz	Idq = 0.6 A	Th = 25 °C
Vds = 28 V	Rgs = 18 Ω	Rth mb-h = 0.2 K/W

Fig.4 Output power versus drive power.



Conditions

f = 28 MHz	Idq = 0.6 A	Th = 25 °C
Vds = 28 V	Rgs = 18 Ω	Rth mb-h = 0.2 K/W

Fig.5 Intermodulation distortion versus output power.

Table 2 Power gain, input and load impedance versus frequency; Idq = 0.6 A; Rgs = 12 Ω

BLF246	V_{DS} = 28 V	P_O = 80 W P.E.P.	Class-AB
f	**G**	**Inp.Imp.**	**Load Imp.**
MHz	**dB**	**Ω**	**Ω**
1.5	19.57	11.97 – j0.51	3.34 + j0.01
5.0	19.54	11.71 – j1.67	3.34 + j0.02
10.0	19.47	10.92 – j3.06	3.33 + j0.04
15.0	19.35	9.86 – j4.03	3.32 + j0.07
20.0	19.20	8.75 – j4.59	3.31 + j0.09
25.0	19.00	7.72 – j4.84	3.30 + j0.11
30.0	18.77	6.83 – j4.86	3.28 + j0.13

Power transformers for the frequency range of 30 – 80 MHz

Technical Publication ECO7703

1 ABSTRACT

In this report design information is given for transformers with a power handling capability up to 300 W in the frequency range of 30 – 80 MHz.

The most suitable core material is ferrite type 4C6. The efficiency of these transformers is typically 98%.

2 SUMMARY

In this frequency range only transmission line transformers can be used. For the windings coaxial cables with P.T.F.E. isolation are recommended.

The size of the core is based on a 1% power loss and a dissipation of 350 mW/cm^3 corresponding with a flux density of 6 Gauss at 80 MHz.

The required number of turns is determined by the ratio $R_P/L = 860\ \Omega/\mu H$ in which R_P is the loss resistance and L the inductance in parallel with the input or output terminals.

In the appendix the relation between the above mentioned quantities is derived.

In the report a practical example is given of a symmetrical 1 : 4 impedance transformer with a power handling capability of 120 W.

3 INTRODUCTION

In Ref.1 information was given on the design of power transformers mainly intended for the frequency range of 1.6 to 28 MHz. In this report some additional information will be presented for the frequency range of 30 to 80 MHz.

4 CHOICE OF CORE MATERIAL

The best available ferrite for this frequency range is 4C6. In this material a series of toroids can be obtained in different sizes according to Table 1.

Table 1

D(1) (mm)	d(2) (mm)	h(3) (mm)	A(4) (mm^2)	A/1(5) (mm)	V(6) (mm^3)
36	23	15	97.7	1.06	8 500
23	14	7	31.5	0.552	1 790
14	9	5	12.5	0.351	445
9	6	3	4.51	0.193	105

Notes

1. Outside diameter.
2. Inside diameter.
3. Height.
4. Cross-section.
5. Average length of the lines of force.
6. Volume.

5 POWER HANDLING CAPABILITY

An important question in the design of a power transformer is how much R.F. power can be handled by a given toroid. Restricting ourselves to the core losses at this moment it can be said that these losses are highest at the maximum frequency of operation i.e. 80 MHz.

From practical experience we have found that a core dissipation of 350 mW/cm^3 can be allowed without excessive rise of the core temperature. As it is a realistic target to keep the core losses below 1% of the power handled by the transformer we come to the following recommendations for the power handling of the different toroids (see Table 2).

Table 2

$D \times d \times h$ (mm^3)	P_{RF} (W)
$36 \times 23 \times 15$	300
$23 \times 14 \times 7$	60
$14 \times 9 \times 5$	15
$9 \times 6 \times 3$	3

The core dissipation of 350 mW/cm^3 mentioned above corresponds with a flux density of 6 Gauss at 80 MHz as can be found in earlier versions of Data Handbook MA01 of Philips series on Magnetic Products: Soft ferrites.

6 DETERMINATION OF THE NUMBER OF TURNS

In the frequency range of 30-80 MHz the number of turns is entirely determined by the loss resistance in parallel with the input or output terminals of the transformer being caused by the core losses. According to the Appendix the core loss figures given Chapter 5 can be expressed in another way, viz:

$$\frac{R_P}{L} = \frac{\omega^2 B^2_{max}}{2\mu_o\mu_r} \times \frac{V}{P_L}$$

in which:

R_p = loss resistance in parallel with input or output terminals

L = inductance in parallel with input or output terminals

B_{max} = maximum flux density

μ_r = relative permeability being typ. 120 for 4C6 material

V = volume of transformer core

P_L = power loss in core.

Using the figures given in Chapter 5 we get:

$$\frac{R_P}{L} = 860\Omega/\mu H \text{ at } f = 80 \text{ MHz.}$$

This ratio is hardly dependent on the flux density and therefore it is very useful for defining the number of turns as will be shown by a practical example in Chapter 8.

Applying the above mentioned criterion ensures a sufficiently high reactance in parallel with the input or output terminals at the lowest frequency of operation. So this reactance caused by the inductance of the winding needs no compensation.

7 WINDING LOSSES

In this frequency range conventional transformers can not be used because of their stray-inductance. The only suitable type is the transmission line transformer. For the windings we can choose a.o:

Twisted enamelled copper wire

Miniature twin lead

Coaxial cable with P.T.F.E. isolation, available in several diameters and characteristic resistances.

The first and second are not recommended for high power operation. The third type is e.g. available in 50 Ohms version with diameters of 1.7 and 2.8 mm. Some important properties of these cables at 80 MHz are given in Table 3.

Table 3

Outside diameter	1.7	2.8	mm
Power loss	0.40	0.24	dB/m
Power handling capability	100	200	W

At lower frequencies the power loss is less and the power handling capability higher.

8 PRACTICAL EXAMPLE

Suppose that in a 100 W transmitter the output transistors are connected in push-pull. The optimum load impedance between the collectors is 12.5 Ω and this must be transformed to 50 Ω. Then we need a symmetrical 1 : 4 impedance transformer plus a balun. The first one will be worked out in detail. A schematic diagram is given in Fig.1.

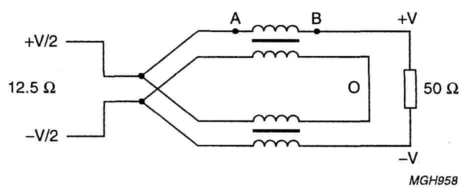


Fig.1 Schematic diagram

From Table 2 we see that this transformer can be made with one 36 mm toroid but also with two 23 mm toroids, in which case the power handling capability is still 120 W. The latter solution is more attractive because it is smaller.

The optimum characteristic impedance for each winding is 25 Ω which can realized by the parallel connection of two 50 Ω cables of 1.7 mm diameter. As the power is transported through 4 cables, each cable is loaded with 25 W being a quarter of the allowable maximum.

The number of turns will be calculated with the 50 Ω output terminals as a reference point. To keep the core losses below 1% we must keep the parallel loss resistance above 5000 Ω. This means an inductance of: $L = \frac{R_P}{860} = \frac{5000}{860} = 5.81\mu H$ (see Chapter 6).

Between the points A and B in Fig.1 the voltage is one quarter of the output voltage. This means that the inductance between these points must be one sixteenth of that across the output terminals, so: $L_{AB} = \frac{L}{16} = \frac{5.81}{16} = 0.363\mu H$

Now the number of turns can be calculated with: $n = \sqrt{\frac{L1}{\mu_o \mu_r A}} = 1.48$

In practice we will choose of course 2 turns by which the core losses reduce to: $\left(\frac{1.48}{2}\right)^2 \times 1\% = 0.55\%$

The inductance in parallel with the output terminals rises to: $\left(\frac{2}{1.48}\right)^2 \times 5.81 = 10.6\mu H$

This corresponds to a reactance of 2000 Ω at 30 MHz which is high enough to be neglected.

To realize the windings cables are required with a length of appr. 98 mm giving a cable loss of 0.039 dB or 0.91%.

So the total calculated loss of this transformer is:

0.55 + 0.91 = 1.46% at f = 80 MHz.

8.1 Reference:

Application report no. ECO6907 ‘Design of H.F. Wideband Power Transformers’ by A.H. Hilbers, June 17th, 1970.

9 APPENDIX

In the Data Handbook, as given in Chapter 5, curves are given showing the core losses expressed in kW/m³ or mW/cm³ versus the flux density B with the frequency as a parameter. It is often useful to know what this means in terms of an equivalent loss resistance in parallel with the inductance. The power dissipated in this resistance is equal to:

$$P_L = \frac{E_{max}^2}{2R_p} \tag{1}$$

On the other hand:

$$B_{max} = \frac{E_{max}}{\omega A n} \tag{2}$$

Eliminating E_{max} in (1) and (2) gives:

$$P_L = \frac{\omega^2 B_{max}^2 A^2 n^2}{2R_p} \tag{3}$$

Further we know that:

$$L = \frac{\mu_o \mu_r n^2 A}{l} \tag{4}$$

So that:

$$n^2 A = \frac{Ll}{\mu_o \mu_r} \tag{5}$$

Substituting (5) in (3) we get:

$$P_L = \frac{\omega^2 B_{max}^2 ALl}{2\mu_o \mu_r R_p} \tag{6}$$

The product Al is equal to the volume of the core V, so that:

$$\frac{P_L}{V} = \frac{\omega^2 B_{max}^2}{2\mu_o \mu_r} \times \frac{L}{R_P} \tag{7}$$

or:

$$\frac{R_p}{L} = \frac{\omega^2 B_{max}^2}{2\mu_o \mu_r} \times \frac{V}{P_L}$$

Wideband class-A power amplifier for TV transposers in band I (50 – 80 MHz) with two transistors BLV33

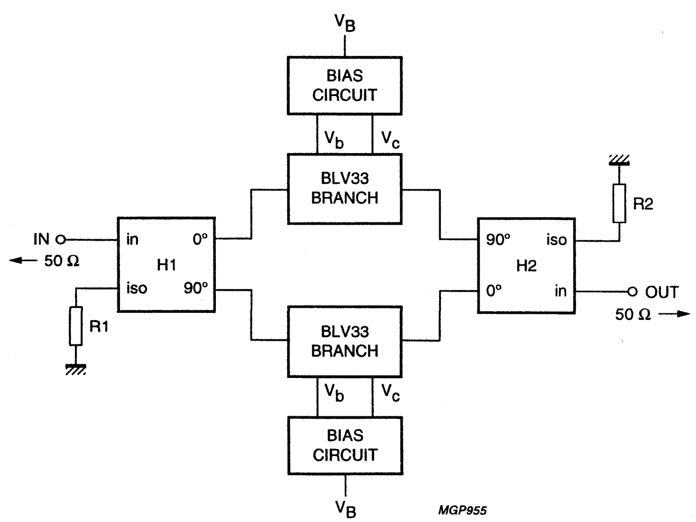
1 SUMMARY

The transistor BLV33 is primarily intended for use in linear VHF amplifiers for television transmitters and transposers. In report ECO7904 Mr. Zwanen describes the application of the BLV33 in a transposer amplifier for the TV band III (174 to 230 MHz).
On customers request we have made a theoretical design of such a linear transposer amplifier for the TV band I (50 to 80 MHz).

2 EXPECTED PERFORMANCE

Frequency range	band I 50 to 80 MHz
Gain	17.4 dB ± 0.3 dB
Input VSWR	≤1.25
Output VSWR	≤1.25
Output power P_{Osync}	
at –60 dB int	≤30 W
at –55 dB int	≤45 W
Cross modulation at P_{Osync} = 40 W	≤7.5%
D.C. setting BLV33	I_C = 3.2 A/V_{CE} = 25 V

Figure 1 shows the schematic line-up of the complete amplifier and Fig.2 gives the circuit of one BLV33 branch. The applied bias-unit has been described in report ECO7904.



H1 = H2 = hybrid coupler Anaren type 1A0230-3.
R1 = R2 = 50 Ω resistor type Pyrofilm PPR 515-20-3.

Fig.1 Schematic line-up of the amplifier.

Wideband class-A power amplifier for TV transposers in band I (50 – 80 MHz) with two transistors BLV33

NCO8207

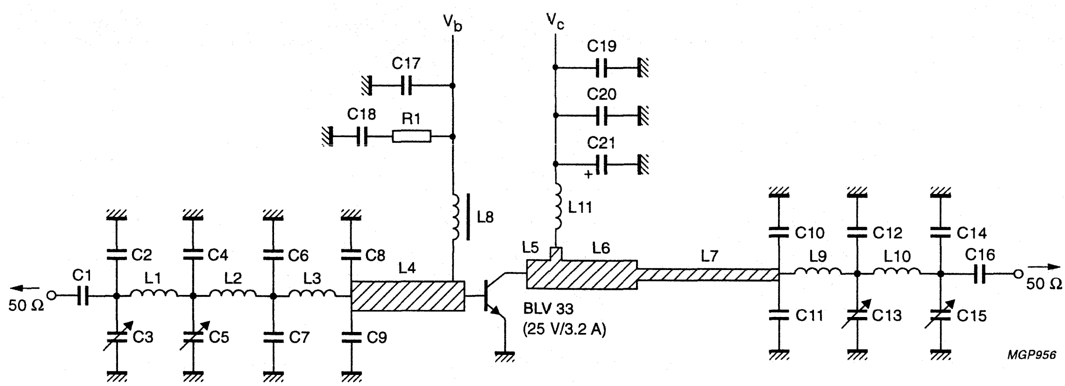


Fig.2 Circuit of a BLV33 branch.

3 PARTS LIST

C1 = C16 = C17 = C19	2k7	chip capacitor Philips cat. no. 2222 852 13272
C2 = C14	39 pF	chip capacitor ATC 100B
C3 = C5	0 to 18 pF	film dielectric trimmer Philips cat. no. 2222 809 05003
C4	110 pF	chip capacitor ATC 100B
C6 = C7	82 pF	chip capacitor ATC 100B
C8 = C9	300 pF	chip capacitor ATC 100B
C10 = C11	160 pF	chip capacitor ATC 100B
C12	150 pF	chip capacitor ATC 100B
C13 = C15	0.40 pF	film dielectric trimmer Philips cat. no. 2222 809 07009
C18 = C20	330 nF	polyester capacitor Philips cat. no. 2222 352 25334
C21	47 μF	eleco Philips cat. no. 2222 030 37479
L1	103 nH	5 turns enamelled C_u-wire, ∅ 1 mm, int.diam. D = 5.5 mm length 7.6 mm, leads 2 × 5 mm
L2	61.3 nH	5 turns enamelled C_u-wire, ∅ 1 mm, int.diam. D = 4.5 mm length 10.6 mm, leads 2 × 5 mm
L3	27.1 nH	3 turns enamelled C_u-wire, ∅ 1 mm, int.diam. D = 4.4 mm, leads 2 × 5 mm
L4	30.1 Ω	stripline, width 6 mm, length l = 30 mm
L5	30.1 Ω	stripline, width W = 6 mm, length l = 5 mm
L6	30.1 Ω	stripline, width W = 6 mm, length l = 10.6 mm
L7	60.2 Ω	stripline, width W = 2 mm, length l = 35.5 mm
L8	1 μH	choke Philips cat. no. 4322 057 01081
L9	43.8 nH	4 turns enamelled C_u-wire, ∅ 1.5 mm, int.diam. D = 4.5 mm length 11.3 mm, leads 2 × 5 mm
L10	87.5 nH	5 turns enamelled C_u-wire, ∅ 1.5 mm, int.diam. D = 6.5 mm length 15.1 mm, leads 2 × 5 mm
L11 = L10		
R1	10 Ω	metal film resistor

Printed-circuit board material is epoxy fibre-glass ($\varepsilon_r \approx 4.5$), thickness 1/16".

SUMMARY

For transmitters and transposers for the FM broadcast band (87.5 – 108 MHz), a 300 W push-pull amplifier using two BLV25 transistors has been designed and built. The transistors operate in class-B from a 28 V supply. In addition, a suitable single-stage driver amplifier using a BLW86 transistor also operating in class-B from a 28 V supply has been designed and built.

Table 1 shows the main properties of each amplifier and of the driver/final-amplifier combination. The driver and final amplifier have been aligned at output powers of 45 W and 300 W respectively.

The 2× BLV25 amplifier has a heatsink with forced air cooling and a 10 mm copper plate heat-spreader.

Table 1 Amplifier performance overview; note 1

FM BAND 87.5 – 108 MHz	BLW86 DRIVER P_{OUT} = 45 W		2 × BLV25 FINAL AMPLIFIER P_{OUT} = 300 W		COMBINATION AMPLIFIER BLW86 AND 2 × BLV25 P_{OUT} = 300 W	
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Gain (dB)	12	13	10.4	11	22.6	25
Input VSWR	1.2	1.3	1.45	1.70	1.1	1.85
Efficiency (%)	69	72	70	71	63	66

Note

1. Circuit board: double copper-clad epoxy fibre glass (ε_r = 4.5), thickness 1⁄16-inch.

1 INTRODUCTION

The BLV25 power transistor is intended for use in FM broadcast transmitters and transposers. This transistor which is in a 6-lead flanged package with ½-inch ceramic cap (SOT119) can deliver 175 W output power at 108 MHz. This report describes the design and practical implementation of a 300 W wideband push-pull amplifier for the FM broadcast band using two BLV25 transistors operating in class-B from a 28 V supply voltage. In addition, a suitable driver amplifier is described. The driver is a single-stage amplifier designed for an output power of 45 W using a BLW86 transistor which also operates in class-B from a 28 V supply. The BLW86 is in a ⅜-inch, 4-lead flanged package with a ceramic cap (SOT123).

2 AMPLIFIER DESIGN THEORY

First, consider the BLV25 transistor. Table 2 gives some of its characteristics at an output power of 160 W and a supply voltage of 28 V.

The output of a BLV25 can be accurately represented by the equivalent circuit of Fig.1. In Section 3.2, it will be explained how the information in Table 2 and Fig.1 are used to align the amplifier.

Figure 2 shows a schematic of the amplifier; Fig.3 shows the complete circuit.

Table 2 Some characteristics of the BLV25 at several frequencies in the FM broadcast band

Freq. f (MHz)	POWER GAIN G (dB)	INPUT IMPEDANCE Z_i (Ω)	OPTIMUM LOAD IMPEDANCE Z_L (Ω)
87.5	11.8	0.54 + j0.38	1.96 – j0.04
92.2	11.5	0.56 + j0.43	1.94 – j0.06
97.2	11.1	0.58 + j0.48	1.91 – j0.07
102.5	10.8	0.60 + j0.53	1.88 – j0.08
108.0	10.4	0.63 + j0.59	1.84 – j0.11

2.1 The output network

The output network consists of three parts:

1. The combination of L_9, L_{10} and C_8 which transforms the output impedance of the transistors to a resistance of 12.5 Ω (balanced).
2. The transmission lines L_{11} and L_{12} which are connected such that they perform a 1:4 impedance transformation, making the output impedance of this part 50 Ω (balanced).
3. The transmission lines L_{13} and L_{14} which function as a balanced-to-unbalanced transformer (balun), so their output impedance is 50 Ω (unbalanced).

Note on 1:
The matching section L_9, L_{10} and C_8 is rather conventional except that the inductors have been replaced by striplines.

Note on 2:
Lines L_{11} and L_{12} are transmission lines with a characteristic resistance of 25 Ω. They are soldered to a copper track on the p.c. board. This track is 2.8 mm wide, so its characteristic impedance with reference to the ground plane of the p.c. board is 50 Ω.

Theoretically, their lengths should be ¼ wavelength for the centre of the frequency band, namely 42 cm. As this is rather impractical, we must find a way to use shorter lines. Two possibilities exist:

Lines L_{11} and L_{12} are not soldered to tracks on the p.c. board but are surrounded by ferrite tubes of suitable dimensions and material. Finding the correct combination is however somewhat involved.

The lengths of lines L_{11} and L_{12} are reduced significantly and the parallel inductance introduced is compensated by increasing the value of C_8. As this method provides good results, it has been adopted.

Note on 3:
The line L_{14} is a transmission line with a characteristic resistance of 50 Ω. It is also soldered to a 2.8 mm wide track on the p.c. board. For the length of this line, the story is similar to that of the 1:4 impedance transformer. By making the line shorter than a ¼ wavelength, an inductance is introduced from point B (Fig.2) to ground. To restore the symmetry, an equal inductance must be introduced between point A and ground. This is done by means of line L_{13} which is a 2.8 mm wide track on the p.c. board of the same length as L_{14}. Finally, the parallel inductances (from point A to ground, and from point B to ground) are compensated by the series capacitors C_9 and C_{10}.

After initial calculation of the separate sections and their compensation, the network was optimized using a computer optimization program. The final dimensions of the components can be found in Fig.3.

The maximum VSWR of this network is <1.05.

A remark must be made about the reactive loading of C_8 which is nearly 900 VA at 108 MHz, so a high-quality capacitor must be used. Two or three capacitors in parallel can also be considered.

2.2 The input network

This network is very similar to the output network and, like it, consists of three parts:

1. The combination of L_1 and L_2 forms an unbalanced-to-balanced transformer whose output impedance is 50 Ω (balanced)
2. The combination L_3 and L_4 forms a 4:1 impedance transformer whose output impedance is 12.5 Ω (balanced)
3. The components L_5 to L_8 and C_3 to C_7 form a two-section matching network to match the input impedances of the transistors to 12.5 Ω (balanced).

All the remarks made for the output network also apply to the input network, though several values are different.

The calculation of the input network was made in the same way as that for the output network. However, the total length of the lines L_1 to L_4 became too long for practical use. After dividing the lengths of these lines by 1.6, the other components were re-optimized, raising the input VSWR from 1.20 to 1.27. All component values are given in Table 5.

A consequence of this way of designing is that the power gain at 87.5 MHz is approximately 1.4 dB higher than that at 108 MHz. This variation must be compensated in one of the driver stages.

An alternative design with a nearly flat power gain of about 10 dB can be made, however, the input matching is only good at the high end of the frequency band; at 87.5 MHz, the input VSWR rises to about 3.2. Further details of this alternative are not given here.

2.3 Bias components

Theoretically, point V_B can be grounded directly. However, it may be better to ground it via an RF choke shunted by a 12 Ω resistor as shown in Fig.4 because of:

- Small asymmetries in the transistors and circuit, and
- Possible parasitic oscillation when the transistors operate in parallel rather than push-pull.

Resistors R_1 and R_2 have been added to improve stability during mismatch. For point V_C, the same holds as for point V_B, except that the supply voltage must be connected to the former. In the simplest configuration, point V_C is decoupled for RF frequencies. A better proposition is probably the circuit shown in Fig.5.

3 PRACTICAL 300 W PUSH-PULL AMPLIFIER WITH 2 × BLV25

3.1 General remarks

Having established a theoretical design, let us now look at a practical implementation.

The amplifier has been designed on a double copper-clad epoxy fibre glass ($\varepsilon_r = 4.5$) board, thickness $^1/_{16}$-inch. Figure 6 shows the print board and Fig.7 the layout of the amplifier. Rivets and, at the board edges, soldered copper straps have been used to provide good contact between both sides of the board. Where the emitters are grounded, contact is made with the lower side of the board.

The print board and transistors are attached to a 10 mm thick copper plate which acts as a heat-spreader. This plate is screwed to a standard heatsink with forced air cooling. At an ambient temperature of 25 °C, and with the amplifier operating at 300 W output power, the heatsink temperature is below 55 °C.

3.2 Alignment

The first alignment was done with small signals, starting with the output circuit. The BLV25 transistors were replaced by dummy loads, representing the complex conjugate of the optimum load impedance. The dummy consists of a 2.22 Ω resistance and a 300 pF capacitance.

To reduce parasitic inductance and to maintain the best possible symmetry, we used several components in parallel. These components were soldered to an empty SOT119 header.

The reflection versus frequency was measured at the output terminal and minimized by adjusting the capacitors C_{16}, C_{14}, C_{15} and C_9. Figure 8 shows the schematic diagram and Fig.9 the return losses; the VSWR remains below 1.13.

The alignment of the input network was done with the transistors in circuit and with the supply voltage and load connected. First, alignment was made with the transistors in class-A (I_C = 1.7 A and V_{CE} = 25 V). The reflection versus frequency was then minimized at small-signal levels. Then the operation was altered to class-B, and the amplifier realigned at an output power of 300 W. The required circuit modifications were rather small. Figure 10 shows the final circuit. Resistances R_2 and R_3 are necessary to prevent parallel oscillations. The inductance of these resistors is very important (see Table 6).

In spite of the dummy adjustment of the output circuit, the capacitance of C_9 had to be reduced to improve the collector efficiency, η, of the amplifier. In addition, three capacitors in parallel have been used because of the very high reactive loading at that point.

3.3 Performance

The amplifier has been aligned at an output power of 300 W. Figures 11 to 13 show the gain, input VSWR and collector efficiency as functions of frequency at 300 W output power. Figure 14 shows the variation of efficiency with output power, both measured at 108 MHz.

4 BLW86 DRIVER AMPLIFIER

4.1 Amplifier Design

The required drive power for the 2× BLV25 amplifier described in Section 3 is about 30 W. The input VSWR of this final amplifier varies between 1.45 and 1.7 (see Fig.12), so the load impedance of the driver amplifier differs from 50 Ω and varies with frequency. As the effect of this on the performance of the driver cannot be predicted, some reserve output power was built in and a 45 W driver was designed. The driver is a single-stage class-B amplifier using a BLW86 transistor.

Table 3 shows some properties of the BLW86 from 87.5 to 108 MHz, valid for class-B operation and an output power of 45 W.

Table 3 Some characteristics of the BLW86 at several frequencies in the FM broadcast band

Freq. (MHz)	GAIN (dB)	INPUT IMPEDANCE (Ω)	LOAD IMPEDANCE (Ω)
87.5	13.61	0.76 – j0.00	7.65 + j3.28
89.8	13.40	0.76 + j0.04	7.56 + j3.32
92.2	13.18	0.76 + j0.08	7.48 + j3.36
94.7	12.96	0.76 + j0.12	7.39 + j3.40
97.2	12.75	0.75 + j0.16	7.32 + j3.47
99.8	12.53	0.75 + j0.20	7.23 + j3.51
102.5	12.31	0.75 + j0.24	7.13 + j3.54
105.2	12.10	0.75 + j0.28	7.05 + j3.60
108	11.89	0.75 + j0.32	6.95 + j3.63

The input impedance has to be matched to the 50 Ω source impedance to obtain a good input VSWR and the 50 Ω load impedance has to be transformed into the optimum load impedance, which is given in Table 2. This has been done using Chebychev low-pass LC filter techniques (see Chapter "Reference").

The driver amplifier was designed on double-clad epoxy glass fibre board ($\varepsilon_r = 4.5$), $^1/_{16}$-inch thick. Figure 16 shows the board and layout of the amplifier. Rivets and straps were again used and the emitter connected to the underside of the board.

4.2 Alignment

The alignment procedure was as described in Section 3.2. The optimal load impedance given in Table 2 suggested a dummy load of 10 Ω resistance in parallel with a 91 pF capacitance. Alignment with this dummy load resulted in a collector efficiency of about 60%. Later, it was found that lowering the dummy capacitance to 56 pF raised the efficiency to about 70%. Figure 17 shows the alignment circuit and Fig.18 the VSWR at the output terminal measured with the 10 Ω // 56 pF dummy load.

The input circuit has been aligned with the transistor in the circuit and the supply voltage connected. Again, alignment was started with the transistor operating in class-A ($I_C = 1$ A and $V_{CE} = 25$ V). The small-signal input VSWR has been minimized.

Then, the transistor was set to class-B operation, and the amplifier realigned at an output power of 45 W. Figure 19 shows the final circuit and Table 7 shows the part list. The collector DC biasing coil, L_8, plays an active role in the impedance transformation.

4.3 Performance

Figs 20 and 21 show the gain and input VSWR as functions of frequency. The gain is 12.5 ±0.5 dB and the VSWR remains below 1.3:1 throughout the band.

Figure 21 shows that the collector efficiency is better than 69%. The measurements were taken at 45 W output power.

Figures 23 and 24 show collector efficiency and amplifier gain versus output power at 108 MHz. Note, the amplifier was only aligned at 45 W output power.

5 COMBINATION OF DRIVER AND FINAL AMPLIFIER

Figs 25 and 26 show the gain and input VSWR of the combination of driver and final amplifier at 300 W output power. This gives an indication of the effect of the fluctuating input VSWR of the final amplifier on the performance of the driver amplifier. The efficiency of the combination is more than 63%, as Fig.27 shows.

No additional alignment was made. The required input drive power for 300 W output is less than 1.7 W.

6 STABILITY AND EFFICIENCY IMPROVEMENT

It is recommended to add an inductance L_{CC} between the collectors of the two BLV25 transistors, see Fig.28 (c.f. Fig.10) to improve stability at low output powers. An additional advantage of this modification is that it raises collector efficiency while hardly affecting the input VSWR (which remains below 1.75). Figures 29 to 31 show the results measured on a water-cooled amplifier for three conditions: without L_{CC}, with $L_{CC} = 41$ nH, and with $L_{CC} = 29$ nH.

7 CONCLUSION

A 300 W push-pull amplifier using two BLV25 transistors driven by a single-stage amplifier using a BLW86 have been designed. Table 4 shows the main performance parameters of the individual amplifiers and of their combination.

Table 4 Performance overview (basic amplifier without the modification for higher efficiency)

FM BAND 87.5 – 108 MHz	BLW86 DRIVER P_{OUT} = 45 W		2 × BLV25 FINAL AMPLIFIER P_{OUT} = 300 W		COMBINATION AMPLIFIER BLW86 AND 2 × BLV25 P_{OUT} = 300 W	
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Gain (dB)	12	13	10.4	11	22.6	25
Input VSWR	1.2	1.3	1.45	1.70	1.1	1.85
Efficiency (%)	69	72	70	71	63	66

8 REFERENCE

G.L. Matthaei, Tables of Chebychev impedance transforming networks of low-pass filter form. Proc. of the IEEE, Aug. 1964, pp. 939-963.

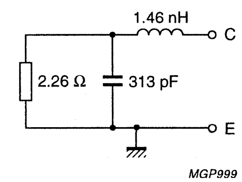


Fig.1 Equivalent circuit of BLV25 output.

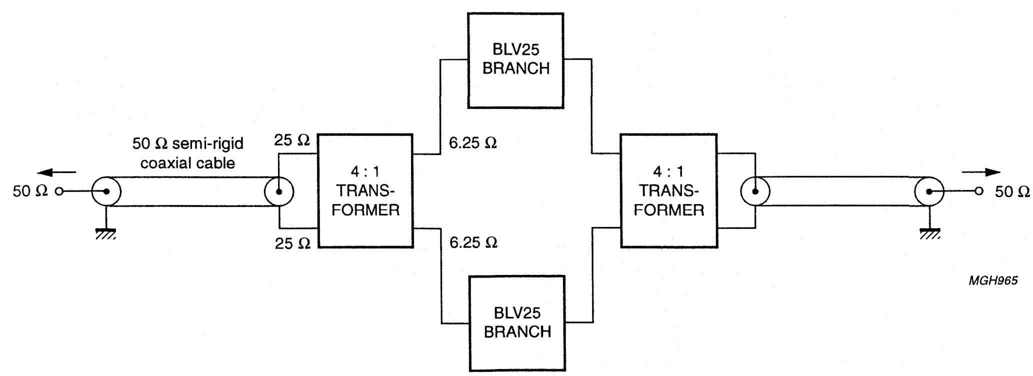
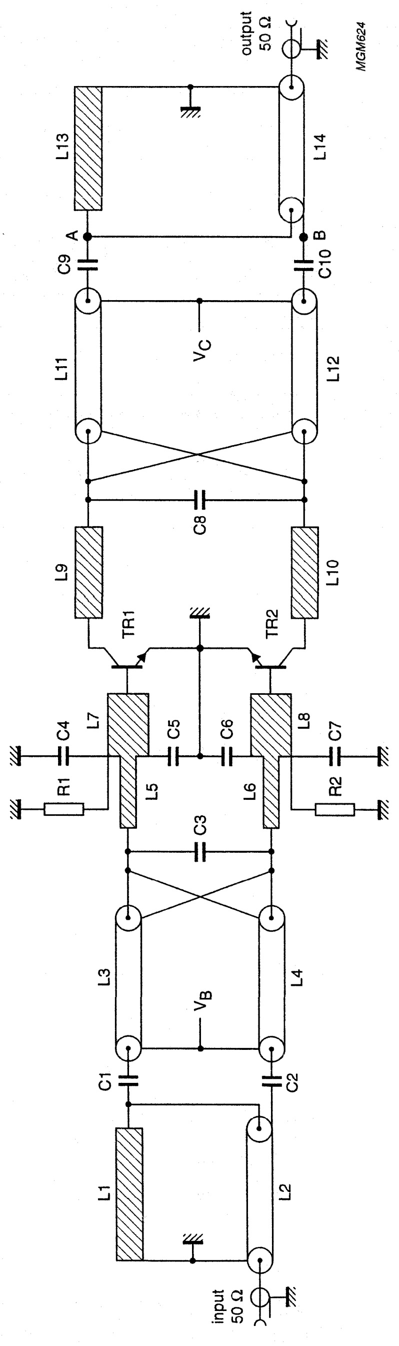


Fig.2 Main amplifier schematic.



For parts list, see Table 5.

Fig.3 300 W push-pull amplifier for the FM broadcast band (Theoretical design).

Table 5 Parts list of the main amplifier (Theoretical design)

$R_1 = R_2 = 22\ \Omega$, carbon
$C_1 = C_2 = 200$ pF chip (ATC 100B)
$C_3 = 330$ pF chip (ATC 100B)
$C_4 = C_5 = C_6 = C_7 = 620$ pF chip (ATC 100B)
$C_8 = 240$ pF, 500 V chip (ATC 100B or ATC 175)
$C_9 = C_{10} = 100$ pF, 500 V chip (ATC 100B)
$L_1 = 50\ \Omega$ stripline, w = 2.8 mm, l = 144 mm
$L_2 = 50\ \Omega$ semi-rigid coaxial cable, d = 2.2 mm, l = 144 mm soldered on 50 Ω stripline, w = 2.8 mm
$L_3 = L_4 = 25\ \Omega$ semi-rigid coaxial cable, d = 2.2 mm, l = 96 mm; soldered on 50 Ω stripline, w = 2.8 mm
$L_5 = L_6 = 50\ \Omega$ stripline, w = 2.8 mm, l = 18.1 mm
$L_7 = L_8 = 30\ \Omega$ stripline, w = 6 mm, l = 4.8 mm
$L_9 = L_{10} = 30\ \Omega$ stripline, w = 6 mm, l = 14.1 mm
$L_{11} = L_{12} = 25\ \Omega$ semi-rigid coaxial cable, d = 3.5 mm, l = 60.3 mm soldered on 50 Ω stripline, w = 2.8 mm
$L_{13} = 50\ \Omega$ stripline, w = 2.8 mm, l = 139.6 mm
$L_{14} = 50\ \Omega$ semi-rigid coaxial cable, d = 3.5 mm, l = 139.6 mm soldered on 50 Ω stripline, w = 2.8 mm
$T_1 = T_2 =$ BLV25
Print board material: $^1\!/_{16}$-inch epoxy fibre-glass, $\varepsilon_r = 4.5$

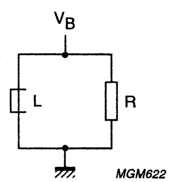


Fig.4 V_b bias, components: R = 12 Ω, carbon; L = Fxc 3B RF choke, part no. 4312 020 36640.

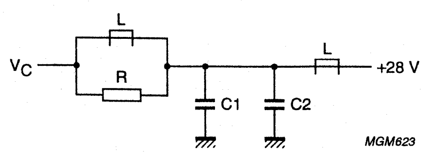


Fig.5 V_c bias. Components: R = 12 Ω, carbon; $C_1 = 2.7$ nF, chip (NP0 type); $C_2 = 100$ nF, chip (X7R type); L = FXC3B bead, part no. 4312 020 31500 wound with 3 to 6 wires in parallel.

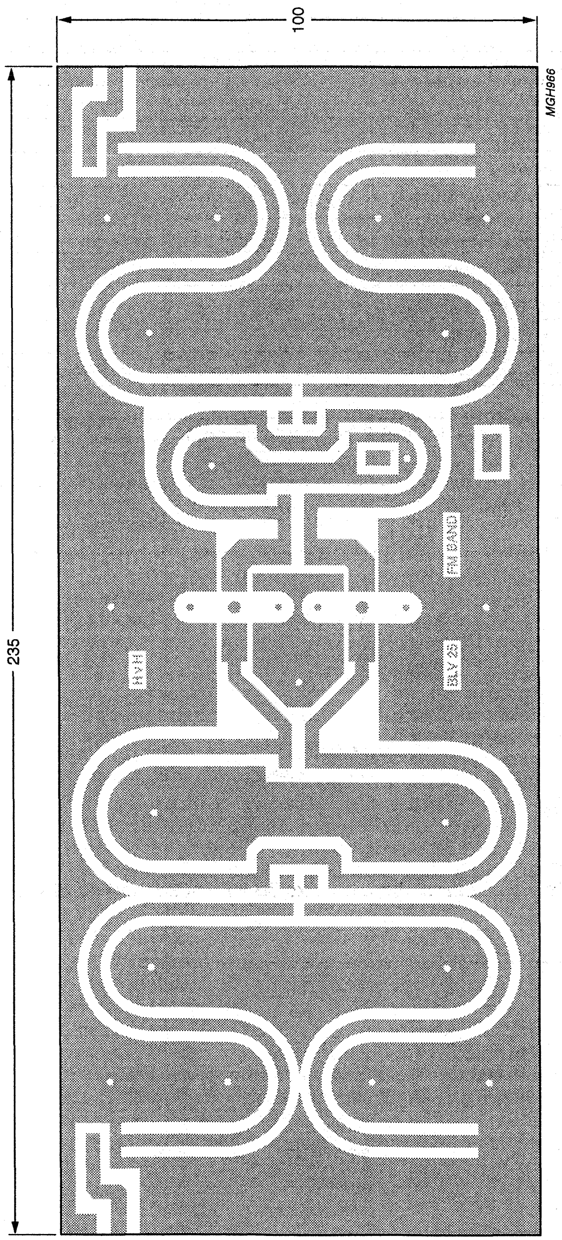


Fig.6 Printed-circuit board.

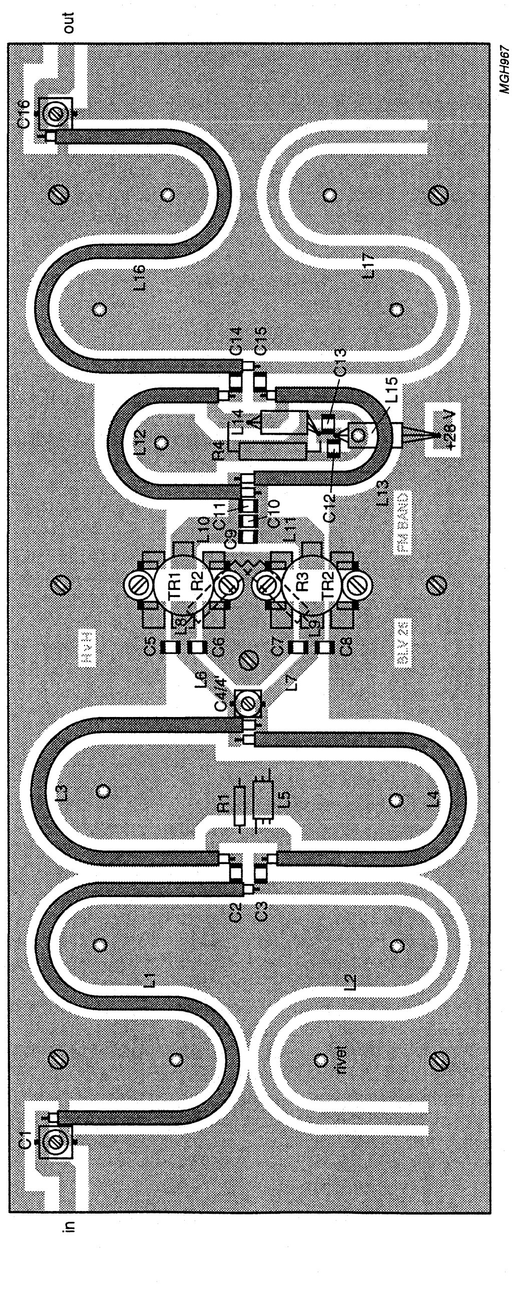


Fig.7 Amplifier lay out.

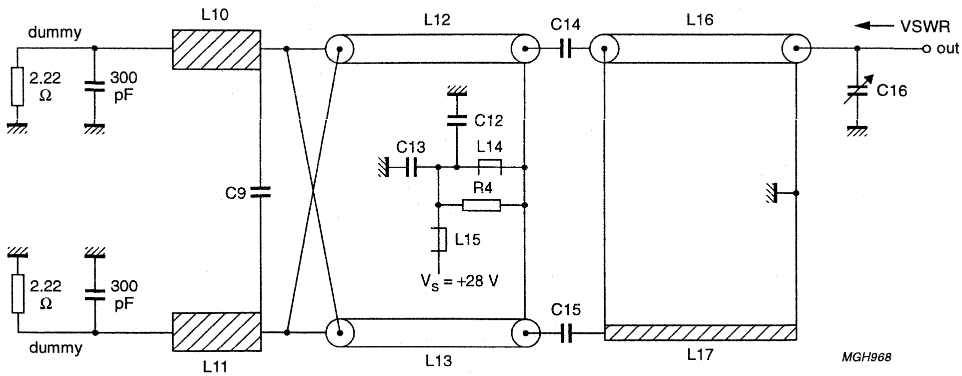


Fig.8 Output alignment circuit.

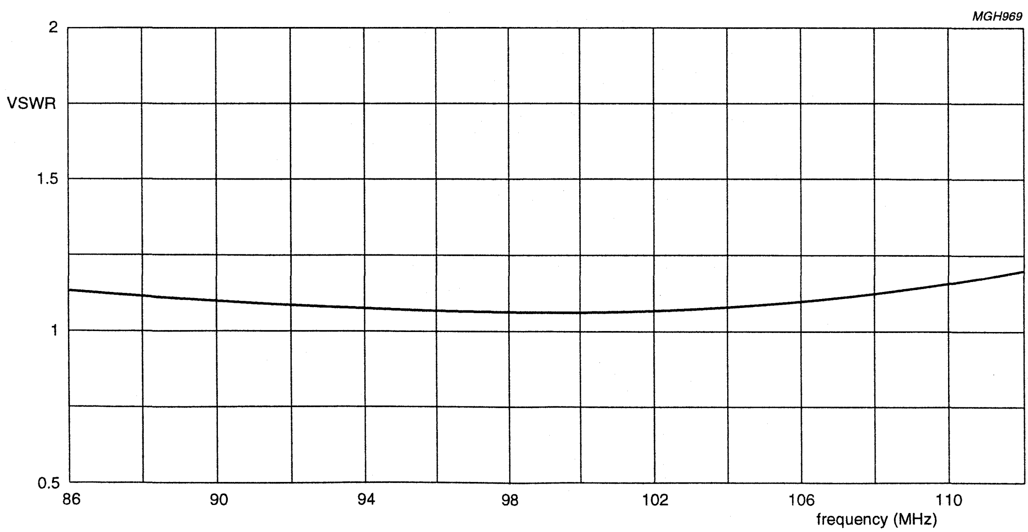
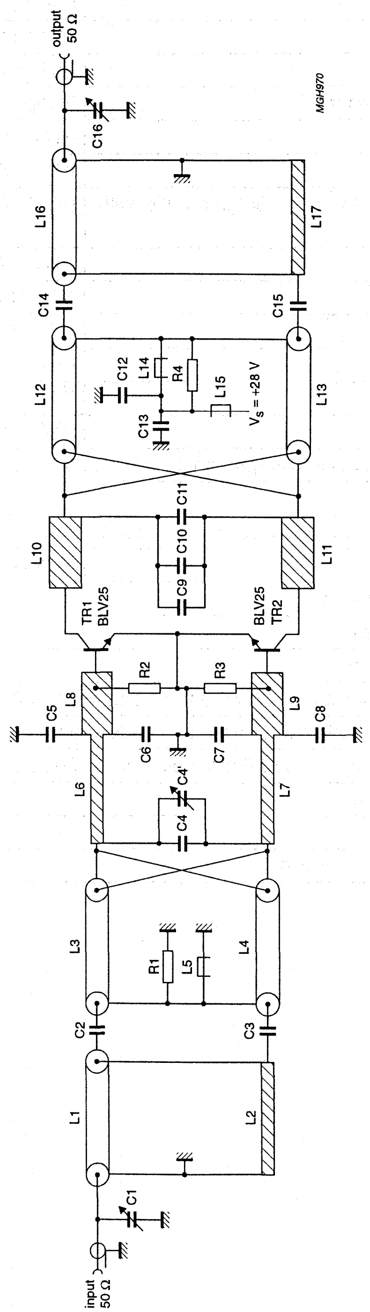


Fig.9 Return loss in circuit of Fig.8.



For parts list see Table 6.

Fig.10 Practical amplifier circuit diagram.

Table 6 Parts list of the main amplifier (Practical design)

R_1 = 12.1 Ω metal film	Philips MR 25, (2322 151 71219)
R_2 = R_3 = 4.99 Ω metal film	Philips MR 52, (2322 153 54998)
R_4 = 12.1 Ω metal film	Philips MR 52, (2322 153 51219)
C_1 = C'_4 = C_{16} = 2 – 18 pF film dielectric trimmer	Philips, (2222 809 05003)
C_2 = C_3 = 200 pF chip	ATC 100B-201-K-Px-300
C_4 = 300 pF chip	ATC 100B-301-K-Px-200
C_5 = C_6 = C_7 = C_8 = 680 pF chip (ATC 100B-681-K-Px-50) in parallel with 150 pF chip	(ATC 100B-151-J-Px-300)
C_9 = 43 pF chip	ATC 100B-430-J-Px-500
C_{10} = 68 pF chip	ATC 100B-680-J-Px-500
C_{11} = 82 pF chip	ATC 100B-820-J-Px-500
C_{12} = 2.7 nF chip	Philips NPO size 1210, (2222 852 13272)
C_{13} = 100k chip	Philips X7R size 1812, (2222 852 48104)
C_{14} = C_{15} = 100 pF chip	ATC 100B-101-J-Px-500
L_1 = 50 Ω semi-rigid coaxial cable, d = 2.2 mm, l = 144 mm, soldered on 50 Ω stripline, w = 2.8 mm	
L_2 = 50 Ω stripline, w = 2.8 mm, l = 144 mm	
L_3 = L_4 = 25 Ω semi-rigid coaxial cable, d = 3.5 mm, l = 96 mm, soldered on 50 Ω stripline, w = 2.8 mm	
L_5 = FXC 3B RF choke	Philips 4312 020 36642
L_6 = L_7 = 50 Ω stripline, w = 2.8 mm, l = 18.1 mm	
L_8 = L_9 = 30 Ω stripline, w = 6 mm, l = 4.8 mm	
L_{10} = L_{11} = 30 Ω stripline, w = 6 mm, l = 14.1 mm	
L_{12} = L_{13} = 25 Ω semi-rigid coaxial cable, d = 3.5 mm, l = 60.3 mm soldered on 50 Ω stripline, w = 2.8 mm	
L_{14} = L_{15} = FXC 3B beads, Philips 4312 020 31500 wound with 6 leads in parallel	
L_{16} = 50 Ω semi-rigid coaxial cable, d = 3.5 mm, l = 139.6 mm soldered on 50 Ω stripline, w = 2.8 mm	
L_{17} = 50 Ω stripline, w = 2.8 mm, l = 139.6 mm	
T_1 = T_2 = BLV25	
Print board material: $^1/_{16}$-inch epoxy fibre-glass, ε_r = 4.5	

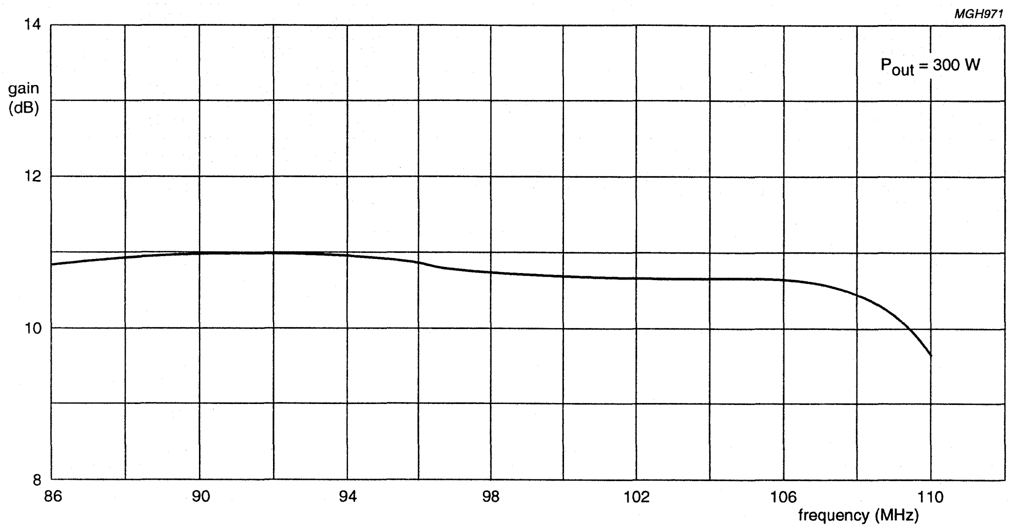


Fig.11 Gain versus frequency (main amplifier).

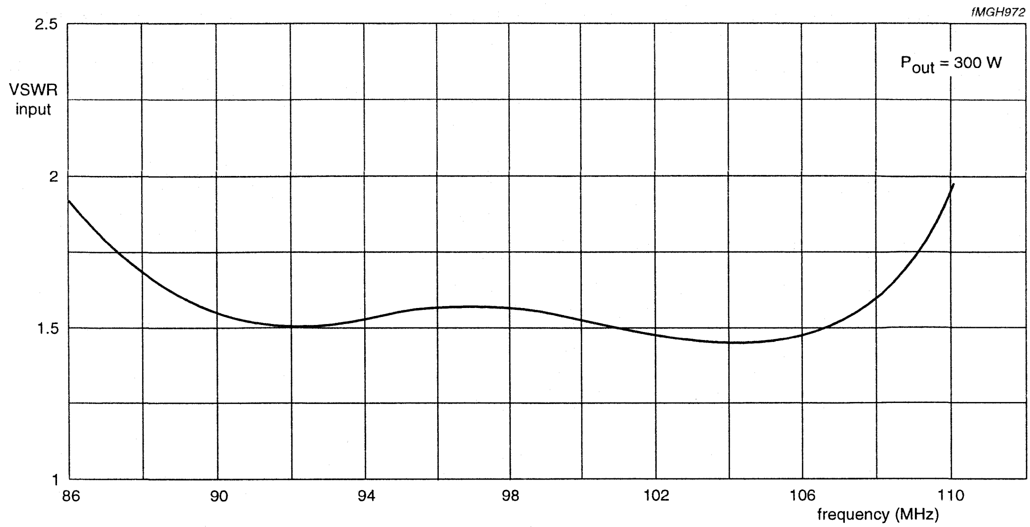


Fig.12 Input VSWR versus frequency (main amplifier).

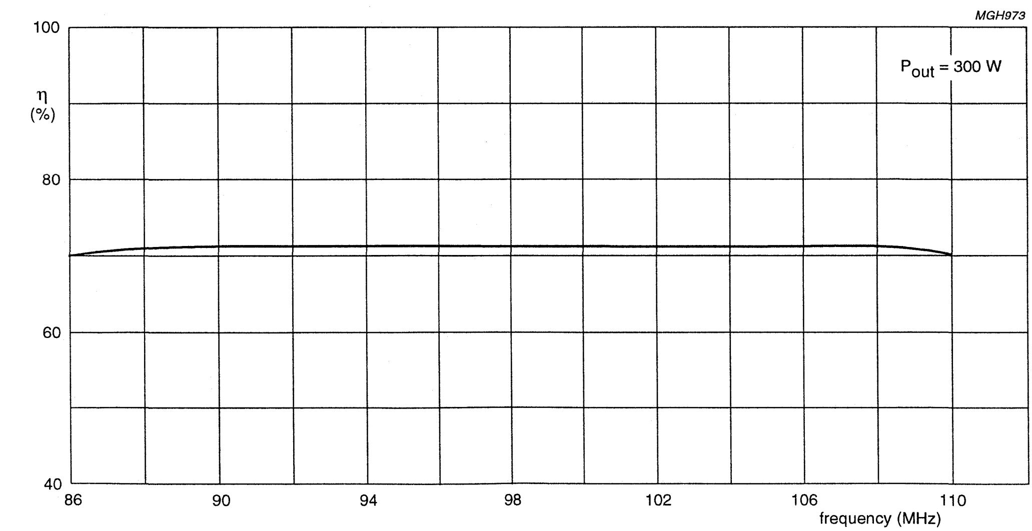


Fig.13 Collector efficiency versus frequency (main amplifier).

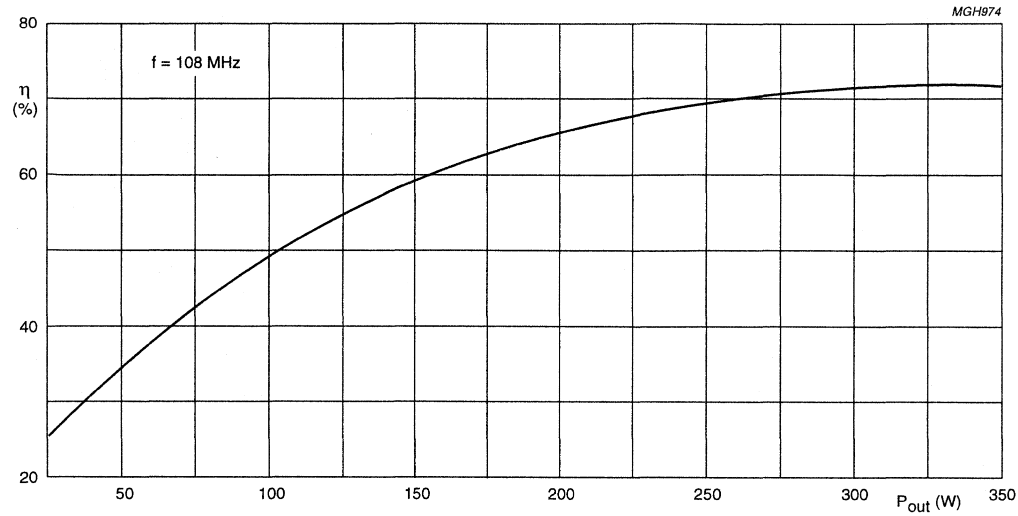


Fig.14 Efficiency, η, versus output power (main amplifier).

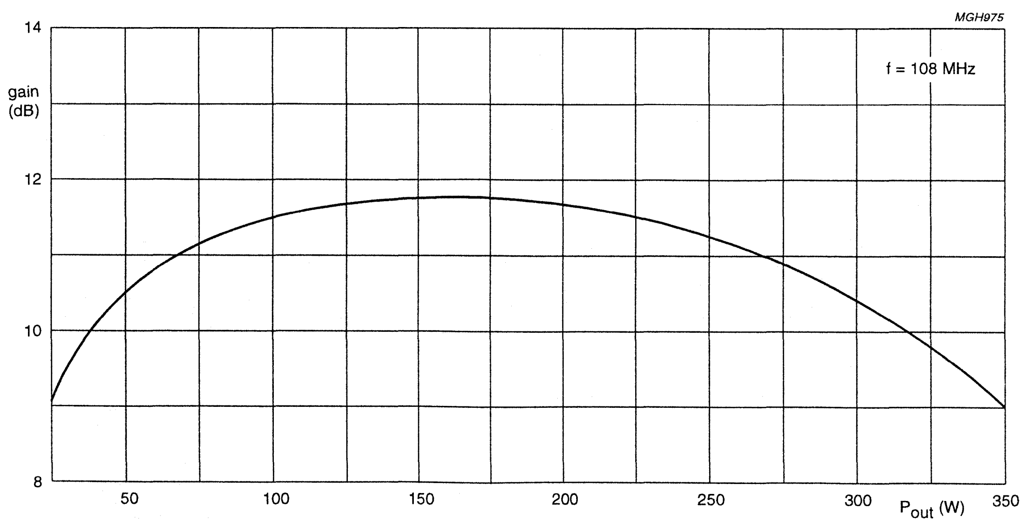


Fig.15 Gain versus output power (main amplifier).

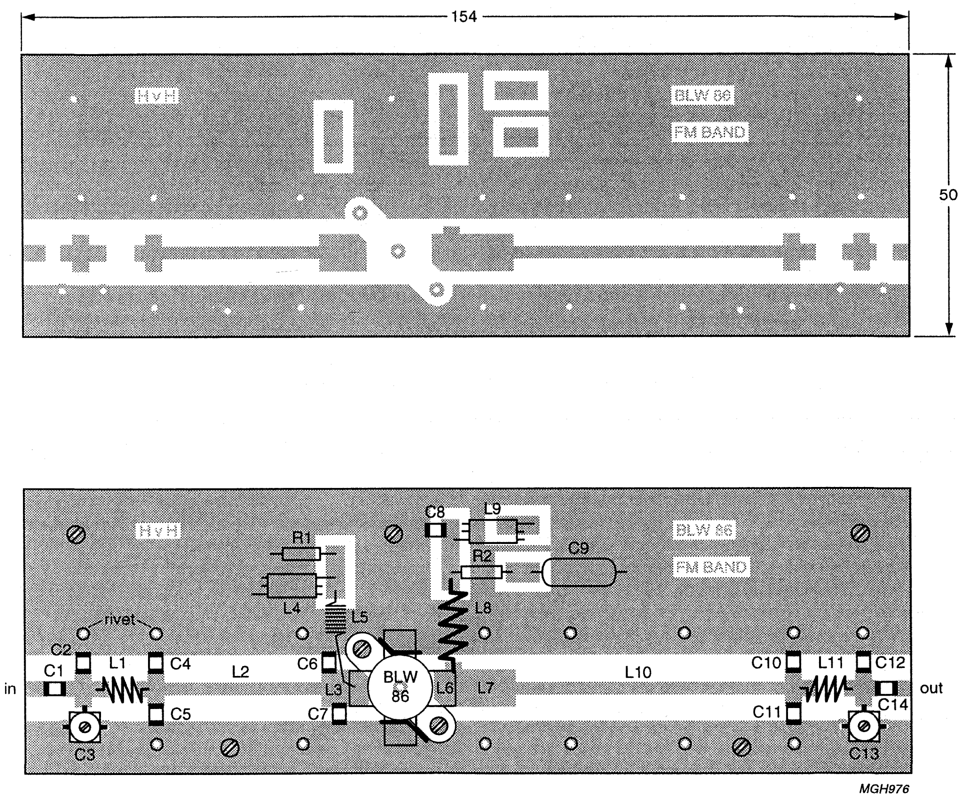


Fig.16 Printed circuit board and lay out of the driver.

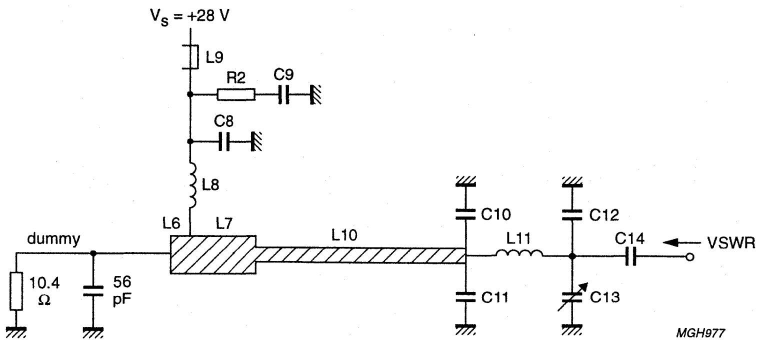


Fig.17 Output alignment circuit (driver).

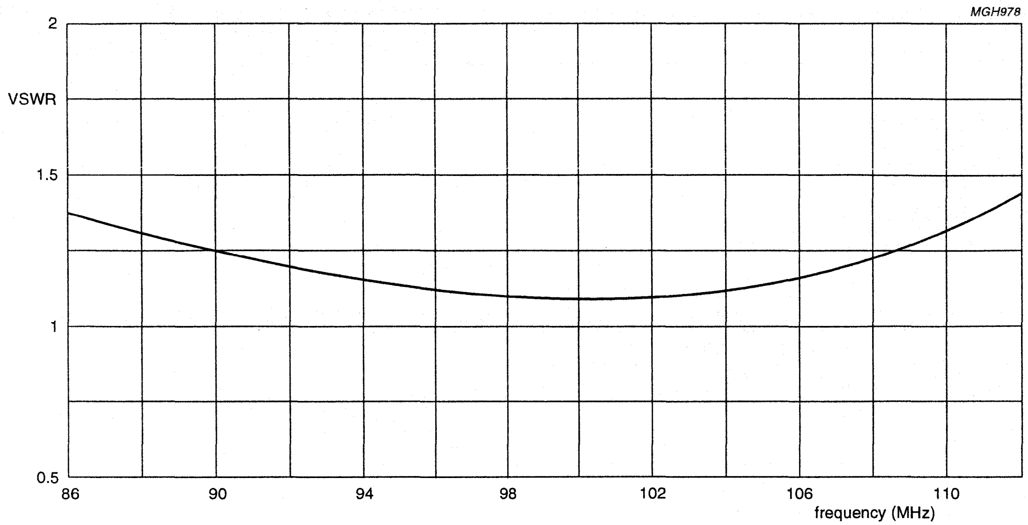


Fig.18 Output VSWR in circuit of Fig.17.

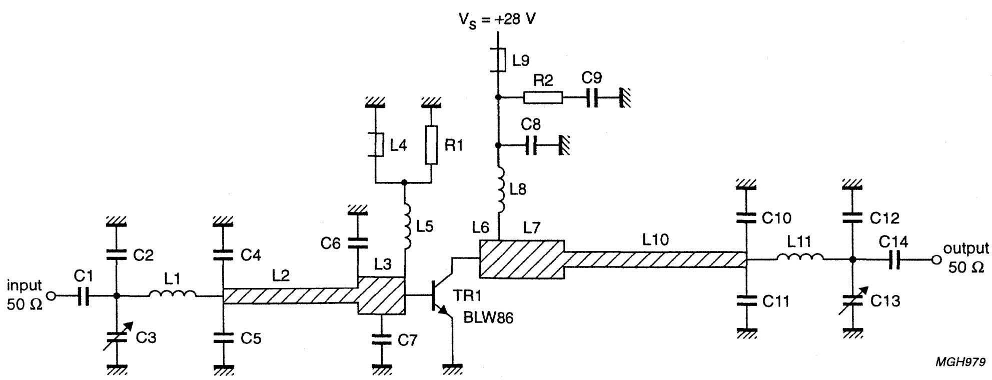


Fig.19 Driver amplifier circuit.

Table 7 Driver amplifier

R_1 = 12.1 Ω metal film	Philips MR 25 (2322 151 71219)
R_2 = 10 Ω metal film	Philips MR 25, (2322 151 71009)
$C_1 = C_8 = C_{14}$ = 2.7 nF chip	Philips NPO size 1210, (2222 852 13272)
C_2 = 33 pF chip	ATC 100B-330-J-Px-500
$C_3 = C_{13}$ = 2 – 18 pF film dielectric trimmer	Philips, (2222 809 09003)
$C_4 = C_5$ = 120 pF chip	ATC 100B-121-J-Px-300
$C_6 = C_7$ = 510 pF chip	ATC 100B-511-M-Px-100
C_9 = 100 nF metallized film capacitor	Philips, (2222 352 45104)
$C_{10} = C_{11}$ = 30 pF chip	ATC 100B-300-J-Px-500
C_{12} = 18 pF chip	ATC 100B-180-J-Px-500
L_1 = 48 nH 4 turns enamelled Cu wire ϕ = 0.8 mm, i.d. 3 mm, closely wound, length 3.5 mm, leads 2 × 5 mm	
L_2 = 60.2 Ω stripline, w = 2 mm, l = 27.2 mm	
L_3 = 30.1 Ω stripline, w = 6 mm, l = 7.9 mm	
$L_4 = L_9$ = FXC 3B RF choke	Philips 4312 020 36640
L_5 = 200 nH 14 turns enamelled Cu wire ϕ = 0.5 mm, i.d. 3 mm, closely wound, length 9 mm	
L_6 = 30.1 Ω stripline, w = 6 mm, l = 3 mm	
L_7 = 30.1 Ω stripline, w = 6 mm, l = 11.8 mm	
L_8 = 27.9 nH 4 turns enamelled Cu wire ϕ = 1 mm, i.d. 4 mm, length 14.3 mm, leads 2 × 5 mm	
L_{10} = 60.2 Ω stripline, w = 2 mm, l = 47 mm	
L_{11} = 55 nH 4 turns enamelled Cu wire ϕ = 1 mm, i.d. 4 mm, length 5.5 mm, leads 2 × 5 mm	
T_1 = BLW86	
Print board material: $^1/_{16}$-inch epoxy fibre-glass, ε_r = 4.5	

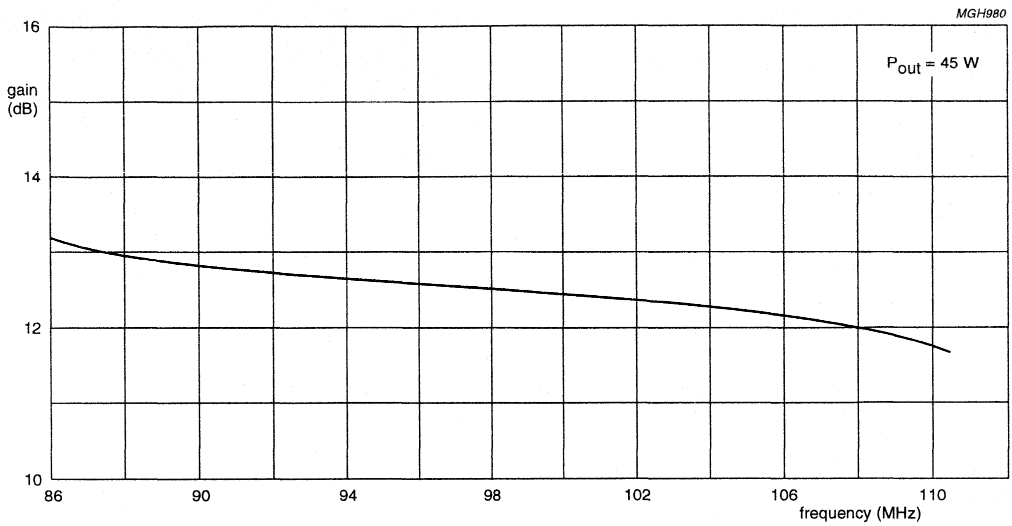


Fig.20 Gain versus frequency (driver).

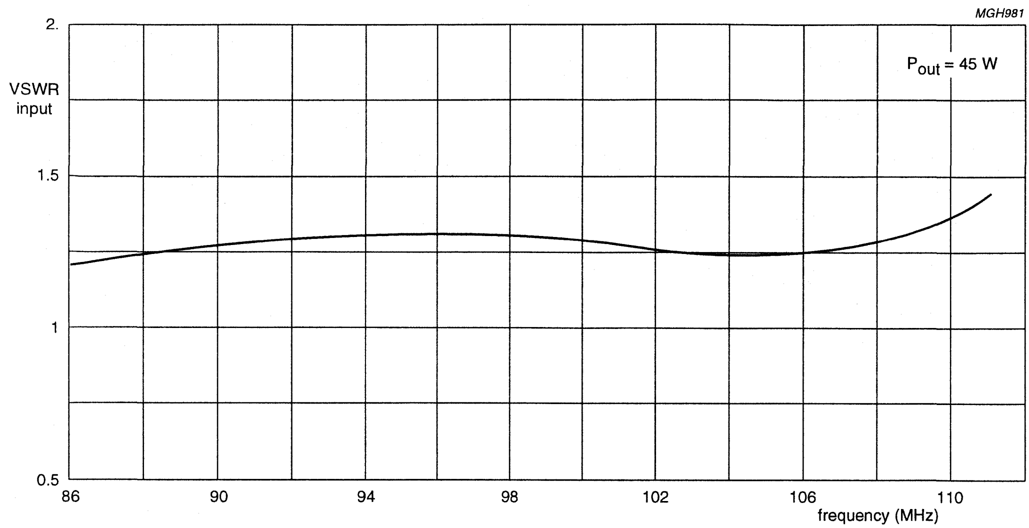


Fig.21 Input VSWR versus frequency (driver).

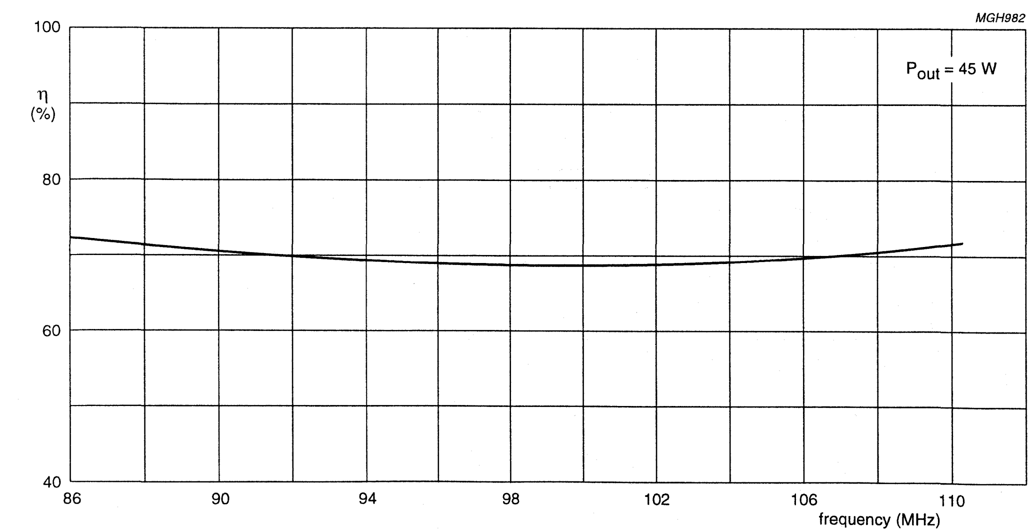


Fig.22 Collector efficiency versus frequency (driver).

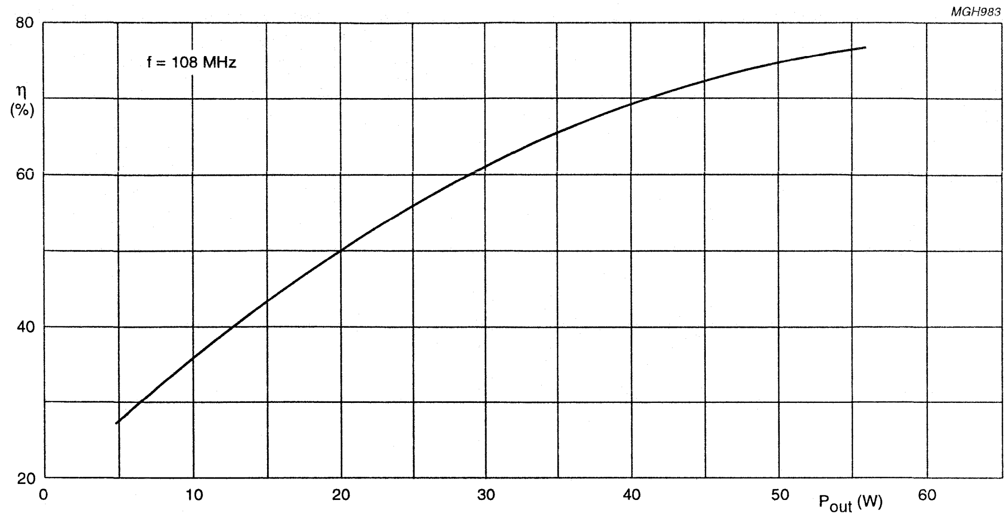


Fig.23 Collector efficiency, η, versus output power (driver).

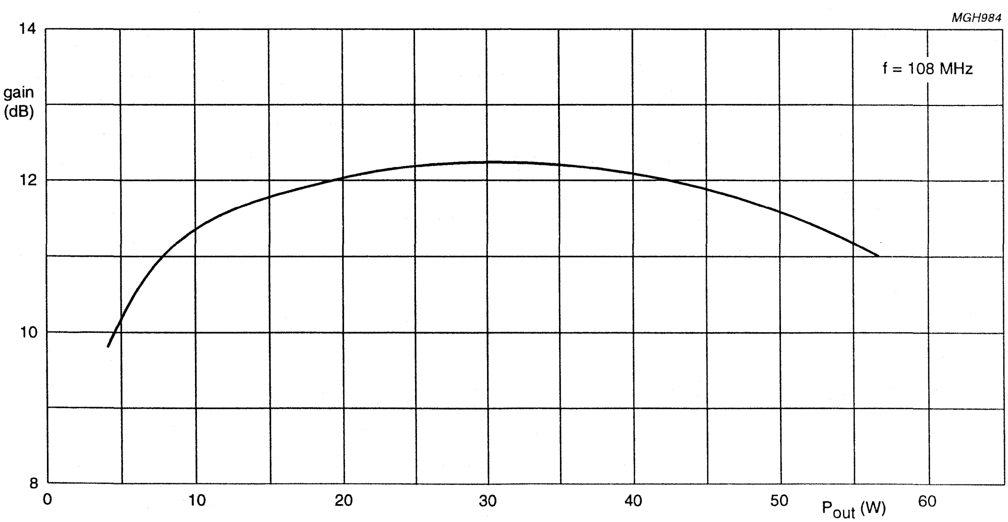


Fig.24 Gain versus output power (driver).

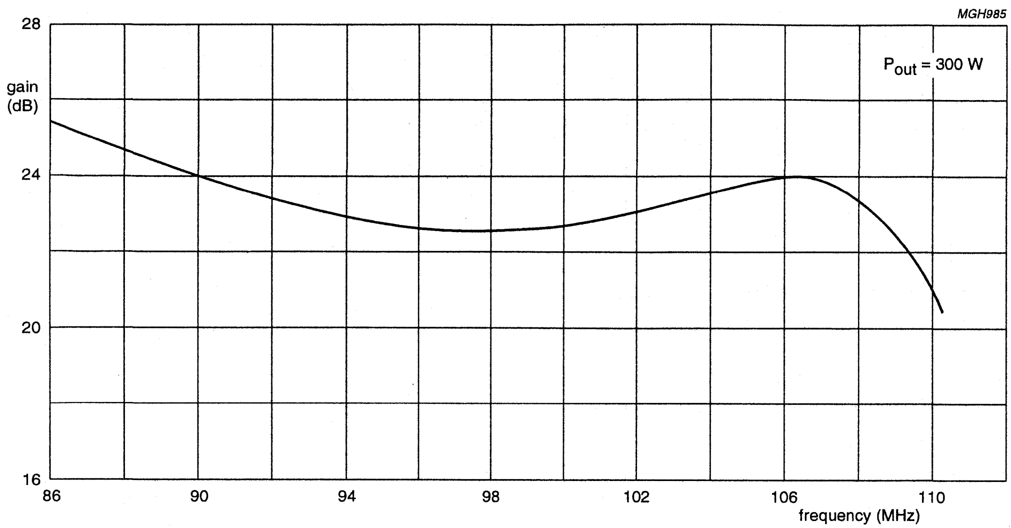


Fig.25 Gain versus frequency (combination amplifier).

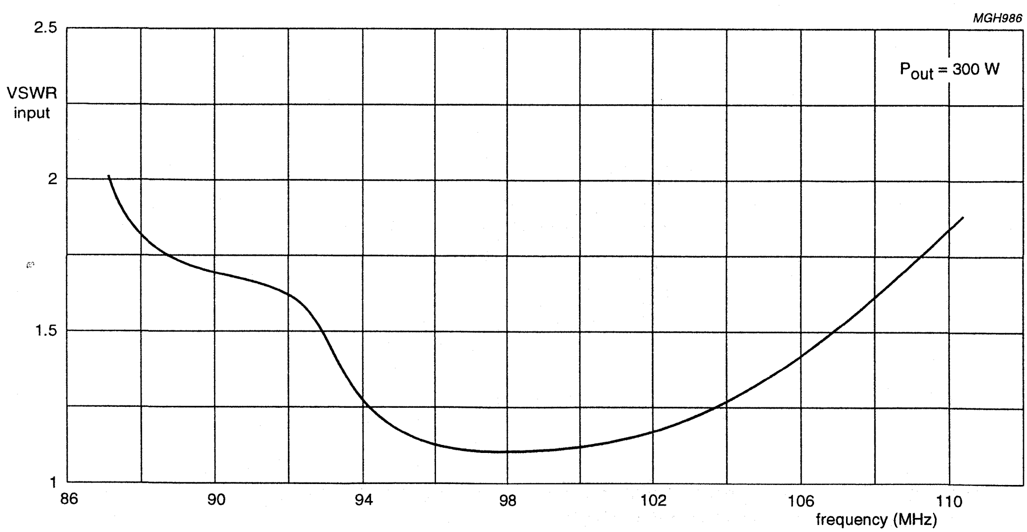


Fig.26 Input VSWR versus frequency (combination amplifier).

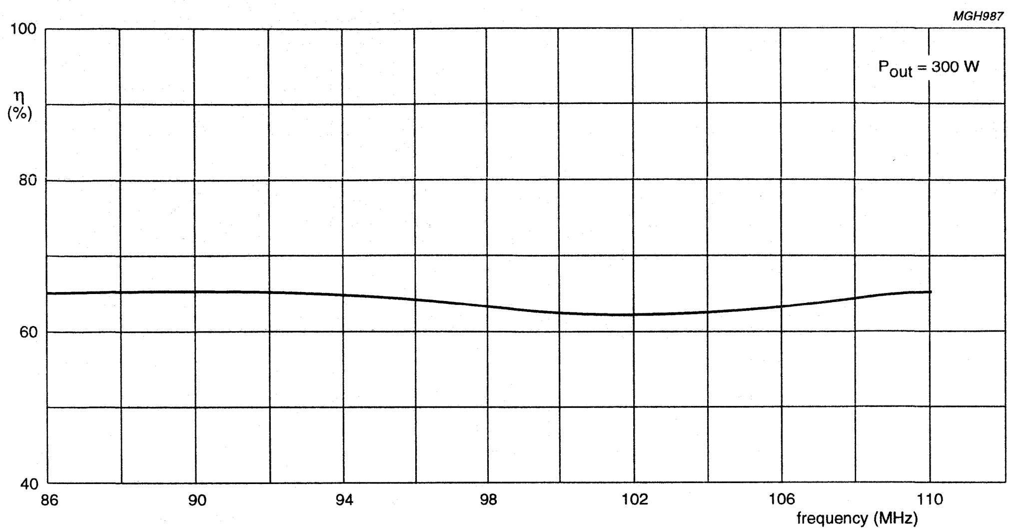


Fig.27 Efficiency versus frequency (combination amplifier).

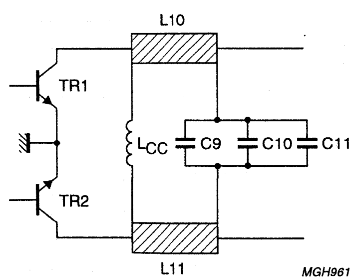
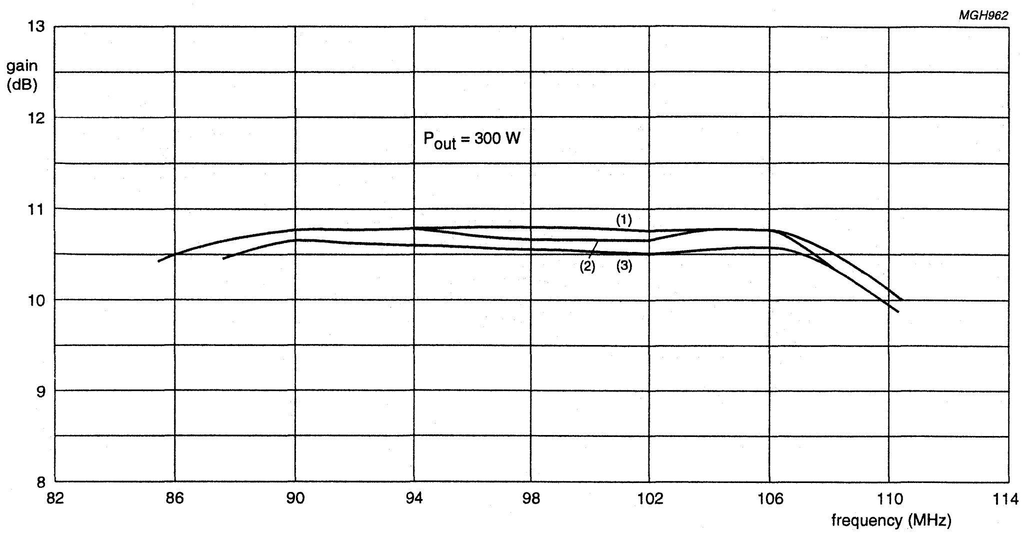


Fig.28 Adding inductance L_{CC} improves stability at low output powers and raises efficiency. Compare this with the relevant part of the circuit shown in Fig.10.



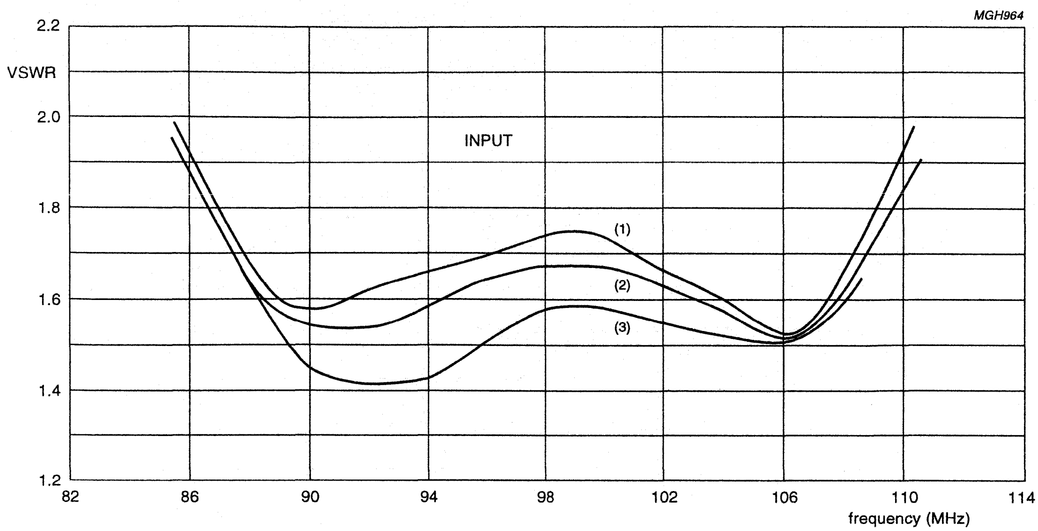
Legend:

(1) no L_{CC}.

(2) L_{CC} = 41 nH; 2 turns enamelled Cu wire ϕ = 1.7 mm, i.d. D = 8 mm, length 6 mm, leads 2 × 10 mm.

(3) L_{CC} = 29 nH 1 turn enamelled Cu wire ϕ = 1.7 mm, i.d. D = 10 mm, leads 2 × 12 mm.

Fig.29 Gain versus frequency.



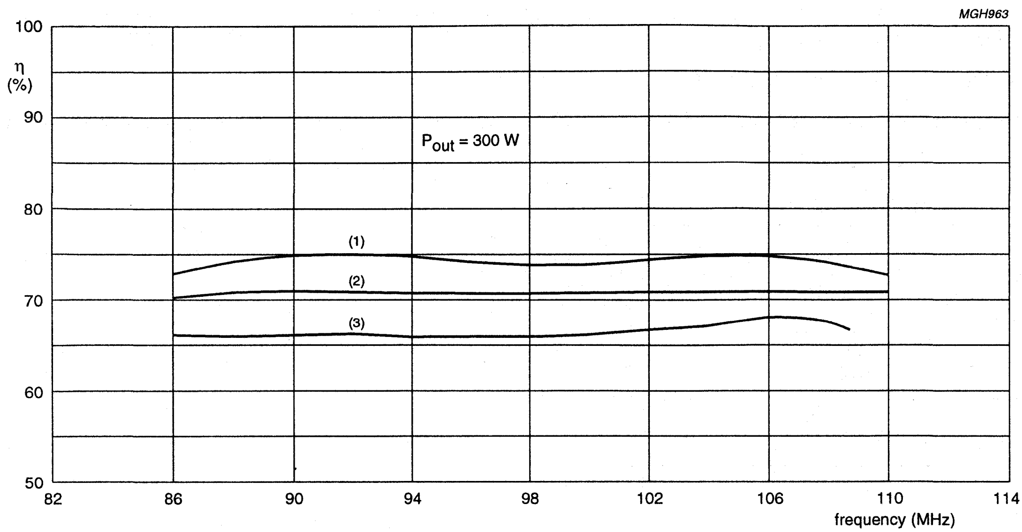
Legend:

(1) no L_{CC}.

(2) L_{CC} = 41 nH; 2 turns enamelled Cu wire ϕ = 1.7 mm, i.d. D = 8 mm, length 6 mm, leads 2 × 10 mm.

(3) L_{CC} = 29 nH 1 turn enamelled Cu wire ϕ = 1.7 mm, i.d. D = 10 mm, leads 2 × 12 mm.

Fig.30 Input VSWR versus frequency.



Legend: as Fig.29.

Fig.31 Efficiency versus frequency.

A wideband power amplifier (25 – 110 MHz) with the MOS transistor BLF245

Application Note NCO8602

1 SUMMARY

For military communication purposes a wideband class-AB power amplifier has been designed around the BLF 245 with the frequency range 25 to 110 MHz.

The DC-setting is V_D = 28 V and I_{DQ} = 200 mA.

In the input and output matching networks asymmetrical 1 : 4 transformers on 4C6 ferrite core material have been applied.

Table 1 The main properties are:

		UNIT
gain at P_O	17.7 ± 0.5	dB
bandwidth	25 – 110	MHz
V_D	28	V
I_{DQ}	200	mA
efficiency	55 – 67	%
input VSWR	≤1.6	

2 INTRODUCTION

The BLF245 is an RF power MOS transistor for the VHF frequency range in a SOT123 encapsulation.

For application in military communication equipment a wideband power amplifier has been developed with a frequency range from 25 to 110 MHz. The transistor operates in class-AB at V_{DS} = 28 V and a quiescent current I_{DQ} = 200 mA. The useful output power is in the range of 25 – 30 W.

3 DESIGN OF THE AMPLIFIER

3.1 General remarks

The amplifier has been developed with 1 : 4 impedance transformers in the input as well as in the output circuit. These transformers of the transmission line type with a ferrite core transform the 50 Ω system impedance at the input and output to about 12.5 Ω. An LC compensation circuit has been applied to transform this 12.5 Ω to the optimum load impedance of the transistor. At the input a circuit matches the 12.5 Ω to the gate impedance of the transistor and also takes care of a flat gain over the whole bandwidth.

3.2 Output circuit

For an optimum alignment of the output circuit the transistor has been replaced by a dummy. This dummy consists of a resistor of 12 Ω parallel with a capacitor of 82 pF. The real part of the dummy has been determined by the available drain voltage and the required output power.

$$R_L = \frac{V_D^2}{2P_O} \rightarrow R_L = \frac{28^2}{2.30} = 13.1\ \Omega$$

This is near to the value of 12.5 Ω mentioned in Section 3.1. The capacitor is about 15% higher than the output capacitance of the transistor. The RF choke at the drain side must have a sufficient high reactance at the lower end of the frequency range. Choosing this reactance appr. a factor 5 higher than the transistor loadresistance we get an inductance of 455 nH for L_4.

The output capacitance of the transistor can be compensated according to the Appendix. The result is: L_6 = 18.6 nH and C_{11} = 82 pF. To transform the achieved 12.5 Ω to the 50 Ω system impedance an asymmetrical 1 : 4 transformer has been used. Information about this kind of transformation can be found in Refs 1 and 2. For the transformer a toroid of 4C6 material has been used. Dimensions: 23 × 14 × 7 mm. On this toroid 5 turns of two 0.7 mm twisted enamelled Cu-wires are uniformly distributed and connected as shown in Fig.1.

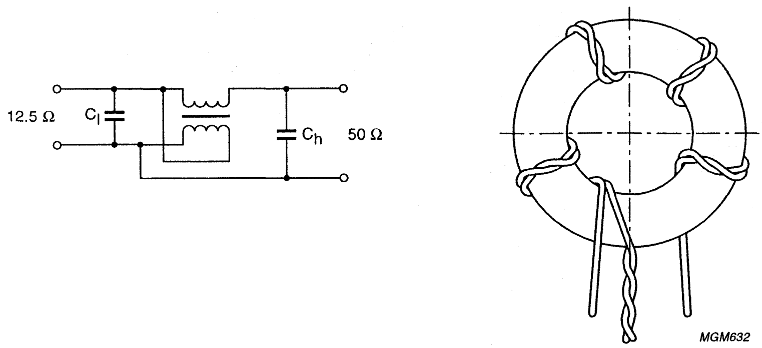


Fig.1 Output transformer.

With the aid of a network analyser the transformer has been corrected for higher frequencies. With C_l = 68 pF and C_h = 12 pF the return losses in the range 20 – 140 MHz are better than –30 dB (VSWR < 1.07). Optimization of the complete output circuit has been carried out by measuring the return losses at the output with the network analyser under swept condition (see Fig.2).

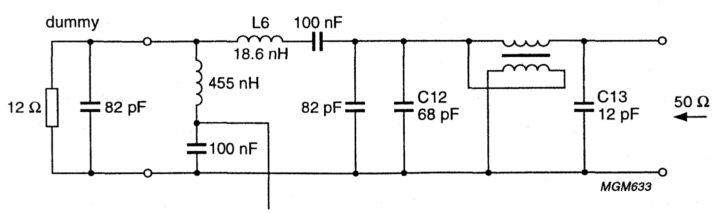


Fig.2 Output circuit before optimization.

Figure 4 shows the return losses of the output circuit before and after practical optimization. By decreasing L_6 to 10 nH and C_{12} to 43 pF the return losses improved about 10 dB in the frequency range 20 to 140 MHz to –20 dB (VSWR = 1.22).

3.3 Input circuit

As mentioned in Section 3.1 a special circuit matches the input impedance of the transistor to 12.5 Ω and also takes care of a sufficient flat gain over the whole bandwidth. To determine the gate-source impedance and the gain of the transistor in combination with the output circuit described in Section 3.2, narrow band input circuits have been used at several frequencies. By tuning such an auxiliary input circuit the gain of the transistor in combination with the output circuit can be measured directly. In case the input circuit has been tuned the output impedance of this circuit is the conjugate complex of the input impedance of the transistor.

Figs 5 to 7 give the input impedance and the gain of the transistor in combination with the output circuit. The matching network chosen at the input of the transistor is depicted in Fig.3.

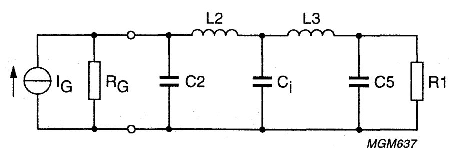


Fig.3 Input matching circuit.

C_i represents the input capacitance of the BLF245 which is appr. 220 pF (see Fig.6). Across this capacitor a constant voltage versus frequency from 25 up to 110 MHz has to be developed. Provided Ci is an ideal capacitance the optimum dimensioning of this network is as follows:

$R_G = R_1 = 1.6/(\omega_c \times C_i) = 10.5\ \Omega$

$C_2 = C_5 = 0.386\ C_i = 85$ pF

$L_2 = L_3 = 0.997\ R_1/\omega_c = 15.1$ nH.

in which ω_c is the maximum angular frequency. The calculated voltage variation across C_i is ±0.36 dB and the maximum VSWR seen by the generator is 1.36. Deviating from this calculation, for the ease of transformation, R_G and R_1 have been chosen 12.5 Ω. Further the resistive component of C_i is substantial especially at higher frequencies.

Therefore the values of the components have been changed in a computer optimization program for a maximally flat gain and a low input VSWR. This optimization results in a gain of 17.5 dB with a variation of ±0.17 dB and a maximum VSWR = 1.177. These results have been achieved by changing the components of Fig.3:

$C_2 = 97$ pF, $C_5 = 102$ pF, $L_2 = 17.6$ nH, $L_3 = 29$ nH and $R_1 = 12\ \Omega$.

The remaining part of the transformation from 12.5 Ω to the 50 Ω system impedance has been accomplished with a transformer similar to the output transformer. However the input transformer has been wound on a core consisting of 2 small toroids of 4C6 material (6 × 4 × 2 mm).

On this core 6 turns of two 0.25 mm twisted enamelled Cu-wires are uniformly distributed similar to the output transformer described in Section 3.2. (see Fig.1). With correction capacitors at the high ohmic and the low ohmic side of respectively 8.2 and 47 pF the return losses in the range 20 – 140 MHz are better than –27 dB (VSWR ≤ 1.1).

For the practical optimization of the complete inputcircuit the transistor has been adjusted at V_D = 28 V and a quiescent current I_{DQ} = 200 mA. The gain and input return losses have been measured in the frequency range of 20 up to 110 MHz.

The best results have been achieved by changing the correction capacitor C_3 from 47 to 62 pF and by executing R_1 as a parallel connection of 5 resistors of 61.9 Ω.

Figure 8 gives the complete circuit diagram of the BLF245 wideband amplifier and Table 3 gives the corresponding parts list.

4 MEASURED PERFORMANCE

4.1 Constant input power

Figs 9 to 11 give the gain, efficiency and output power versus the frequency at a constant input power (P_i = 0.5 W).

In the frequency range of 25 to 110 MHz the gain is 17.2 to 17.9 dB, the efficiency 55 to 70% and the output power 26.5 to 30.5 W.

4.2 Constant output power

Figs 12 and 13 give the gain and efficiency versus the frequency at a constant power (P_O = 27.5 W) and heatsink temperatures of 25 and 70 °C.

Figs 14 and 15 give the input return losses and the 2e and 3e harmonics of the output signal also versus the frequency. The return losses have been measured at a heatsink temperature of 25 and 70 °C. The harmonics have been measured at 25 °C. By increasing the heatsink temperature from 25 to 70 °C the gain decreases about 1.2 dB. The heatsink temperature has no influence on efficiency and return losses. At 25 °C the gain of the amplifier varies from 17.2 to 18.2 dB, the efficiency from 55 to 67% and the return losses at the input are at least –14 dB (VSWR ≤ 1.6). Also the 2e and 3e harmonics are at least 14 dB down.

4.3 Constant frequency

Figs 16 to 18 give the output power versus input power and the gain and efficiency versus power at 4 frequencies.

4.4 Stability

Applying an R&S PTU low pass filter at the output of the amplifier stability measurements have been carried out. Choosing a low pass frequency as close as possible above the measuring frequency the amplifier was stable through the whole frequency range of 25 to 110 MHz.

4.5 Mismatch

The amplifier has been tested for load mismatch at all phase angles. Up to VSWR = 10 : 1 the amplifier is stable. At VSWR = 20 : 1 the amplifier is only stable below 70 MHz. However also at higher frequencies degradation of the RF performance did not occur.

5 CONCLUSIONS

Based on the results presented in this report it may be concluded that it is quite possible to design a wideband amplifier from 25 to 110 MHz with a very good performance using the MOS transistor BLF 245.

Table 2 The main properties are:

		UNIT
Bandwidth	25 – 110	MHz
V_D	28	V
I_{DQ}	200	mA
Gain (P_O = 27.5 W)	17.7 ± 0.5	dB
Efficiency	55 – 67	%
Input VSWR	≤1.6	

6 REFERENCES

Ref.1.
A.H. Hilbers
Application report ECO6907: Design of HF wideband Power Transformers.

Ref.2.
A.H. Hilbers
Application report ECO7703: Power Transformers for the Frequency Range 30 – 80 MHz

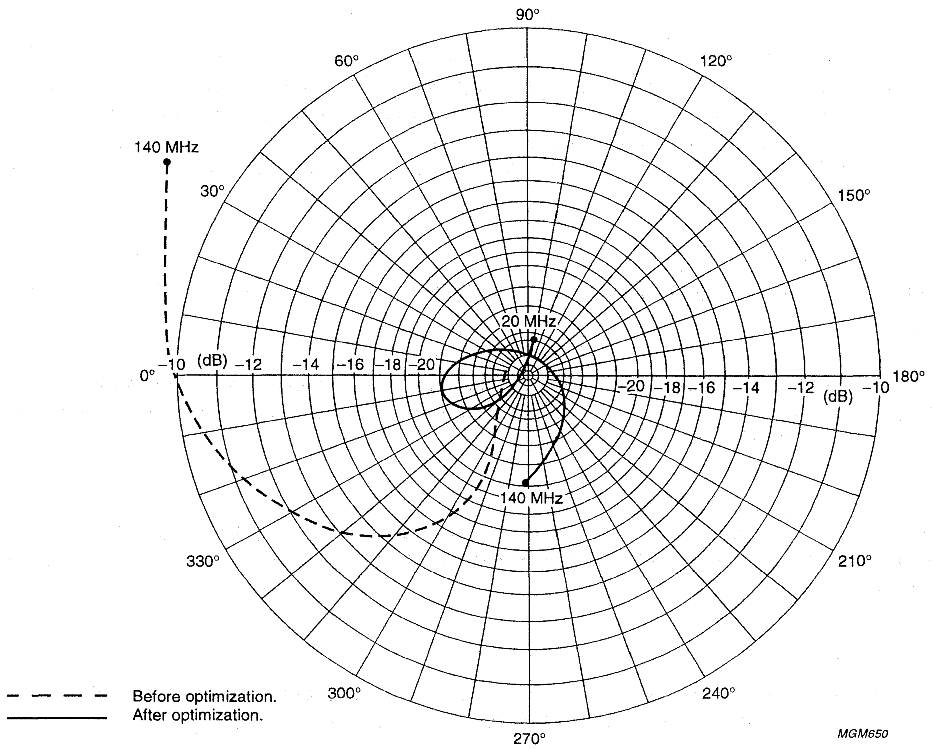


Fig.4 Return losses output circuit.

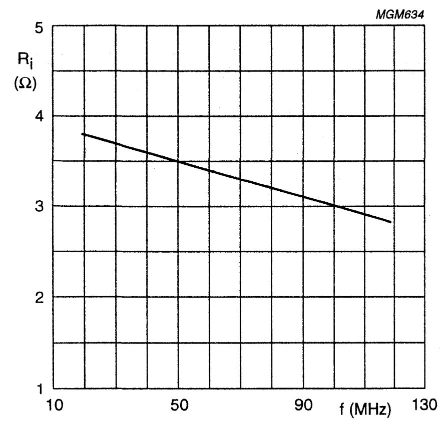


Fig.5 Real part of input impedance of loaded transistor.

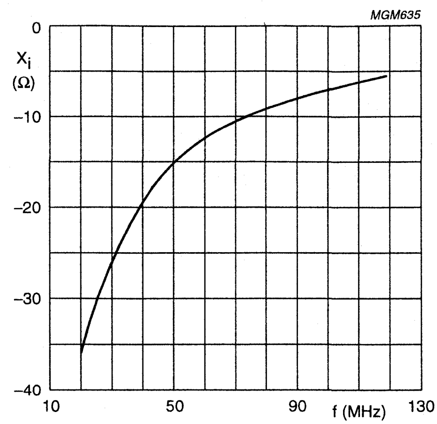


Fig.6 Imaginary part of input impedance of loaded transistor.

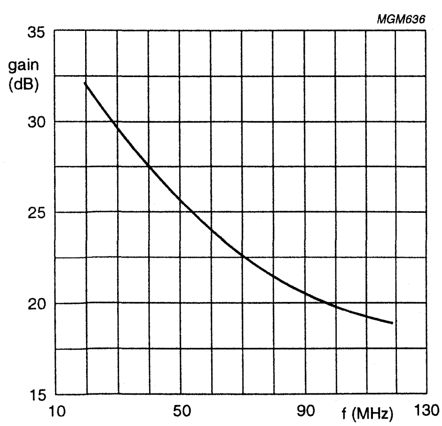


Fig.7 Gain of loaded transistor.

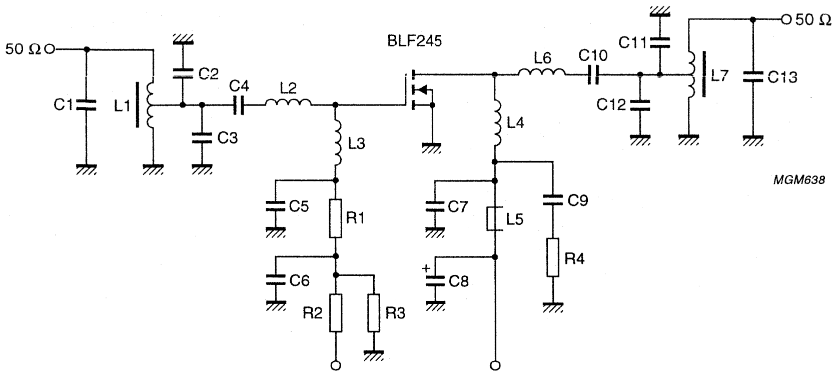


Fig.8 Circuit diagram of the BLF245 wideband amplifier.

Table 3 Parts list of the BLF245 wideband amplifier

WIDEBAND POWER AMPLIFIER WITH BLF245 (f = 25 – 110 MHz)	
C1 = 8.2 pF multilayer ceramic chip capacitor; note 1	
C2 – C5 = 100 pF multilayer ceramic chip capacitor; note 1	
C3 = 62 pF multilayer ceramic chip capacitor; note 1	
C4 = C10 = 10 nF multilayer ceramic chip capacitor	cat. no. 2222 852 47103
C6 = C7 = 100 nF multilayer ceramic chip capacitor	cat. no. 2222 852 47104
C8 = 2.2 uF electrolytic capacitor	
C9 = 3 × 100 nF multilayer ceramic chip capacitor	cat. no. 2222 852 47104
C11 = 82 pF multilayer ceramic chip capacitor; note 1	
C12 = 43 pF multilayer ceramic chip capacitor; note 1	
C13 = 12 pF multilayer ceramic chip capacitor; note 1	
L1 = 2 Ferroxcube toroids, grade 4C6 (6 × 4 × 2 mm) with 6 turns of 2 × 0.25 mm twisted enamelled Cu-wire (see Fig.1)	cat. no. 4322 020 97160
L2 = 17.6 nH, 2 turns enamelled Cu-wire (0.6 mm) int.dia.: 3 mm, length 2.5 mm, leads 2 × 5 mm	
L3 = 28.8 nH, 3 turns enamelled Cu-wire (0,6 mm) int.dia.: 3 mm, length 3.2 mm, leads 2 × 5mm	
L4 = 455 nH, 12 turns enamelled Cu-wire (1 mm) int.dia.: 7 mm, length 16.5 mm, leads 2 × 5 mm	
L5 = Ferroxcube h.f.choke, grade 3B	cat. no. 4312 020 36642
L6 = 10 nH, 1 turn enamelled Cu-wire (1 mm) int.dia.: 3 mm leads 2 × 3 mm	
L7 = Ferroxcube toroid, grade 4C6 (23 × 14 × 7 mm) with 5 turns of 2 × 0.7 mm twisted enamelled Cu-wire (see Fig.1)	cat. no. 4322 020 97190
R1 = 12.4 Ω, parallel connection of 5 metal film resistors 61.9 Ω	cat. no. 2322 151 76199
R2 = 1 KΩ, metal film resistor	cat. no. 2322 151 71002
R3 = 1 MΩ, metal film resistor	cat. no. 2322 151 71005
R4 = 10 Ω, metal film resistor	cat. no. 2322 153 51009
Printed-circuit board: double Cu-clad, 1.6 mm epoxy fibre-glass (ε_r = 4.5)	

Note

1. American Technical Ceramics type 100B or capacitor of same quality.

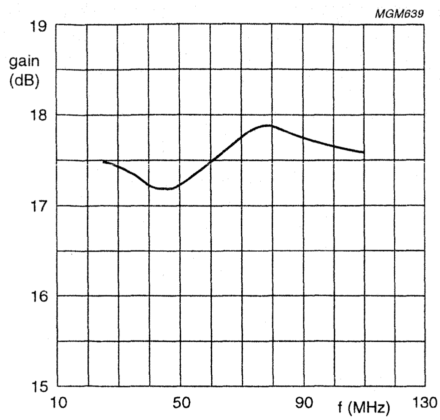


Fig.9 Gain at $P_i = 0.5$ W.

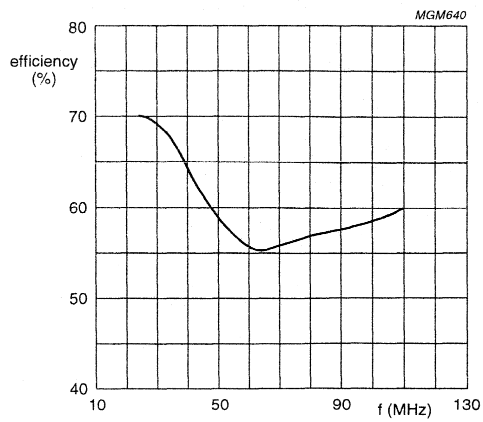


Fig.10 Efficiency at $P_i = 0.5$ W.

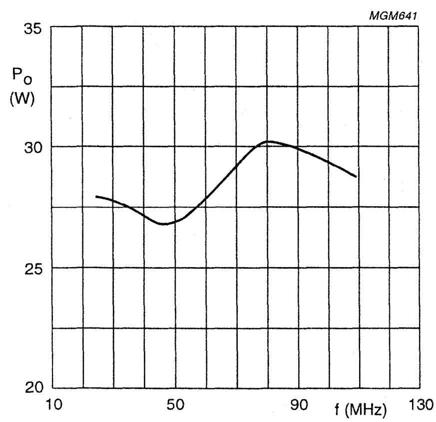


Fig.11 Output power at $P_i = 0.5$ W.

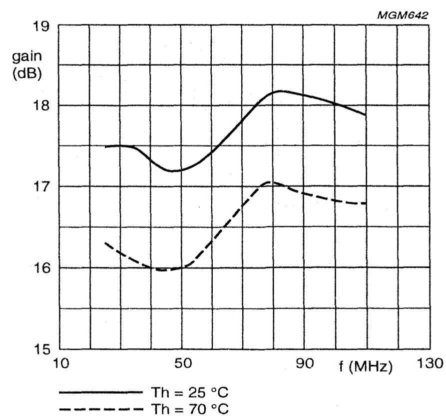


Fig.12 Gain at $P_O = 27.5$ W.

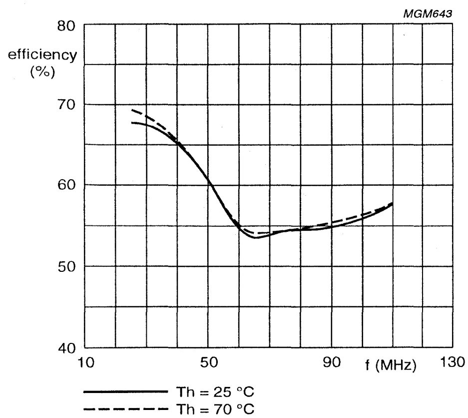


Fig.13 Efficiency at P_O = 27.5 W.

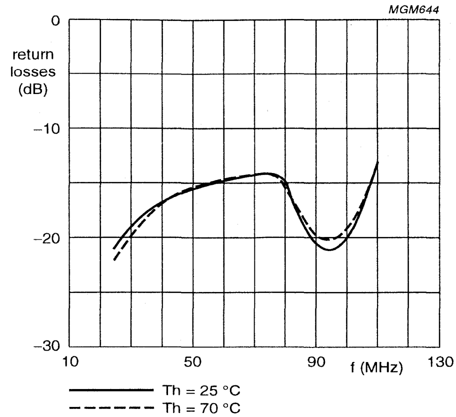


Fig.14 Input return losses at P_O = 27.5 W.

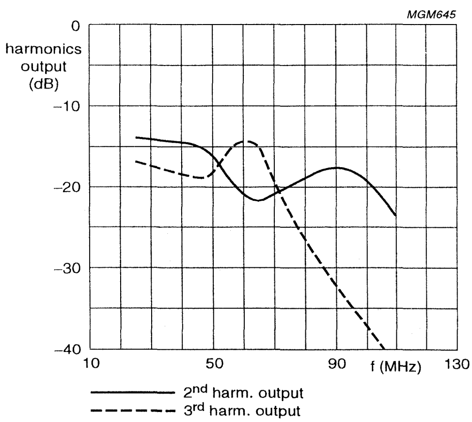


Fig.15 Output harmonics at P_O = 27.5 W.

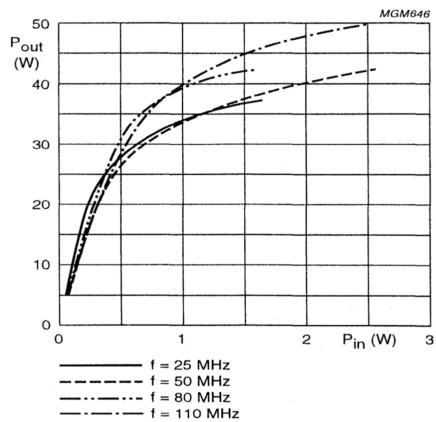


Fig.16 Output power versus input power.

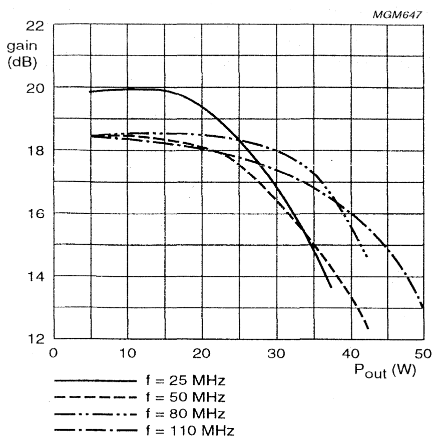


Fig.17 Gain versus output power.

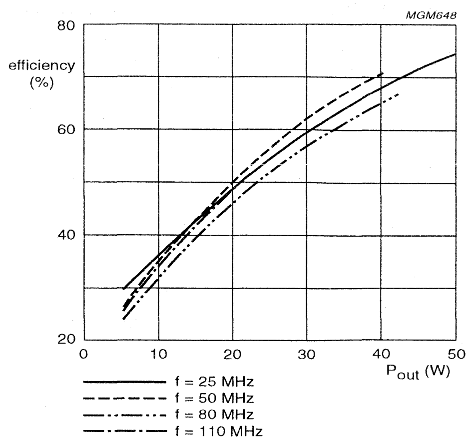


Fig.18 Efficiency versus output power.

7 APPENDIX

The output capacitance of a transistor can be compensated over a certain bandwidth by absorbing it in a low-pass Chebyshew π-section.

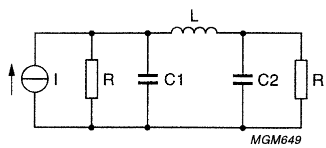


Fig.19

If C1 is the transistor output capacitance the components L and C2 must be added.
$C2 = C1 = C$

The normalized value of C is: $A = \omega_m CR$
In which $\omega_m = 2\,\pi\,f_{max}$

Now we can calculate the normalized value of L with:
$B = 8A/(3A^2 + 4)$
where $B = \omega_m\,L/R$

The maximum VSWR of this network can be calculated with the following procedure.

1. Determine $\gamma = \dfrac{1}{A}$
2. $X = \gamma + \sqrt{\gamma^2 + 1}$
3. $\text{VSWR} = \left\{\dfrac{X^3 + 1}{X^3 - 1}\right\}^2$

In our amplifier:
$R = 12.5\ \Omega$
$C = 82$ pF

This gives:
$A = 0.784$
$B = 1.029$
$L = 18.62$ nH
$\gamma = 1.412$
$X = 3.142$
$\text{VSWR} = 1.138$

A wideband 30 W push-pull amplifier with two MOS transistors BLF244 (V_{DS} = 28 V); range 25 – 110 MHz

Application Note NCO8701

1 INTRODUCTION

A wideband push-pull power amplifier has been developed for the frequency range 25-110 MHz. The design is based on the BLF244, a silicon N-channel enhancement mode vertical D-MOS transistor designed for large-signal amplifier applications in the VHF range. This device can deliver 15 W output power at 175 MHz when operated from a 28 V supply. The transistor has a 4-lead flange envelope with a ceramic cap (SOT123).
The objective was to design and construct a 30 W wideband amplifier with high gain and efficiency and low input VSWR and second order distortion. With respect to gain and efficiency a reasonable flatness was desired. The push-pull design is employed because of its low second order distortion.
The design and practical realization of this amplifier are described in the following chapters.

2 AMPLIFIER DESIGN

2.1 General

The schematic set up of the amplifier is depicted in Fig.1.

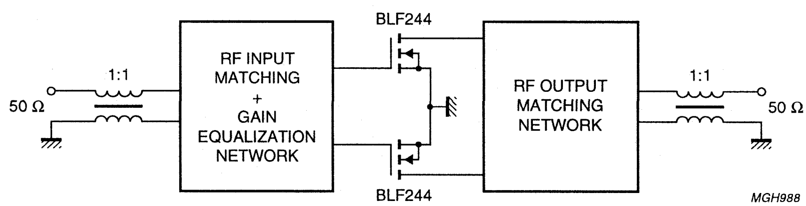


Fig.1

Two 1 : 1 balance to unbalance transformers are applied; one for splitting the single-ended input source into two out of phase sources driving the transistor-inputs, the other for adding the outputs from the transistors.
Transmission line transformers are employed because of there excellent broadband response. These transformers consist of a twisted-wire-pair transmission line wound on a ferrite toroid.
At the input side a special matching network is applied to obtain a low VSWR and compensation for variation in gain with frequency.
The matching network at the output side provides the transistors with the optimum load for an output power of 30 W at V_{DS} = 28 V.

2.2 Powergain, input- and output impedance

The design has been started by determining powergain, input impedance and output impedance of the transistor for the frequency range 25-110 MHz.

First the output impedance was determined.
For HF and VHF the optimum load resistance RL can be calculated with reasonable accuracy with the formula:

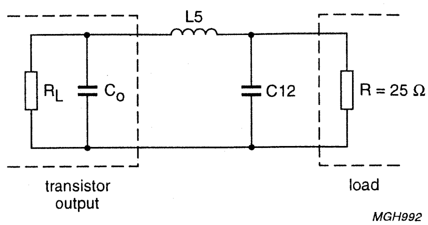


Fig.2

$$R_L = \frac{V^2_{DS}}{2 \cdot P_O} \qquad (1)$$

For V_{DS} = 28 V and P_O = 15 W we get: R_L = 26.1 Ω.
The output impedance is the parallel combination of the output capacitance C_O of the transistor and the optimum load resistance.
Because of the large drain voltage swing the effective output capacitance C_O is approx. 15% higher than the value of C_{oss}. For BLF244 C_{OSS} is typical 38 pF, so C_O is equal to 43.7 pF. So the output impedance of this transistor can be represented by 26.1 Ω//43.7 pF for the whole frequency range.
Second the large-signal input impedance and powergain versus frequency were determined by measurement. For this purpose a single-ended test amplifier was constructed. This amplifier was matched at the output side to a load of 25 Ω by a broadband matching network: Dimensioning of this network was based on a practical dummy transistor of 24 Ω//43 pF. The maximum VSWR measured within the band was 1.16.
At the input side tunable narrowband matching networks were applied at several frequencies. By tuning this amplifier for minimum return loss at P_O = 15 W the powergain was measured directly.

For measurement of the input impedance the DC power, signal source and transistor were disconnected from the amplifier and the signal source circuit connection was terminated with 50 Ω. After that the impedance was measured at the gate connection of the transistor. The input impedance of the transistor is the conjugate of the measured impedance if the circuit doesn't contain resistive components.
This procedure was repeated at several frequencies in the band to get sufficient data for the design.
Figures 14, 15 and 16 present the data in graphical form.

2.3 Output matching section

Because of the symmetrical set-up of this amplifier its matching sections can be divided into two equal parts. Each part belonging to one transistor. In the next discussion one half of the output matching section will be considered.

As mentioned in the previous section the optimum load resistance for P_O = 15 W and V_{DS} = 28 V is 26.1 Ω according to equation (1).
When two of these transistors are used in a push-pull configuration the optimum load resistance adds up to 52.2 Ω. This value is very close to 50 Ω to which these transistors have to be matched. So, if we choose the optimum load resistance to be 50 Ω we can suffice with a 1 : 1 balance to unbalance transformer.
The output capacitance C_O of the transistor can be compensated over a certain bandwidth by absorbing it in a low-pass Chebyshev π-section, see Fig.2.

R_L represents the optimum load resistance for the transistor. The components L5 and C12 can be determined with the following formulae if $R_L = R$ and $C_O = C12 = C$:
The normalized value of C is:

$$A = \omega_m \cdot C \cdot R \qquad (2)$$

in which $\omega_m = 2 \times \pi \times f_{max}$

The normalized value of L5 can be calculated as follows:

$$B = \frac{\omega_m \times L_5}{R} \qquad (3)$$

$$B = \frac{8 \times A}{3 \cdot A^2 + 4} \qquad (4)$$

The maximum VSWR of this network follows from:

$$VSWR_{max} = \left\{\frac{x^3 + 1}{x^3 - 1}\right\}^2 \qquad (5)$$

in which $x = \gamma + (\gamma^2 + 1)^{1/2}$

and $\gamma = 1/A$

For this section R = 25 Ω and C = 43 pF. This results in: A = 0.7430 → B = 1.0509 → L5 = 38 nH and $VSWR_{max}$ = 1.156.

In practice this circuit comprises some additional components, see Fig.3.

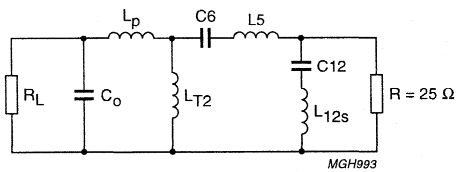


Fig.3

These are:

- L_p – the parasitic drain and source inductance which has been accounted for by this way. Its value is approx. 1.4 nH
- L_{T2} – the drain choke inductance which equals approx. 0.8 μH. Determination of this inductance will be treated in a later chapter.
- L_{12S} – the parasitic series inductance of C12, which is approx. 1 nH
- C_6 – the DC-blocking capacitor which is also employed for low frequency compensation of L_{T2}.

The value of C_6 is calculated with the aid of the information given in ref.(1). The drain load circuit for low frequency is shown in Fig.4.

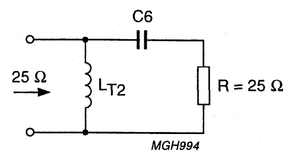


Fig.4

Compensation according to ref.(1) gives at f = 25 MHz:

C_6 = 1.28 nF with $VSWR_{max}$ = 1.04

The circuit in Fig.3 was optimized for the frequency range 25-110 MHz. For this purpose a computer optimization program was used. The criterion used was for overall minimum VSWR with respect to 25 Ω.

The results before and after optimization are shown in Table 1.

Table 1

BEFORE OPTIMIZATION		AFTER OPTIMIZATION	
C_6	1.28 nF	C_6	7.9 nF
L_5	38 nH	L_5	34.6 nH
C_{12}	43 pF	C_{12}	37.9 pF
$VSWR_{max}$	1.169	$VSWR_{max}$	1.098

2.4 Input matching section

The purpose of the input matching section is two-fold. First to match the transistor input impedance to the source impedance of 50 Ω with a sufficiently low VSWR across the frequency band.
Second to compensate the variation in gain with frequency.

The input matching section chosen is depicted in Fig.5 for one transistor.

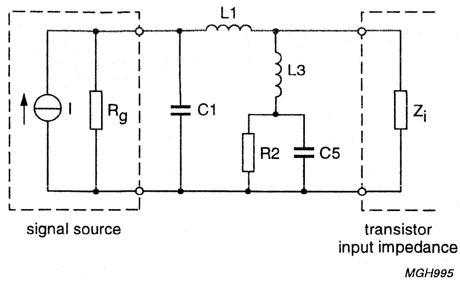


Fig.5

Since the input impedance of the transistor is strongly capacitive, Zi can be approximated by an ideal capacitor. This network can then be treated as a symmetrical double pi-section, see Fig.6.

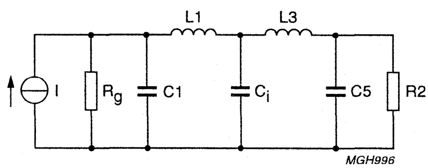


Fig.6

In order to get sufficient gain flatness a constant voltage has to be developed across capacitor Ci. For optimum dimensioning of this network the following formulae are valid:

$$Rg = R2 = \frac{1.6}{\omega_m \cdot ci} \tag{6}$$

$$C1 = C5 = 0.386 \times Ci \tag{7}$$

$$L1 = L3 = 0.997 \times \frac{Rg}{\omega_m} \tag{8}$$

in which ωm is the maximum angular frequency. These formulae have been obtained by a computer optimization program which also indicates that the maximum voltage variation across Ci is ±0.36 dB and the maximum VSWR seen by the generator 1.36. When the input capacitance at the lowest frequency is chosen, which is approx. 117 pF, we find that:

Rg = R2 = 19.8 Ω

C1 = C5 = 45.2 pF

L1 = L3 = 28.6 nH.

In practice Rg is equal to 25 Ω and Zi varies with frequency. This required a re-optimization of this network with the actual values of Zi and Rg. The values calculated above were used as the initial values and parasitics of C1 and C5 were included. The target gain was set to 17.5 dB.
The results of this optimization are shown in Table 2.

Table 2

BEFORE OPTIMIZATION		AFTER OPTIMIZATION	
C1	45.2 pF	C1	60.1 pF
C5	45.2 pF	C5	47.5 pF
L1	28.6 nH	L1	36 nH
L3	28.6 nH	L3	43.8 nH
R2	19.8 Ω	R2	20.8 Ω
Rg	25 Ω	Rg	25 Ω
$VSWR_{max}$	1.812	$VSWR_{max}$	1.376
G_{pmin}	15.8 dB	G_{pmin}	17.1 dB
G_{pmax}	16.9 dB	G_{pmax}	17.9 dB

3 TRANSFORMER DESIGN

3.1 General

As mentioned before transformers employed at the input and output side utilize twisted-wire-pair transmission lines wound on a toroidal core.
The windings are uniformly distributed around the toroid. The required characteristic impedance of the transmission lines is 50 Ω. In practice Zo will differ from this required value and compensation measures will be necessary (2). This can be achieved with:

- Parallel capacitances across input and output terminals of the transformers if Zo > 50 Ω
- Inductances in series with the input and output terminals of the transformer if Zo < 50 Ω.

The result of this compensation is an exact match at the maximum frequency. There will be however, a slight mismatch at low frequency which is many times smaller then that at the maximum frequency without compensation. Because the amount of HF compensation will depend on the circuit layout and the exact transformer construction no calculations will be made on this aspect of the transformers. The amount of compensation will be determined in the circuit by employing adjustable capacitors.

3.2 Design of the output transformer

The characteristic impedance of 50 Ω for the transmission line of the output transformer has been obtained with enamelled copper wire of 0.6 mm diameter. Its diameter with isolation included is 0.66 mm.
The number of twists applied are 2 per centimeter.

A suitable core material for this frequency range is Philips 4C6 grade available in several sizes of toroid. The size of the toroid is determined by the maximum allowable dissipation which is limited to 350 mW/cm^3 to prevent excessive rise in temperature. Designing for a maximum of 1% power loss in the core (300 mW) the minimum effective volume required is:

$$Ve_{min} = \frac{P_{loss}}{350\ mW/cm^3} = \frac{300}{350} = 0.85\ cm^3$$

The smallest toroid that is suitable is a core with dimensions D × d × h = 23 × 14 × 7 mm corresponding with a effective core volume of 1.79 cm^3. As a result the core loss reduces to 170 mW/cm^3.
According to reference (3) this corresponds to a maximum flux density (B) of 0.2 mT at 110 MHz. The required number of turns is determined by the ratio Rp/L in which R_p is the loss resistance that represents the core loss and L the inductance in parallel with the output terminals, see reference (4).
This ratio is equal to:

$$R_p/L = \frac{\omega^2 \times B^2 \times Ve}{2 \times \mu_o \times \mu_r \times P_{loss}} \qquad (9)$$

which amounts to: $$R_p/L = \frac{\left(2 \times \pi \times 110 \times 10^6\right)^2 \times \left(0.2 \times 10^{-3}\right)^2 \times 1.79 \times 10^{-6}}{2 \times 4 \times \pi \times 10^{-7} \times 120 \times 0.3} = 472\Omega/\mu H$$

To keep the core loss below 1% we must keep the parallel loss resistance above 5000 Ω with reference to 50 Ω. This means an inductance of: L = Rp/472 = 10.6 µH

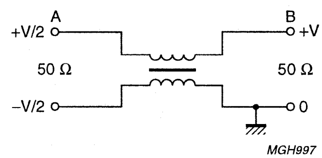


Fig.7

Between point A and B in Fig.7 the voltage is one half of the output voltage. Therefore the inductance between these points must be a quarter of that across the 50 Ω terminals, so:

L_{AB} = L/4 = 10.6/4 = 2.65 µH

The number of turns required can be calculated with the following formula (3):

$$L = A_L \times N^2 \qquad (10)$$

$$A_L = \frac{0.4 \times \pi \times \mu r}{\Sigma l/A} \qquad (11)$$

in which:

A_L is the inductance in (nH)

$\Sigma l/A$ is the core constant in (mm^{-1}) given in (3)

N is the number of turns

µr is the relative permeability (120 for grade 4C6).

For a toroid of 23 mm the core constant is 1.81 mm^{-1}. So, the inductance factor amounts to:

$$A_L = \frac{0.4 \times \pi \times 120}{1.81} = 83.3 \text{ nH}$$

and the required number of turns:

$$N = \sqrt{\frac{2.65 \times 10^3}{83.3}} = 5.6 \text{ turns}$$

In practice the number of turns will be 6, so the inductance in parallel with the output terminals rises to:

$(6/5.6)^2 \times 10.6 = 12\ \mu H$

This corresponds to a reactance of 1885 Ω at 25 MHz which is high enough to be neglected.
The core loss reduces to:

$(5.6/6)^2 \times 1\% = 0.87\%$

The measured value of L_{AB} was approx. 3.5 μH.

3.3 Design of the input transformer

The input transformer is of the same type as the output transformer and is also designed in the same way.

To obtain a characteristic impedance of 50 Ω for the windings enamelled Cu-wire with a bare diameter of 0.50 mm is used. The diameter with isolation included is 0.55 mm. The number of twists applied is 2¾ per centimeter.

Allowing an input power level of 1.5 W the minimum effective volume for 1% power loss in the core is:

$Ve_{min} = 15/350 = 0.043\ cm^3$

The smallest toroid that suits our need is a type with dimensions D × d × h = 9 × 6 × 3 mm. The effective core volume is 0.105 cm^3, so the core loss reduces to 143 mW/cm^3. This corresponds to a maximum flux density B of approx. 0.18 mT at f = 110 MHz according to ref.(3). The ratio Rp/L amounts to:

$$Rp/L = \frac{\left(2 \times \pi \times 110 \times 10^6\right)^2 \times \left(0.18 \times 10^{-3}\right)^2 \times 0.105 \times 10^{-6}}{2 \times 4 \times \pi \times 10^{-7} \times 120 \times 0.015} = 360\Omega/\mu H$$

For 1% loss L amount to:

$L = Rp/360 = 5000/360 = 13.9\ \mu H$

$L_{AB} = 13.9/4 = 3.48\ \mu H$

The required number of turns for a 9 mm toroid with a core constant of 5.17 mm^{-1} is:

$$A_L = \frac{0.4 \times \pi \times 120}{5.17} = 29.2 \text{ nH}$$

$$N = \sqrt{\frac{3.48 \times 10^3}{29.2}} = 11 \text{ turns}$$

An inductance of L = 13.9 μH corresponds to a reactance of 2183 Ω at 25 MHz which is high enough to be neglected.

According to measurements 10 turns were sufficient to obtain $L_{AB} \approx 3.5\ \mu H$.

3.4 The tapped choke (T2)

The chokes in the drain circuits are wound on a common ferrite rod. The windings are twisted together. Constructional details are shown in Fig.8. With this arrangement the dc flux components in the core cancel out and a much smaller component results. Because a rod has a open magnetic circuit saturation effects will hardly occur.
In Fig.9 the output part of the amplifier is given in a different way.

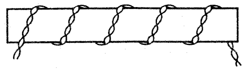


Fig.8

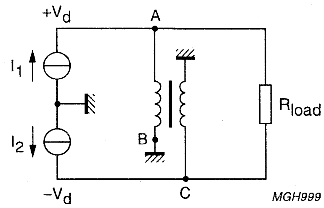


Fig.9

The current sources have a frequency spectrum in which the even order components are in phase and the odd order ones in anti-phase.
For the even harmonics the impedance between point A and C will depend on the coupling factor K between the windings with:

$$\omega L_{AB}(1-K) \tag{12}$$

If the coupling factor amounts to 1 points A and C will be short circuited. If the current components are in anti-phase the total inductance between these points shunts the load resistance. Because the voltage between point A and B is equal to ½ V_{AC} the total inductance L_{AC} is equal to 4 L_{AB} if the coupling factor is 1.
The reactance of this shunting inductance is allowed to be at least 4 times the load resistance or 200 Ω at 25 MHz. So, L_{AC} amounts to 1.27 µH and L_{AB} to 0.318 µH.

To obtain the inductance L_{AB} a ferrite rod grade 4B1 has been used with a length of 30 mm and a diameter of 5 mm. According to ref.(3) its relative permeability is equal to 20. The number of turns can be determined with:

$$N = \sqrt{\frac{L \times l}{\mu o \times \mu r \times A}} \tag{13}$$

For L_{AB} this amount to:

$$N = \sqrt{\frac{0.318 \times 10^{-6} \times 30 \times 10^{-3}}{4 \times \pi \times 10^{-7} \times 1/4 \times \pi \times \left(5 \times 10^{-3}\right)^2}} = 4.4 \text{ turns}$$

In practice 5 turns will be used so L_{AC} will be equal to 1.6 µH. The measured value for L_{AB} was 0.48 µH at 25 MHz. The windings are constructed of enamelled copper wire of 0.8 mm diameter.

4 AMPLIFIER CONSTRUCTION

4.1 Printed circuit board and component layout

The printer circuit board of this amplifier is made of two-sided copper clad epoxy fibre glass (εr = 4.5) laminate of 1/16" thickness.
Circuit components are situated on one side of this board, the other side serves as ground plane. A full sized pattern of the printed circuit board and component layout is given in Fig.13. The parasitic inductance of the printed tracks are absorbed in the inductances of the matching networks. Connections to the ground plane are made by means of tubular rivets, straps under the source leads and at the N-connectors and the mounting screws.

4.2 Heatsink

The printed circuit board is attached to a solid copper plate, with dimensions 120 × 100 × 10 mm, which functions as a heatsink. It is provided with a tube in order to control its temperature by means of a water cooling system. Good thermal contacts between transistors and heatsink is obtained by use of a heat-sinking compound.

5 AMPLIFIER ALIGNMENT

The amplifier was constructed according to the theoretical design procedures. Figure 12 shows the total circuit diagram of this amplifier. Parallel matching components as C1, C5 and C12 are connected directly from one side of the circuit to the other. Therefore their values are exactly one half of those calculated. The component list is given in Table 4.

Alignment of this amplifier was first done on a small signal basis. First the output circuit was aligned by replacing the BLF244 transistors with dummy loads, representing the conjugate of the optimum load impedance. The dummy's consisted of a 25 Ω resistance and a 43 pF capacitance. Several components in parallel were used to obtain symmetry and to reduce parasitic inductances. These components were soldered in an empty SOT123 header. The return loss was measured versus frequency at the load connection of the amplifier and minimized by applying compensation capacitors between the terminals of the output transformer. At the load site of the transformer 3.6 pF (C13) was needed and at the transistor side C12 was increased from 20 to 22 pF. The maximum VSWR obtained was 1.22.

Alignment of the input circuit has been done with the transistors in the circuit and supply and load connected. The quiescent drain current was set to approx. 200 mA per transistor and return loss was measured versus frequency. Experiments with capacitors in parallel with the input transformer terminals showed that no compensation was needed. The maximum VSWR obtained was 1.30.

After the small signal alignment the transistors were set to class-B operation by decreasing the quiescent drain current to 25 mA.
The first results obtained at P_{out} = 30 W were:
Gp = 15.6 ±1.2 dB; Eff. = 61.3 ±10%; VSWR ≤ 1.40 and second harmonic level ≤ –33 dB.

In order to improve the total performance of this amplifier especially with respect to gain flatness, variation in efficiency and second harmonic level some minor changes were introduced in the amplifier.

1. At the input side the circuit configuration shown in Fig.10a was changed into that of Fig.10b. No appreciable improvement was achieved with respect to gain performance but variations in efficiency reduced to ±6%. However, at the lower side of the band the second harmonic level increased to –28 dB.

2. Raising the quiescent drain current to 50 mA improved the gain with approx. 0.3 dB. However, the efficiency decreased with approx. 0.8%.
3. A resistance of approx. 12 Ω from the mid tap of the drain choke T2 to ground instead of direct grounding increased the average efficiency with approx. 1% and its variations decreased to ±2.8%. The second harmonic level improved with 2 dB.
4. The input balun was originally connected as shown in Fig.11a. For a perfect symmetrical push-pull amplifier it does not matter which terminal is grounded. In this case exchange of the terminals strongly affected the second harmonic level. For the case of Fig.11b this level improved to < –40 dB.
5. Finally the value of the resistors shown in Fig.10 was increased to 23.7 Ω. This improved the gain flatness to approx. ±0.6 dB. The input VSWR increased to 1.5.

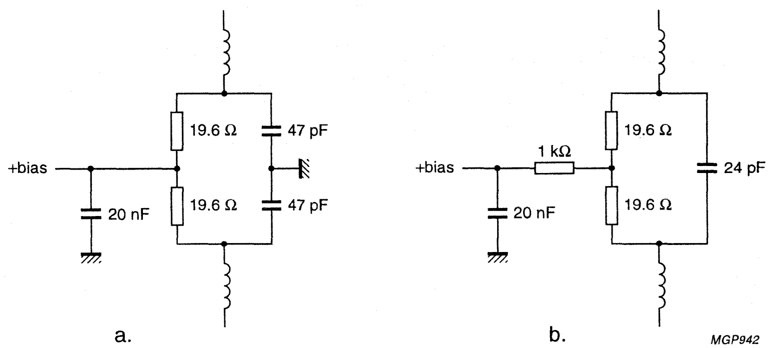


Fig.10

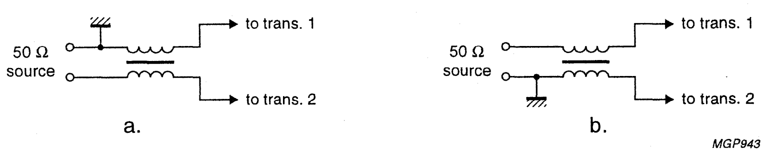


Fig.11

6 AMPLIFIER PERFORMANCE

6.1 General

Measurement of the amplifier performance was carried out under nominal conditions unless stated otherwise. These conditions are:

Supply voltage V_{dd} = 28 V

Quiescent drain current I_{dq} = 50 mA

Heatsink temperature T_{hs} = 25 °C.

Measurements were done at 10 frequencies within the band and 2 frequencies outside the band.

The BLF244 samples used, are matched on their threshold voltage V. The measured parameters of these transistors which can be relevant for balanced operation are given in Table 3.

Table 3

PARAMETER	CONDITIONS	UNIT	T1	T2
V_T	V_{ds} = 10 V; I_d = 5 mA	V	3.14	3.14
G_{FS}	V_{ds} = 10 V; I_d = 750 mA	mS	794	838
C_{rss}	V_{ds} = 28 V; V_{gs} = 0 V; f = 1 MHz	pF	4.46	4.21

The largest asymmetry observed in the drain current was ±3% at f = 25 MHz and P_o = 30 W.

6.2 Performance at constant output power

Measurements of the performance at a constant output power of 30 W were carried out at two heatsink temperatures, viz. T_h = 25 and 70 °C.

The results obtained are:

Powergain = 15.7 ±0.7 dB, see Fig.17

Drain eff. = 60.6 ±3.3%, see Fig.18

Input return loss <–14 dB (VSWR <1.50), see Fig.19

Second harmonic level <–40 dB, see Fig.20

Third harmonic level <–14 dB, see Fig.21.

At T_h = 70 °C the powergain decreased with approx. 1.2 dB see Fig.17.
The other parameters showed no appreciable change.

6.3 Performance at constant input power

Performance of this amplifier was also measured at a constant input power of 700 mW. The result obtained are:

Output power = 27.9 ±2.3 W, see Fig.22

Power gain = 16.0 ±0.3 dB, see Fig.23

Drain eff. = 59.0 ±4.5%, see Fig.24.

6.4 Performance at constant frequency

Figures 25, 26 and 27 show the following curves measured at 5 different frequencies:

$P_o = f(P_i)$

$G_p = f(P_o)$

Eff. = f (P_o).

7 CONCLUSIONS

Using two BLF244 MOS transistors (matched on threshold voltage) in a push-pull configuration approx. 16 dB power gain and 60% drain efficiency have been obtained for an output power of 30 W, when operated with a quiescent drain current of 50 mA per transistor at V_{ds} = 28 V. The largest asymmetry observed in the drain current was ±3% at P_{out} = 30 W and f = 25 MHz. The input VSWR was below 1.5.

Throughout the band the second harmonic level was lower than –40 dB with reference to the fundamental. At a heatsink temperature of 70 °C the powergain decreased with approximately 1 dB while the other parameters showed no appreciable change.

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3. Philips Data Handbook: 'MA01 on Magnetic Products: Soft Ferrites. For power handling of 4C6 material. See also earlier version of this handbook.
4. A.H. Hilbers; 'Power transformers for the frequency range of 30 – 80 MHz'; Laboratory report ECO7703, 1977.

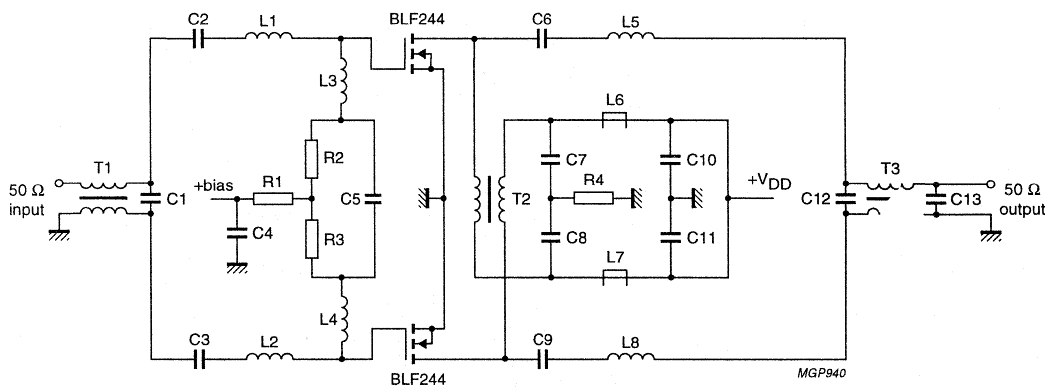


Fig.12 Circuit diagram of the wideband push-pull amplifier.

Table 4 List of components

Capacitors	
C1 = 30 pF	multilayer ceramic chip capacitor; note 1
C2 = C3 = C6 = C7 = C8 = C9 = 10 nF	multilayer ceramic capacitor (cat.nr. 2222 852 47103)
C4 = 2 × 10 nF	multilayer ceramic chip capacitor (cat.nr. 2222 852 47103)
C5 = 24 pF	multilayer ceramic chip capacitor; note 1
C10 = C11 = 100 nF	multilayer ceramic chip capacitor (cat.nr. 2222 852 47104)
C12 = 22 pF	multilayer ceramic chip capacitor; note 1
C13 = 3.6 pF	multilayer ceramic chip capacitor; note 1
Inductors	
L1 = L2 = 27 nH	3 turns enamelled Cu-wire (0.8 mm); int.dia. = 4.0 mm; length = 6.1 mm; leads 2 × 3 mm
L3 = L4 = 48 nH	4 turns enamelled Cu-wire (0.8 mm); int.dia = 4.0 mm; length 6.2 mm; leads 2 × 1 mm
L5 = L8 = 30 nH	3 turns enamelled Cu-wire (0.8 mm); int.dia. = 4.0 mm; length = 4.8 mm; leads 2 × 2 mm
L6 = L7 = Ferroxcube RF choke	grade 3B (cat.nr. 4312 020 36640)
Resistors	
R1 = 1 kΩ	metal film resistor; 0.4 W
R2 = R3 = 23.7 Ω	metal film resistor; 0.4 W
R4 = 12.1 Ω	metal film resistor; 0.4 W
Transformers	
T1– $\frac{1}{1}$ Balun	10 turns of twisted pair of 0.5 mm enamelled Cu-wire (2¾ twists per cm) wound on a toroidal core grade 4C6, dimensions (9 × 6 × 3) mm (cat.nr. 4322 020 97191)
T2– Drain choke	5 turns of twisted pair of enamelled Cu-wire (4.5 twists per cm) wound on a ferroxcube rod grade 4B1, dimensions (5 × 30) mm
T3– $\frac{1}{1}$ Balun	6 turns of twisted pair of 0.6 mm enamelled Cu-wire (2 twists per cm) wound on a toroidal core grade 4C6, dimensions (23 × 14 × 7) mm (cat.nr. 4322 020 97171)
Printed circuit board	double sided Cu-clad epoxy fibreglass laminate (εr = 4.5), thickness 1/16”

Note

1. American Technical Ceramics capacitor type 100B.

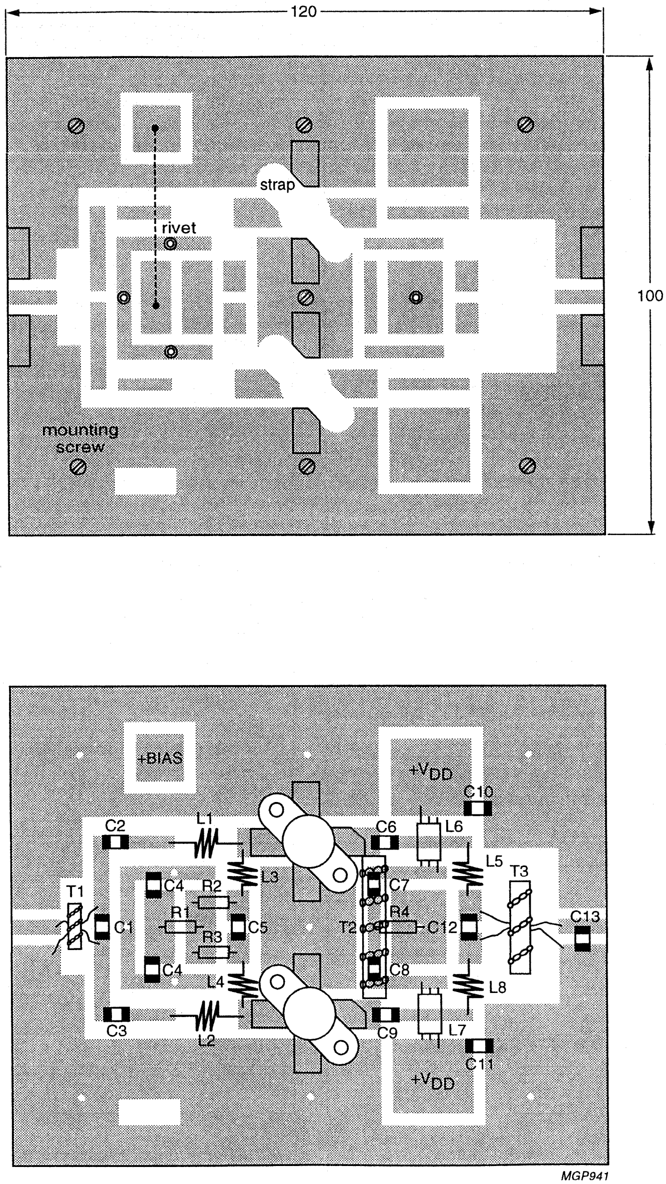


Fig.13 Printed circuit board and component lay-out.

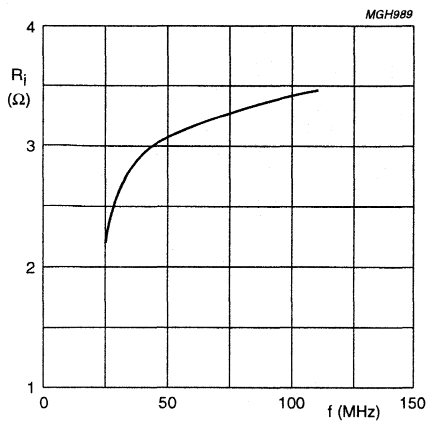


Fig.14 Real part of input impedance.

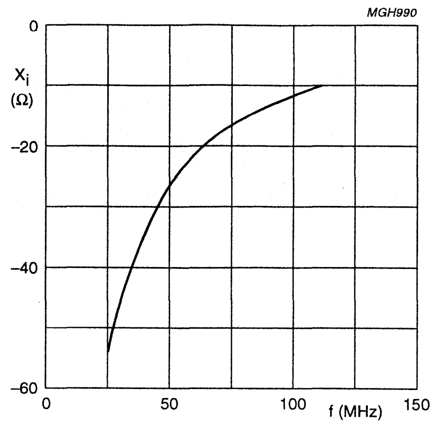


Fig.15 Imaginary part of input impedance.

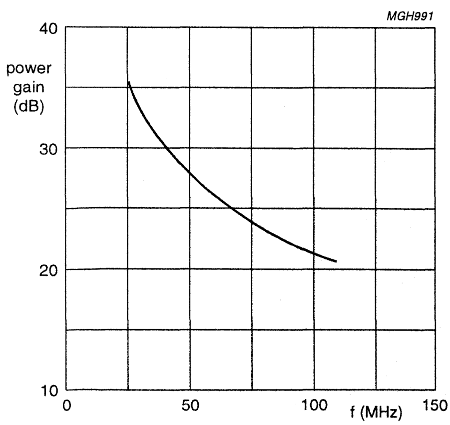


Fig.16 Powergain of transistor.

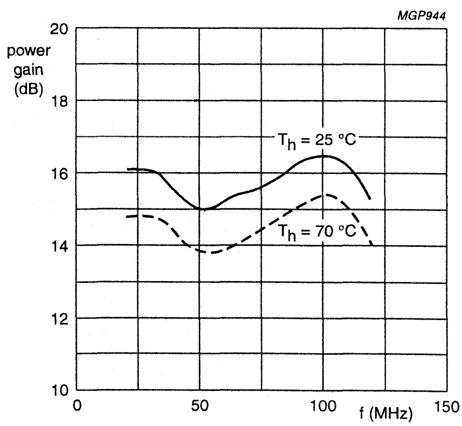


Fig.17 Powergain versus frequency.

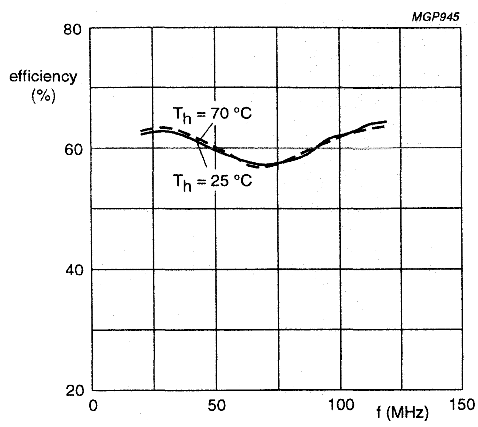


Fig.18 Drain efficiency versus frequency.

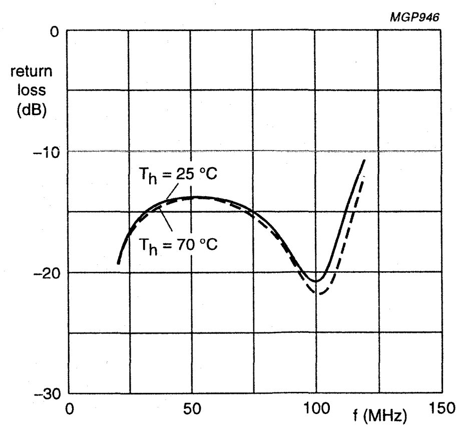


Fig.19 Return loss versus frequency.

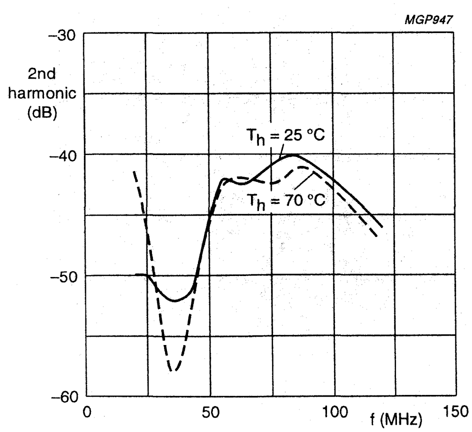


Fig.20 2nd harmonic level versus frequency.

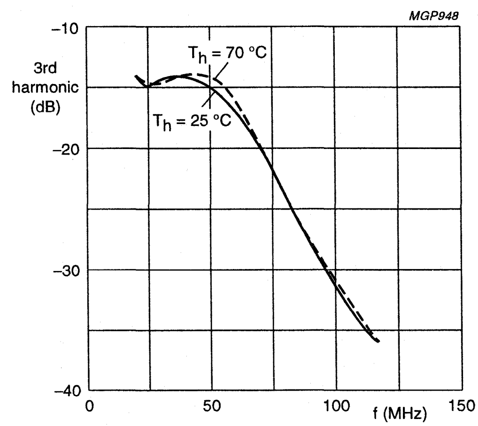


Fig.21 3rd harmonic level versus frequency.

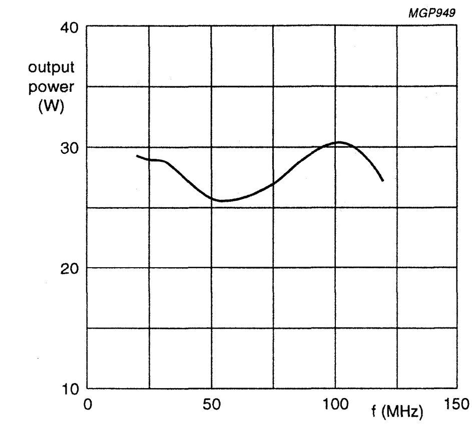


Fig.22 Output power versus frequency.

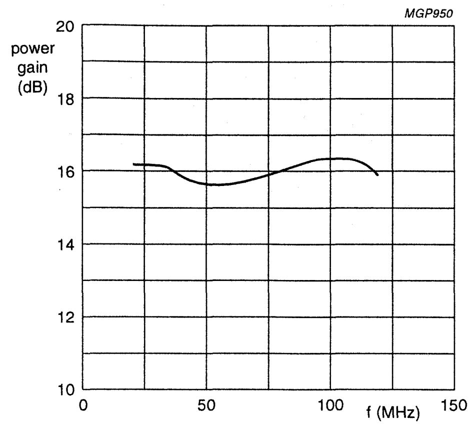


Fig.23 Powergain versus frequency.

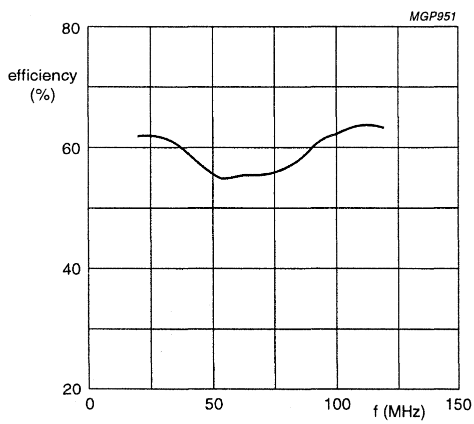


Fig.24 Drain efficiency versus frequency.

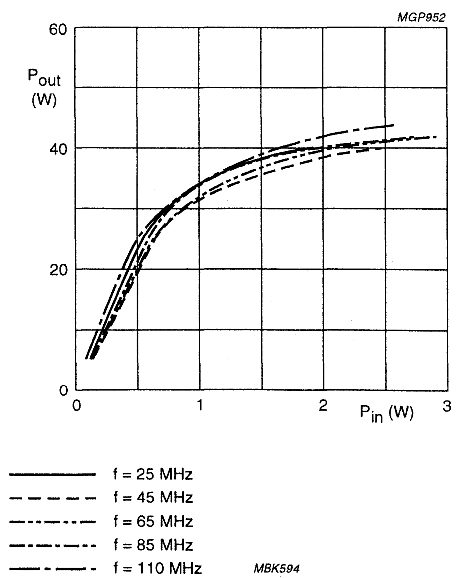


Fig.25 Output power versus input power.

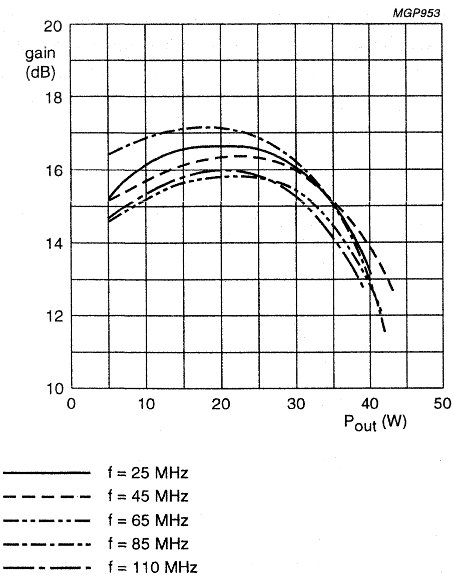


Fig.26 Powergain versus output power.

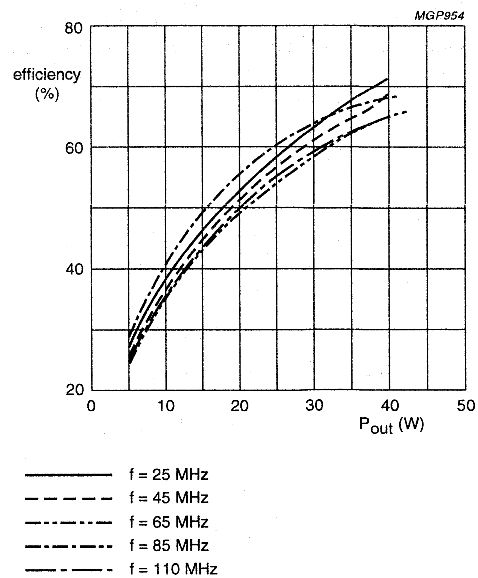


Fig.27 Drain efficiency versus output power.

Performance of 30 W push-pull amplifier for freq. range 25 – 110 MHz with 2 MOS transistors BLF244

Application note
NCO8702

1 INTRODUCTION

In application report NCO8701 a description is given of a wideband power amplifier for the frequency range 25 – 110 MHz. This amplifier is primarily designed for non-linear operation at an output power of 30 W. When this amplifier is used in VHF frequency hopping equipment for military communication purposes linearity is required to some extent, $d_3 < -26$ dB. Also its noise performance is important. To investigate these aspects of the amplifier additional measurements have been carried out.

2 LINEAR PERFORMANCE

A two-tone intermodulation distortion test has been performed on this amplifier. The tone separation was 10 KHz. Measurements were first carried out under nominal conditions, which are:

Supply voltage; V_{dd} = 28 V

Quiescent drain current; I_{dq} = 50 mA/transistor

Heatsink temperature; T_{hs} = 25 °C.

It appeared that the third-order intermodulation distortion product IMD(d3) was the strongest in the output signal. This was < –22.5 dB with reference to one of the two tones at the high end of the band. It also appeared that the IMD products increased at lower power levels. Linearity measurements were repeated at a higher quiescent drain current corresponding with class-AB operation. At I_{dq} = 125 mA transistor IMD(3d) improved to < –26.5 dB. It also turned out that the IMD products at lower power levels did not increase as in the previous case but stayed nearly constant or decreased. Figures 1, 2, 3 and 4 show IMD (d3) versus the peak envelope output power at four different frequencies. Curves are given for both I_{dg} = 50 mA and I_{dg} = 125 mA. Figures 5 and 6 powergain and efficiency versus frequency are given based on two-tone measurements. At I_{dg} = 125 mA the powergain is appr. 1 dB higher than the powergain at I_{dg} = 50 mA. The drain efficiency is approx. 3% lower. Input return loss and output second harmonic suppression at I_{dq} = 125 mA were better than –13.5 dB resp. –37.5 dB.

3 NOISE PERFORMANCE

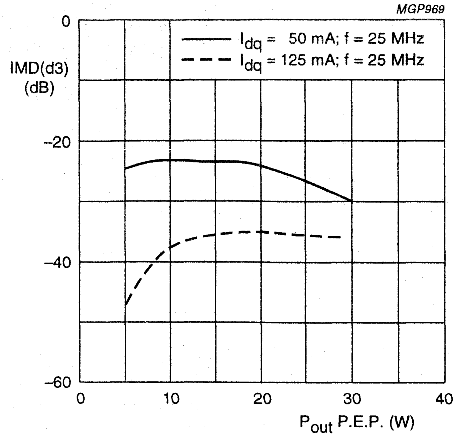
Noise measurements, were performed at several frequencies in the band. Laboratory facilities restricted the lowest frequency of measurement to 40 MHz. Table 1 contains the measured nois figure of the amplifier at four frequencies obtained with the noise generator method. The quiescent drain current was set to 500 mA per transistor.

Table 1

FREQ. (MHz)	F (dB)
40	4.8
50	4.3
90	4.4
110	4.3

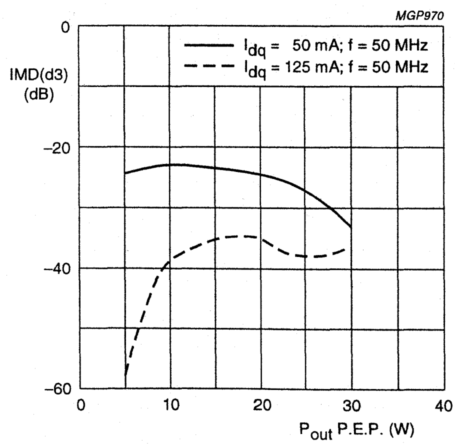
4 CONCLUSIONS

This amplifier can only meet the linearity requirement of < –26 dB over the whole frequency range 25 – 110 MHz if it is operated in class-AB with I_{dg} = 125 mA. When operation is considered only in the band 30 – 88 MHz its IMD is better than –31 dB. The measured noise figure at I_{dg} = 500 mA is 4 – 5 dB.



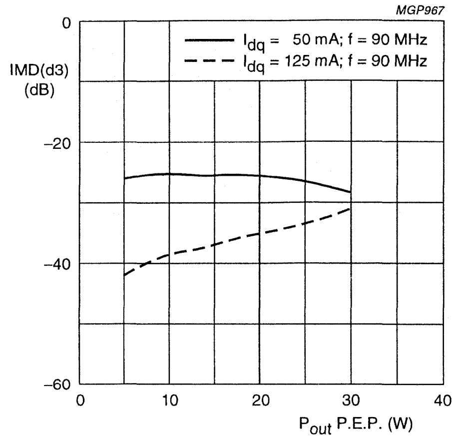
Tone seperation = 10 kHz.

Fig.1 3rd order IMD versus Pout at f = 25 MHz.



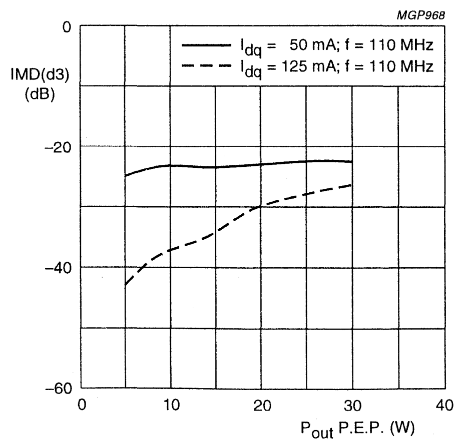
Tone seperation = 10 kHz.

Fig.2 3rd order IMD versus Pout at f = 50 MHz.



Tone seperation = 10 kHz.

Fig.3 3rd order IMD versus Pout at f = 90 MHz.



Tone seperation = 10 kHz.

Fig.4 3rd order IMD versus Pout at f = 110 MHz.

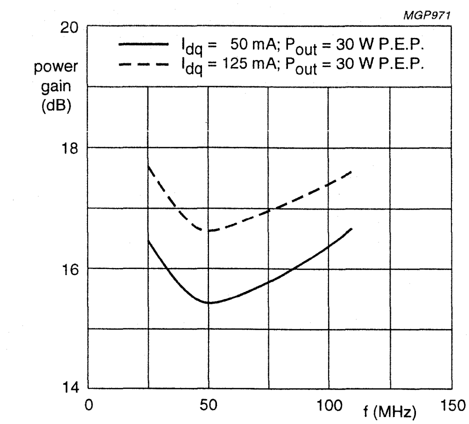


Fig.5 Powergain versus frequency.

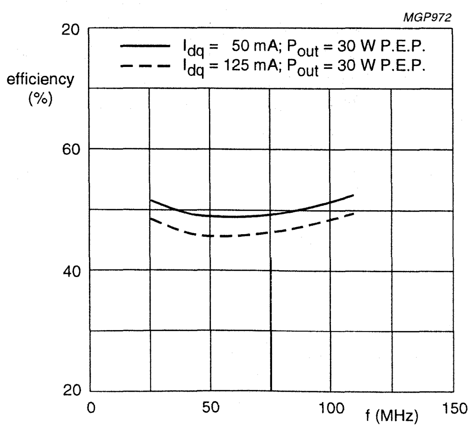


Fig.6 Drain efficiency versus frequency.

A wide-band class-A linear power amplifier (174 – 230 MHz) with two transistors BLV33

Application Note
ECO7904

1 ABSTRACT

For application in driver or final stages of TV-transposers in band III (174 – 230 MHz) a linear wideband power amplifier has been designed with 2 transistors BLV33, coupled by means of 3 dB –90° hybrids.

Each transistor is adjusted in class-A at V_{CE} = 25 V and I_C = 3.25 A. A demonstration model showed a peak sync output power of 40 W at a 3-tone I.M. distortion between –56 and –58 dB. At this power level the cross-modulation varied from 6 to 7.5%. The power gain is between 8.35 and 8.6 dB.

2 INTRODUCTION

For application in T.V. transposers and transmitters for band III a wideband linear power amplifier has been designed with 2 transistors BLV33, coupled by means of 3 dB –90° hybrids. Each transistor is adjusted in class-A at V_{CE} = 25 V and I_C = 3.25 A.

3 DESIGN OF THE AMPLIFIER

For class-A operation the BLV33 is specified at V_{CE} = 25 V, I_C = 3.25 A. The corresponding typical gain, input and load impedance are given below:

Table 1

FREQ. (MHz)	GAIN (dB)	INPUT IMPEDANCE (Ω)	LOAD IMPEDANCE (Ω)
174	11.3	0.68 + j1.20	2.70 + j1.19
202	10.1	0.68 + j1.43	2.30 + j0.87
230	9.08	0.68 + j1.64	1.99 + j0.52

A computer-aided circuit design, carried out by Mr. Hilbers (Central Application Laboratory) indicated a gain of 9.1 dB ±0.1 dB and V.S.W.R. figures of 4.3 (170 MHz), 2.78 (202 MHz) and 1.18 at 230 MHz for a single amplifier.

To obtain a high linear output and at the same time good input and output matching (V.S.W.R. ≤ 1.2) 3 dB –90° hybrids are used. The reflected input power will be absorbed in the 50 Ω resistor, matching the isolated port (see Fig.1). There are some small differences (value and place of chip capacitors) between the theoretical design and practical circuit. For detailed information on computer-aided design see Refs 1 and 2. Mainly due to the insertion loss of the 3 dB hybrids the gain drops from 9 to 8.5 dB. The transistors used in this particular amplifier are typical products, measured in a narrow band test amplifier and specified as follows:

V_{CE} = 25 V – I_C = 3.25 A – T_h = 70 °C

Table 2

Transistor type	BLV33	
Batch no.	MD 8-14 no 5	MD 8-14 no 10
Vision frequency	224.25 MHz	
Output power (peak sync)	22.9 W	22.6 W
Intermodulation product	−55 dB	−55 dB
Gain	9.03 dB	9.11 dB

4 ADJUSTMENTS OF THE AMPLIFIER

The amplifier consists of two equal BLV33 branches (see Fig.1) and both transistors are separately biased at V_{CE} = 25 V, I_C = 3.25 A. A schematic diagram and lay-out of the bias unit is given in Fig.2. Each branch was adjusted for maximum and flat gain by means of a high power sweep with a frequency range from 170 to 230 MHz. The output power of the amplifier was levelled at 40 W which means about 50% of the D.C. input power.

After that, both branches are coupled by means of 3 dB −90° hybrids, input and output matching of the complete amplifier are adjusted below a V.S.W.R. of 1.2 with the aid of capacitors C1-C2-C37-C38 as shown in Fig.1.

5 ASSEMBLING OF THE AMPLIFIER AND MECHANICAL DATA

Due to the dimensions of the p.c. board (220 × 210 mm) 2 extruded blackened aluminium heatsinks (cat. no. 56293) are screwed together. The transistors are screwed on an aluminium plate (thickness 12 mm) which on its turn is screwed on the heatsink. Special attention has been paid to the surface finishing to keep the thermal resistance as low as possible. Figure 3 showed the p.c. board and lay-out of the amplifier.

Dimensions: l = 224 mm – w = 223 mm – h = 113 mm. Weight: 7.5 kg.

6 MEASURED RESULTS

Table 3

Frequency range	170 to 230 MHz		
Output power (peak sync)	30 W	40 W	50 W
I.M. distortion	−60 dB	−56 dB	−54 dB; note 1
Cross modulation	3%	6/7.5%	10/15.5%; note 2
Output power for 1 dB gain compression	100 W		
Gain at 40 W output level	8.5 dB ±0.1 dB		
Input and output V.S.W.R.	≤1.2		
Ambient temp.	25 °C		
Heatsink temp.	65 °C		
Transistor stud temp.	85 °C		

Notes

1. Vision carrier −8 dB, sound carrier −7 dB, side signal −16 dB, zero dB corresponds to peak sync level; $f_{sound} = f_{vision} + 5.5$ MHz, $f_{sideband} = f_{vision} - 1$ MHz to $f_{vision} + 6$ MHz.
2. Vision carrier 0 dB, sound carrier −7 dB: voltage variation of sound carrier (%) when the vision carrier is switched from −20 dB to 0 dB; $f_{sound} = f_{vision} + 5.5$ MHz.

In Fig.4 the typical results of crossmodulation and intermodulation measurements on a demonstration amplifier have been given. Figures 5 and 6 show the S-parameters of the complete amplifier. The measuring set-up is depicted in Fig.7.

7 CONCLUSION

Two transistors BLV33, coupled by means of 3 dB –90° hybrids, can deliver an output power of typ. 40 W with an associated gain of 8.5 dB. Required D.C. input power approx. 165 W. Using a high power sweep with adjustable transistor output power levelling provides a suitable method to adjust a linear wideband power amplifier.

8 REFERENCES

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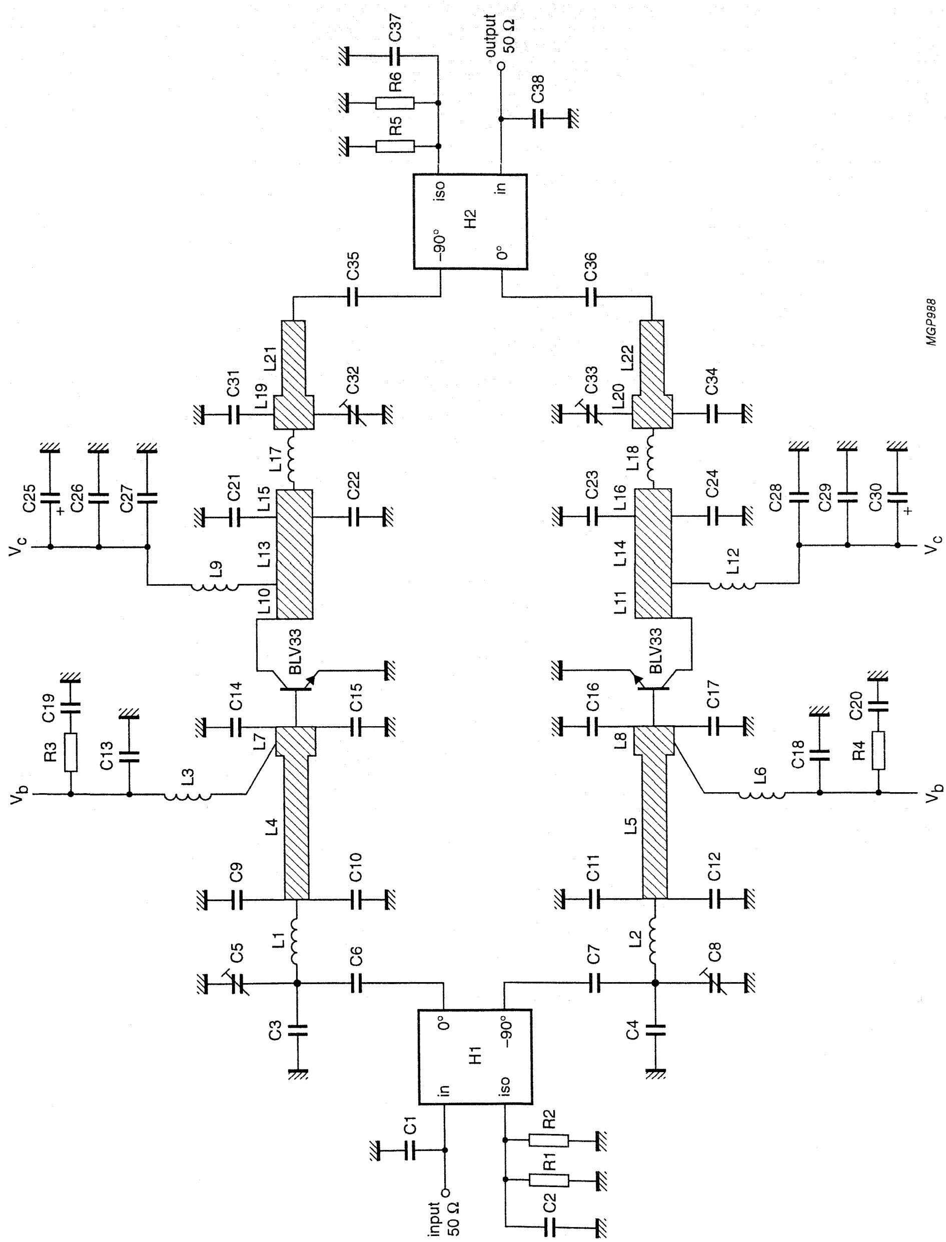


Fig.1 Band III Class A linear power amplifier (170 – 230 MHz).

Table 4

Parts list: Band III class A linear power amplifier (170 – 230 MHz)

C1 = C38	1.5 pF	chip capacitor
C2 = C3 = C4 = C37	5.6 pF	chip capacitor
C5 = C8 = C32 = C33	1.8 to 10 pF	film dielectric trimmer (cat. no. 222280905002)
C6 = C7 = C35 = C36	220 pF	chip capacitor
C9 = C10 = C11 = C12	18 pF	chip capacitor
C13 = C18 = C27 = C28	1000 pF	chip capacitor
C14 = C15 = C16 = C17	100 pF	chip capacitor
C19 = C20 = C26 = C29	330 nF	metallized film capacitor (cat. no. 222235225334)
C21 = C23	68 pF	chip capacitor
C22 = C24	56 pF	chip capacitor
C25 = C30	10 μF (40 V)	electrolytic capacitor (cat. no. 222212117109)
C31 = C34	22 pF	chip capacitor (chip capacitors: ATC type 100B – C – MSX – 500)
R1 = R2 = R5 = R6	100 Ω	power metal film resistor, PR52 type (cat. no. 232219231001)
R3 = R4	10 Ω	carbon resistor, CR68 type (cat. no. 23222141309)
H1 = H2	3 dB –90°	coupler model no. 10262 –3, range 125 – 250 MHz, Anaren Microwave Inc.
L1 = L2	25 nH	2 turns enamelled Cu wire (1 mm); int. diam. 5 mm; length 5 mm; leads 2 × 3 mm
L3 = L6	90 nH	5 turns closely wound enamelled Cu wire (1 mm); int. diam. 4.5 mm; leads 2 × 9 mm
L4 = L5		60 Ω stripline; w = 2 mm; l = 30 mm
L7 = L8		30 Ω stripline; w = 6 mm; l = 11 mm
L9 = L12	20 nH	Cu strip (1 mm); l = 17 mm; h = 5 mm; w = 4 mm
L10 = L11		30 Ω stripline; w = 6 mm; l = 8 mm
L13 = L14		30 Ω stripline; w = 6 mm; l = 14 mm
L15 = L16		30 Ω stripline; w = 6 mm; l = 4 mm
L17 = L18	22 nH	2 turns closely wound Cu wire (1.5 mm); int. diam. 4.5 mm; leads 2 × 3 mm
L19 = L20		30 Ω stripline; w = 6 mm; l = 6 mm
L21 = L22		50 Ω stripline; w = 3 mm; l = 15 mm

The striplines are printed on double Cu-clad printed circuit board with epoxy fibre-glass dielectric (ε_r = 4.5); thickness 1/16 inch.

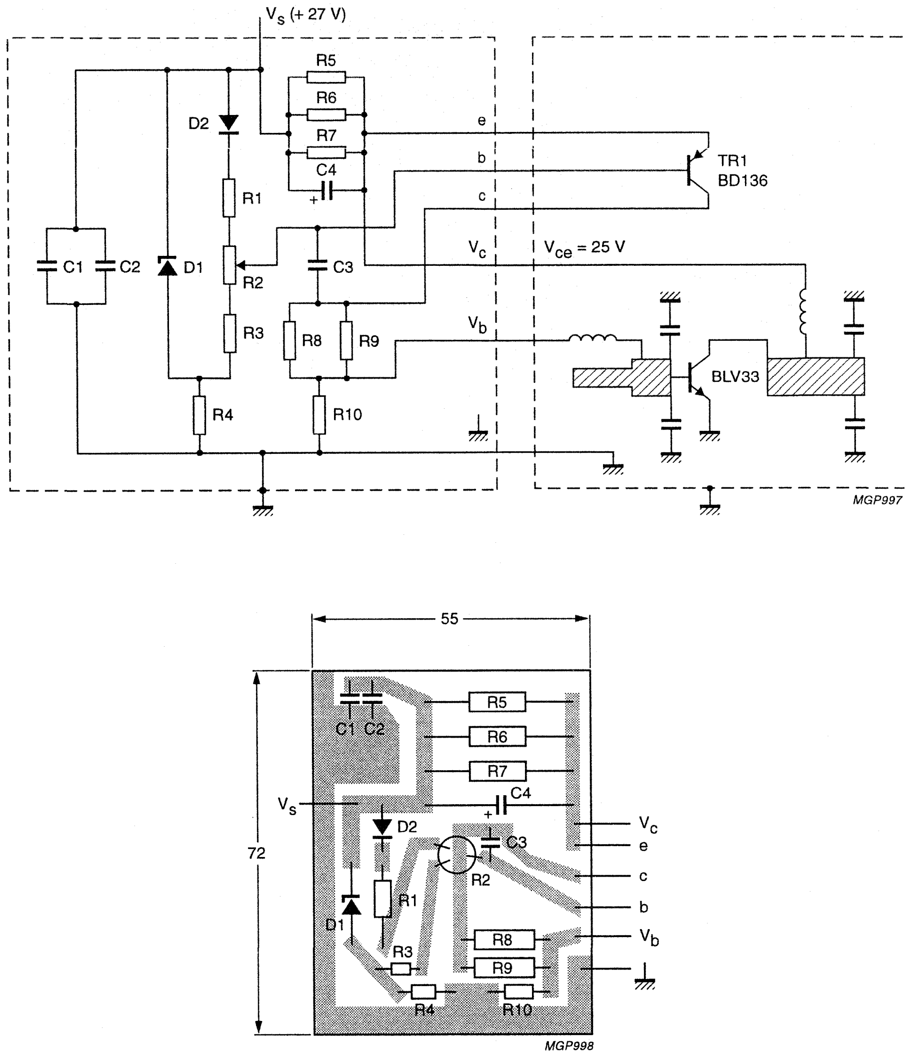


Fig.2 Class A bias circuit for a single transistor BLV33.

Table 5

Parts list: Class A bias circuit for a single transistor BLV33

R1	150 Ω	carbon resistor CR25 type
R2	100 Ω	preset potentiometer CTP10 type
R3	10 Ω	carbon resistor CR25 type
R4	1000 Ω	carbon resistor CR25 type
R5 = R6 = R7	1.8 Ω	rectangular wirewound resistor EH707 type
R8 = R9	180 Ω	carbon resistor CR25 type
R10	33 Ω	carbon resistor CR25 type
C1 = C3	100 nF	metallized film capacitor
C2	100 pF	ceramic capacitor
C4	10 μF	40 V electrolytic capacitor
D1	BZY 88 (3V3)	
D2	BY 206	
T1	BD 136	

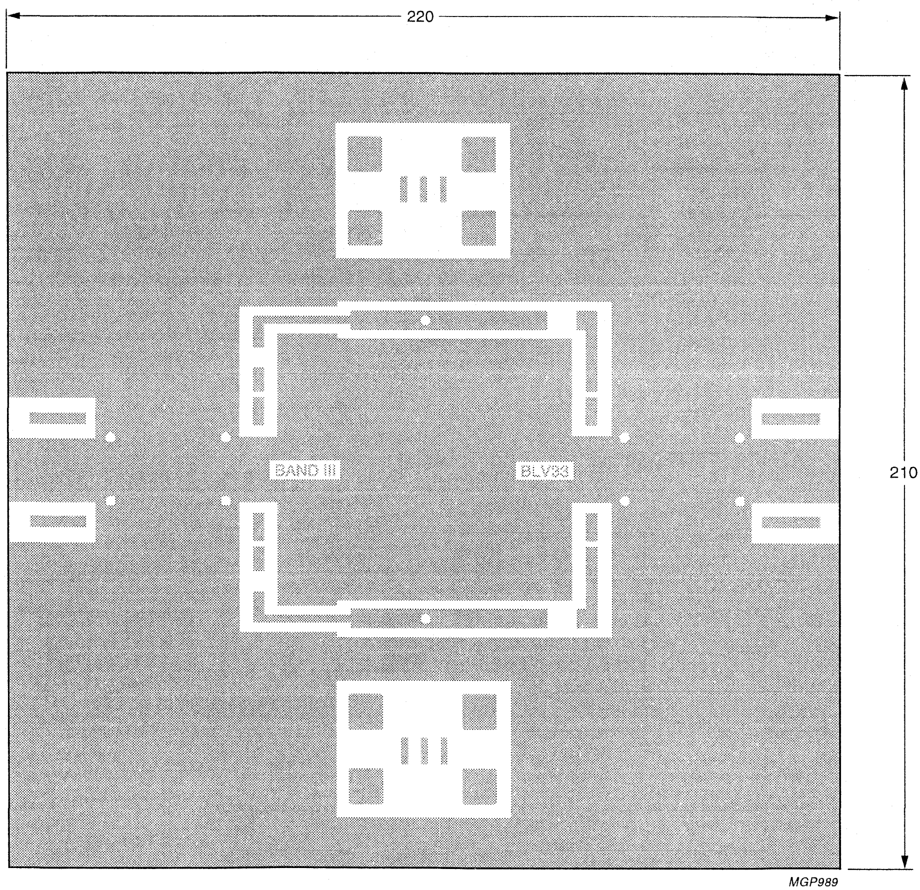
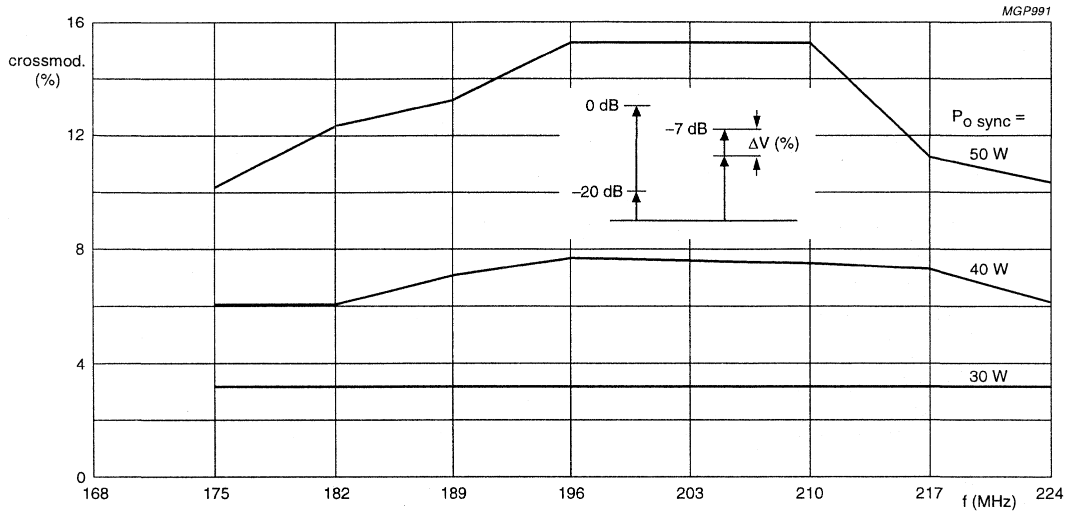
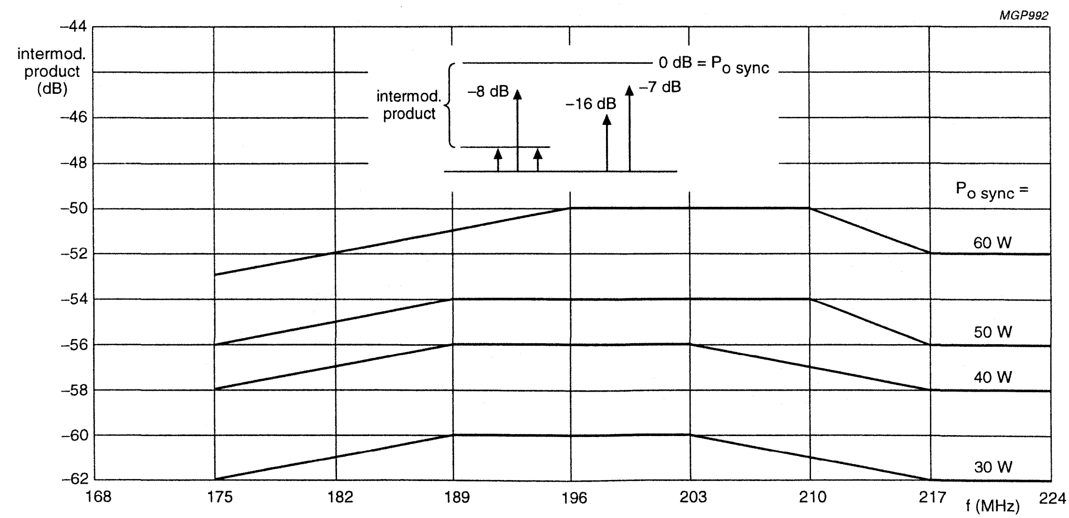


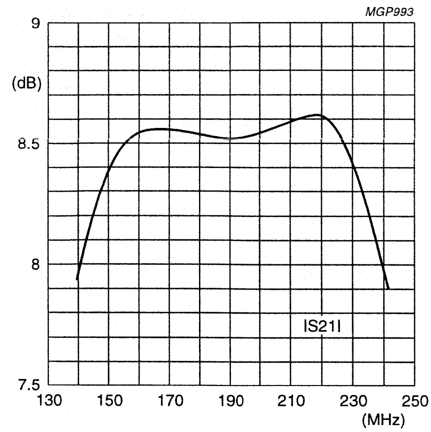
Fig.3 P.C. Board and 2× BLV33 amplifier lay-out.



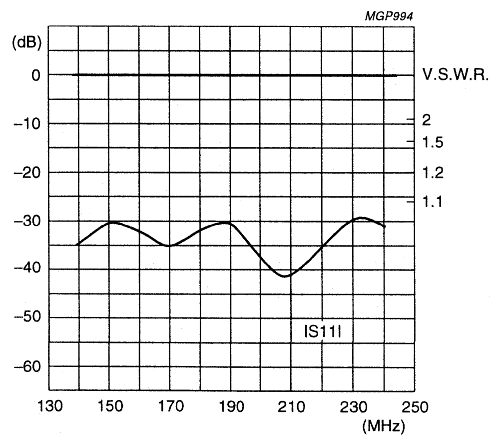


Vision carrier level: −20 dB/0 dB.
Sound carrier level: −7 dB.
Sync level: 0 dB.

Fig.4 Crossmodulation and intermodulation products of the 2× BLV33 wideband Band III power amplifier.

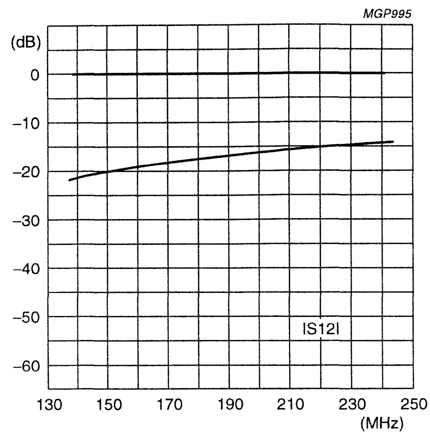


a. Forward transducer gain.

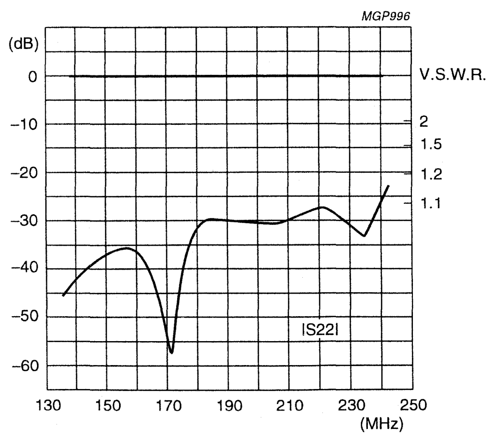


b. Input voltage standing wave ratio.

Fig.5 2× BLV33 wideband Band III power amplifier.



a. Reverse transducer gain.



b. Output voltage standing wave ratio.

Fig.6 2× BLV33 wideband Band III power amplifier.

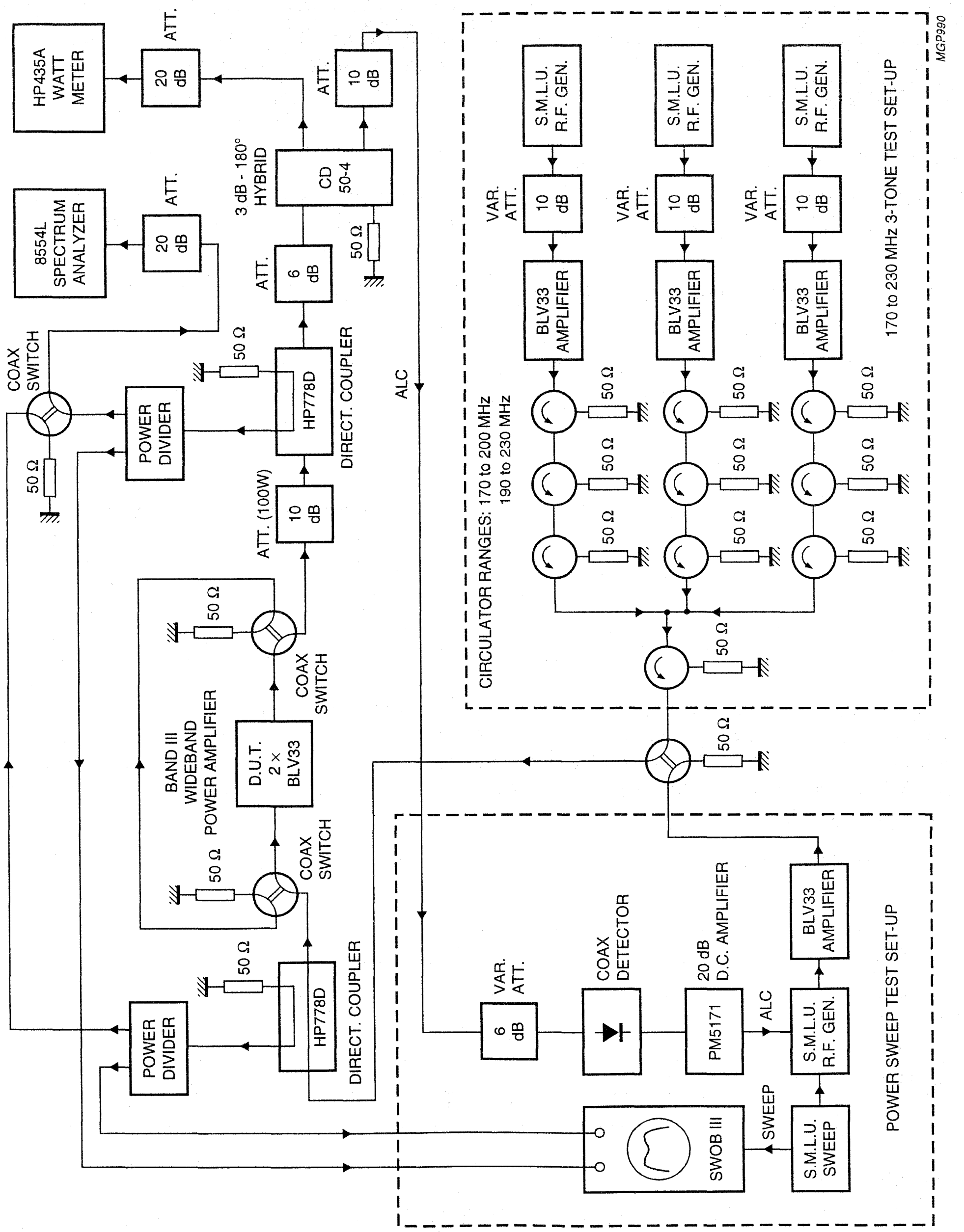


Fig.7 Test set up 2× BLV33 Band III power amplifier.

A wide-band class-A linear power amplifier (174 – 230 MHz) with 2 transistors BLV33F

Application Note ECO8005

1 ABSTRACT

For application in driver or final stages of TV-transposers in Band III (174-230 MHz) a linear wideband power amplifier has been designed with 2 transistors BLV33F, coupled by means of 3 dB – 90° hybrids.
Each transistor is adjusted in Class-A at V_{CE} = 25 V and I_C = 3.25 A. A demonstration model showed a peak sync. output power of 40 W at a 3-tone I.M. distortion between –52 and –53 dB. At this power level the cross-modulation varied from 15 to 18%. The power gain is between 13.3 and 13.6 dB. For natural convection cooling the heatsink temperature is 40 °C above ambient temperature.

2 INTRODUCTION

For application in T.V. transposers and transmitters for Band III a wideband linear power amplifier has been designed with 2 transistors BLV33F, coupled by means of 3 dB –90° hybrids. Each transistor is adjusted in Class-A at V_{CE} = 25 V and I_C = 3.25 A.

Note: The BLV33F is a high gain, internally matched, 1/2 inch 6 leads flange version of the BLV33.

3 DESIGN OF THE AMPLIFIER

For class-A operation the BLV33F is specified at V_{CE} = 25 V, I_C = 3.25 A. The corresponding typical gain, input and load impedance are given in Table 1:

Table 1

FREQ. (MHz)	GAIN (dB)	INPUT IMPEDANCE (Ω)	LOAD IMPEDANCE (Ω)
174	12.94	0.85 + j0.59	2.68 + j1.24
202	12.88	1.02 + j0.47	2.23 + j0.90
230	13.91	0.93 + j0.02	1.84 + j0.51

To obtain a high linear output and at the same time good input and output matching (V.S.W.R. ≤1.2) 3 dB –90° hybrids are used. The reflected input power will be absorbed in the 50 Ω resistor, matching the isolated port (see Fig.1). For detailed information on computer-aided design (carried out by Mr. Hilbers Central Application Laboratory) see Refs 1, 2 and 3. The transistors used in this particular amplifier are typical products, measured in a narrow band test amplifier and specified as follows:

V_{CE} = 25 V – I_C = 3.25 A – Th = 70°

Table 2

Transistor type	BLV33F	
Batch no.	MD 8-16 no.7	MD 8-16 no. 10
Vision frequency	224.25 MHz	
Output power (peak sync)	17.7 W	18 W
Intermod. product	–55 dB	–55 dB
Gain	14.2 dB	14.2 dB

4 ADJUSTMENTS OF THE AMPLIFIER

The amplifier consists of two equal BLV33F branches (see Fig.1) and both transistors are separately biased at V_{CE} = 25 V – I_C = 3.25 A. The printed circuit board of the 2× BLV33F wideband amplifier is given in Fig.2 and schematic diagram + lay-out of the bias unit is given in Fig.3. Figure 9 at the end of the report shows the lay-out of the amplifier with the situation of the components. Each branch was adjusted for maximum and flat gain by means of a high power sweep with a frequency range from 170 – 230 MHz. The output of the amplifier was levelled at 40 W which means about 50% of the D.C. input power. After that, both branches are coupled by means of 3 dB –90° hybrids.

5 ASSEMBLING OF THE AMPLIFIER AND MECHANICAL DATA

Due to the dimensions of the printed circuit board (220 × 210 mm) 2 extruded blackened aluminium heat sinks (cat.no. 56293) are screwed on an aluminium plate (thickness 12 mm) which on its turn is screwed on the heat sink. Special attention has been paid to the surface finishing to keep the thermal resistance as low as possible.

Dimensions of the amplifier: l = 224 mm – w = 223 mm – h = 113 mm. Weight: 7.5 kg.

6 MEASURED RESULTS

In Fig.4 the typical results of crossmodulation and 3-tone intermod. product (from 170 – 230 MHz) have been given for peak sync output powers of 30 W and 40 W. Figure 5 shows peak sync output power as function of 3-tone intermod. products (measured on channel 12: Vision freq. 224.25 MHz – Sound freq. 229.75 MHz). In Figs 6 and 7 the forward and reverse transducer gain as well as input and output voltage standing wave ratio are given. The measuring test set-up is depicted in Fig.8.

Note:
Signal levels 3-tone measurements:
Vision carrier –8 dB; Sound carrier –7 dB;
Sideband –16 dB; 0 dB corresponds to peak sync.

Signals levels crossmodulation:
Vision carrier switched from –20 dB to 0 dB;
Sound carrier –7 dB; 0 dB = peak sync level
Crossmodulation is defined as the voltage variation (%) of the sound carrier.

7 CONCLUSION

Two transistors BLV33F, coupled by means of 3 dB –90° hybrids, can deliver an output power (peak sync) of typ. 40 W for –52 dB 3-tone intermodulation. At 40 W output the crossmodulation varied from 15% to 18% in Band III (170 – 230 MHz). The gain of the amplifier is typically 13.3 + 0.3 dB. The required D.C. input is approx. 165 W. Using a high power sweep with adjustable transistor output levelling provides a suitable method to adjust a linear wideband power amplifier.

8 REFERENCES

Ref.1:
G.L. Matthaei – Tables of Chebyshev
Impedance Transforming Network of Low-Pass Filter Form. Proceedings of the IEEE August 1964, pp 939 – 963.

Ref.2:
A.H. Hilbers and M.J. Köppen – A wideband linear power amplifier (470 – 860 MHz) with two transistors BLW34. C.A.B. report ECO7901.

Ref.3:
R.F.F. Zwanen – A wideband Class-A linear power amplifier (170 – 230 MHz) with two transistors BLV33. C.A.B. report ECO7904.

A wide-band class-A linear power amplifier (174 – 230 MHz) with 2 transistors BLV33F

Application Note ECO8005

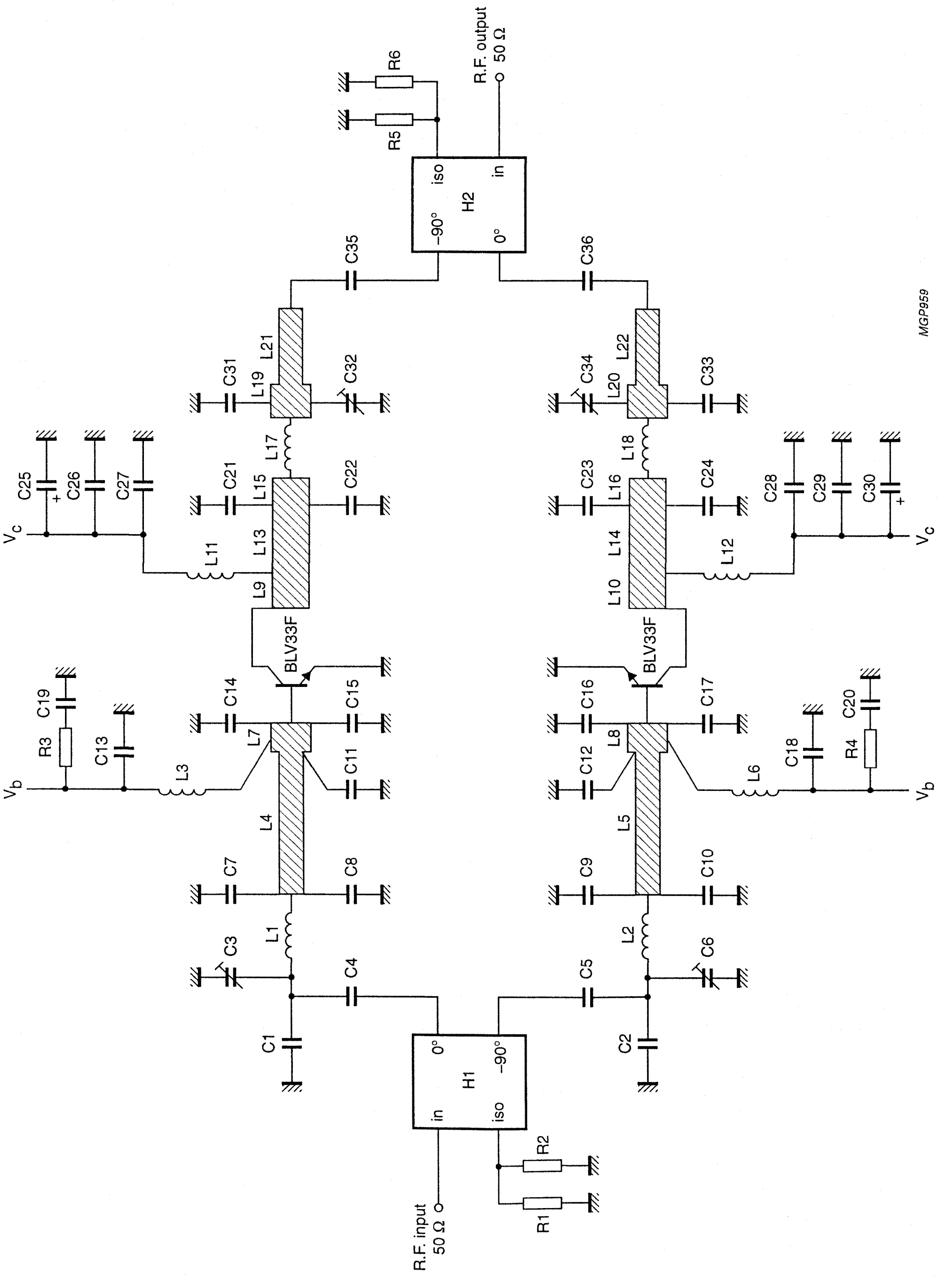


Fig.1 2× BLV33F Band III Class A linear power amplifier.

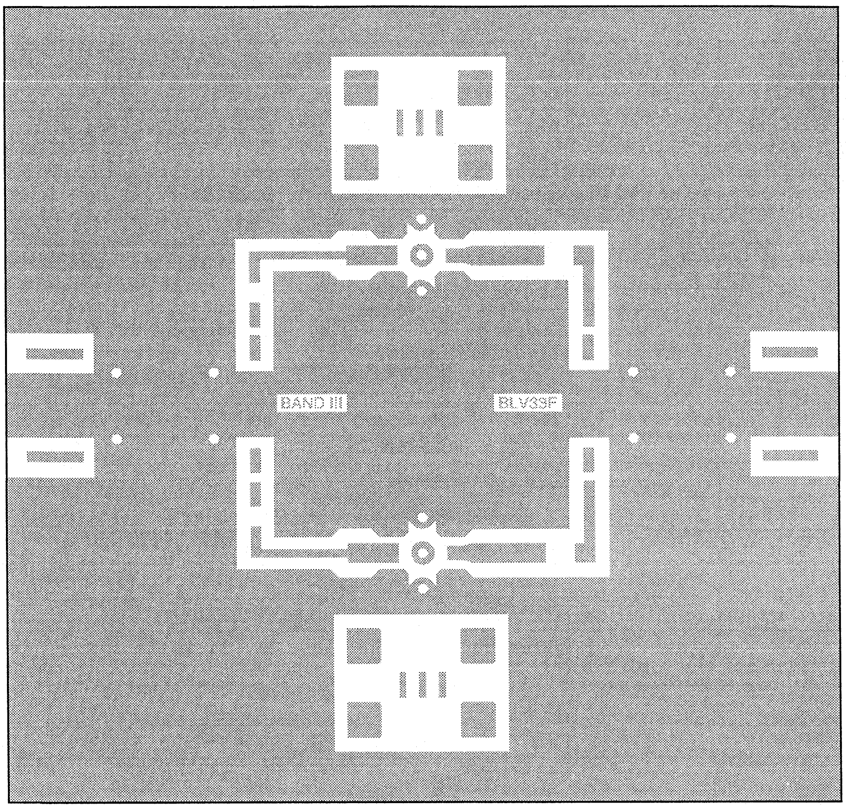


Fig.2 Printed circuit board 2× BLV33F wideband power amplifier.

Table 3 Parts list: BLV33F Band III Class A linear power amplifier (170 – 230 MHz)

C1 = C2 = C7 = C9	10 pF	chip capacitor
C3 = C6 = C32 = C34	1.8 to 10 pF	film dielectric trimmer (cat. no. 222280905002)
C4 = C5 = C35 = C36	220 pF	chip capacitor
C8 = C10	39 pF	chip capacitor
C11 = C12	68 pF	chip capacitor
C13 = C18 = C27 = C28	1000 pF	chip capacitor
C14 = C15 = C16 = C17	120 pF	chip capacitor
C19 = C20 = C26 = C29	300 nF	metallized film capacitor (cat. no. 222235225334)
C21 = C22 = C23 = C24	56 pF	chip capacitor
C25 = C30	10 μF (40 V)	electrolytic capacitor (cat. no. 222212117109)
C31 = C33	18 pF	chip capacitor (chip capacitors: ATC type 100B – C – MSX – 500)
R1 = R2 = R5 = R6	100 Ω	power metal film resistor PR52 type (cat. no. 232219231001)
R3 = R4	10 Ω	carbon resistor CR68 type
H1 = H2	3 dB –90°	coupler, model no. 10262 – 3, range 125 to 250 MHz, ANAREN MICROWAVE INC.
L1 = L2	25 nH	2 turns enamelled Cu wire (1 mm); int. diam. 5 mm; leads 2 × 3 mm
L3 = L6	90 nH	5 turns closely wound enamelled Cu wire (1.5 mm) int. diam. 6.5 mm; length 5 mm; leads 2 × 9 mm
L4 = L5		60 Ω stripline; w = 2 mm; length = 30 mm
L7 = L8		30 Ω stripline; w = 6 mm; length = 11 mm
L9 = L10		40 Ω stripline; w = 4 mm; length = 5 mm
L11 = L12	20 nH	Cu strip (1 mm); length = 17 mm; h = 5 mm; w = 4 mm
L13 = L14		30 Ω stripline; w = 6 mm; length = 17 mm
L15 = L16		30 Ω stripline; w = 6 mm; length = 4 mm
L17 = L18	28 nH	2 turns enamelled Cu wire (1.5 mm); int. diam. 6.5 mm; length 9 mm; leads 2 × 3 mm
L19 = L20		30 Ω stripline; w = 6 mm; length = 6 mm
L21 = L22		50 Ω stripline; w = 3 mm; length = 15 mm

The striplines are printed on double Cu-clad printed circuit board with epoxy fibre-glass dielectric (ε_r = 4.5); thickness 1/16 inch.

Table 4 Parts list: Class A bias circuit for a single transistor BLV33F

R1	150 Ω	carbon resistor CR25 type
R2	100 Ω	preset potentiometer CTP10 type
R3	10 Ω	carbon resistor CR25 type
R4	1000 Ω	carbon resistor CR25 type
R5 = R6 = R7	1.8 Ω	rectangular wirewound resistor EH707 type
R8 = R9	180 Ω	carbon resistor CR25 type
R10	33 Ω	carbon resistor CR25 type
C1 = C3	100 nF	metallized film capacitor
C2	100 pF	ceramic capacitor
C4	10 µF	electrolytic capacitor
D1		BZY 88 (3V3)
D2		BY 206
T1		BD 136

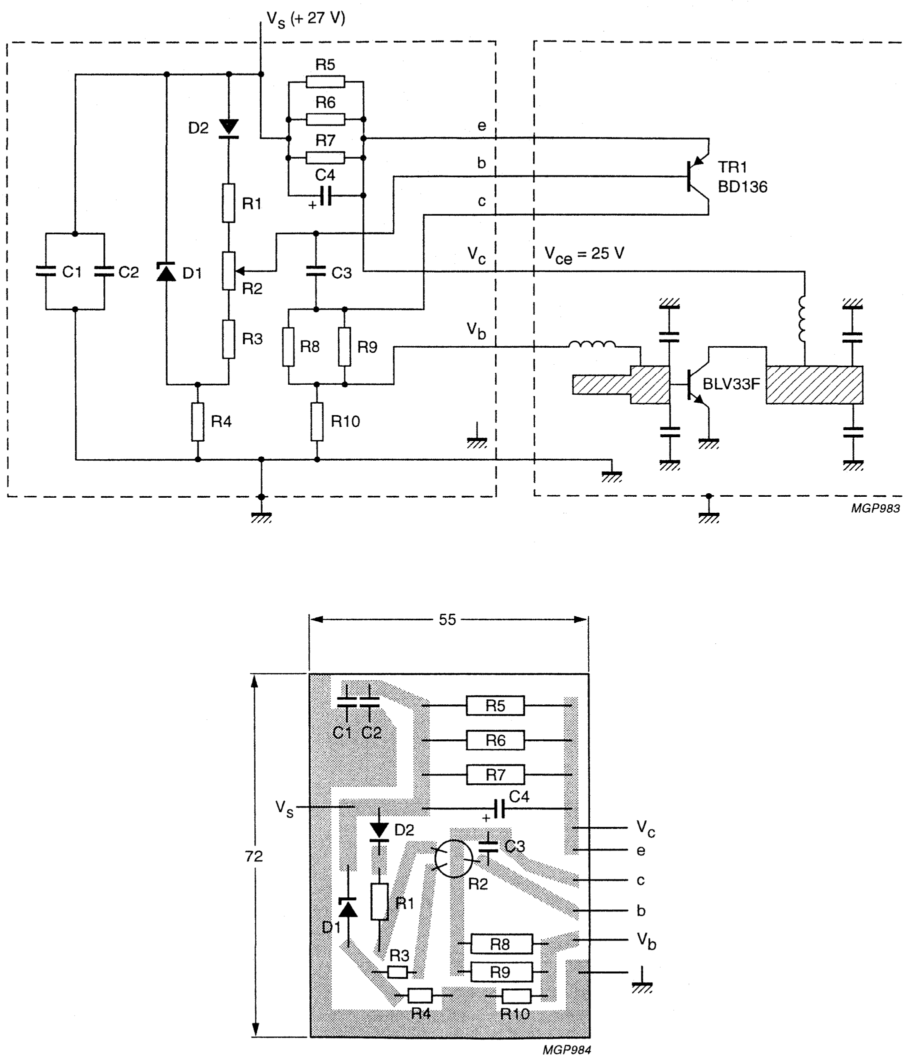
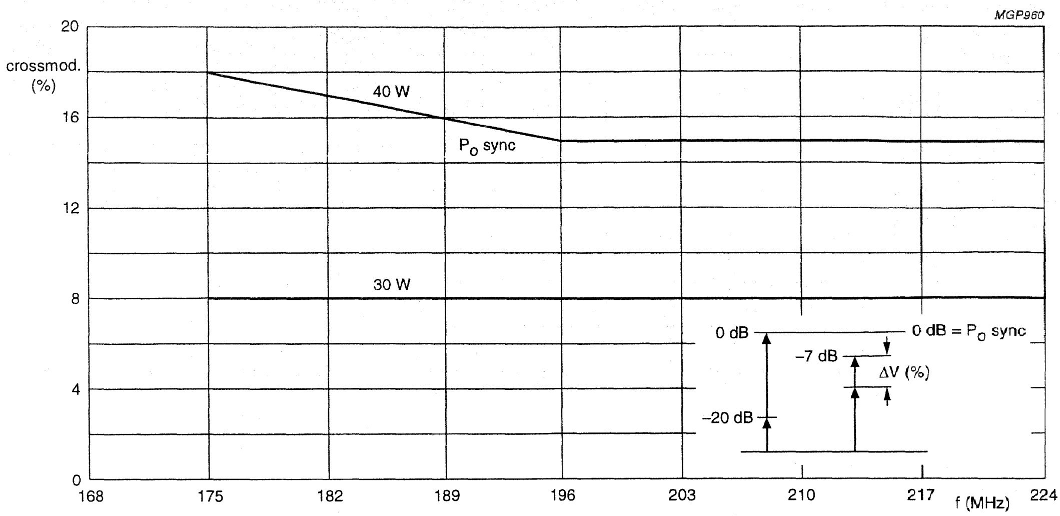
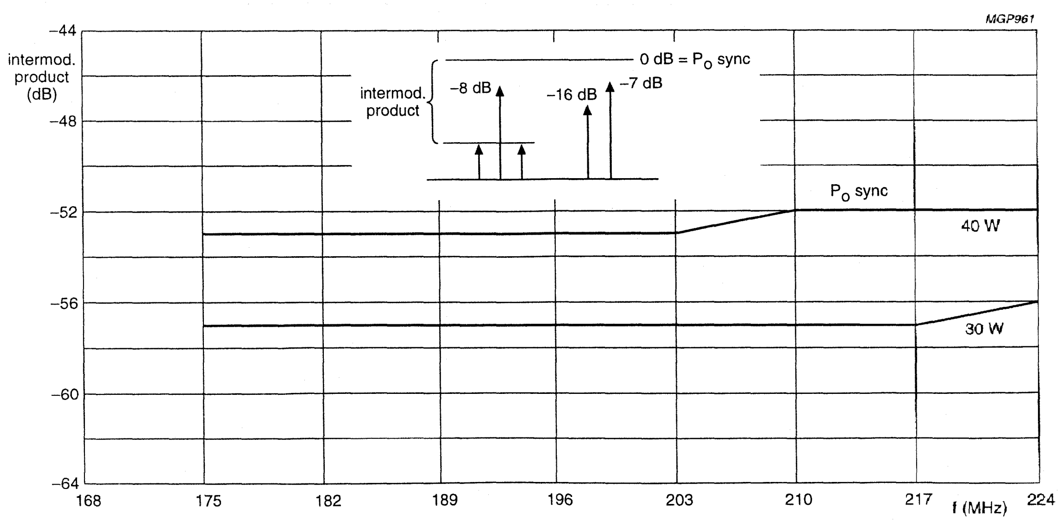


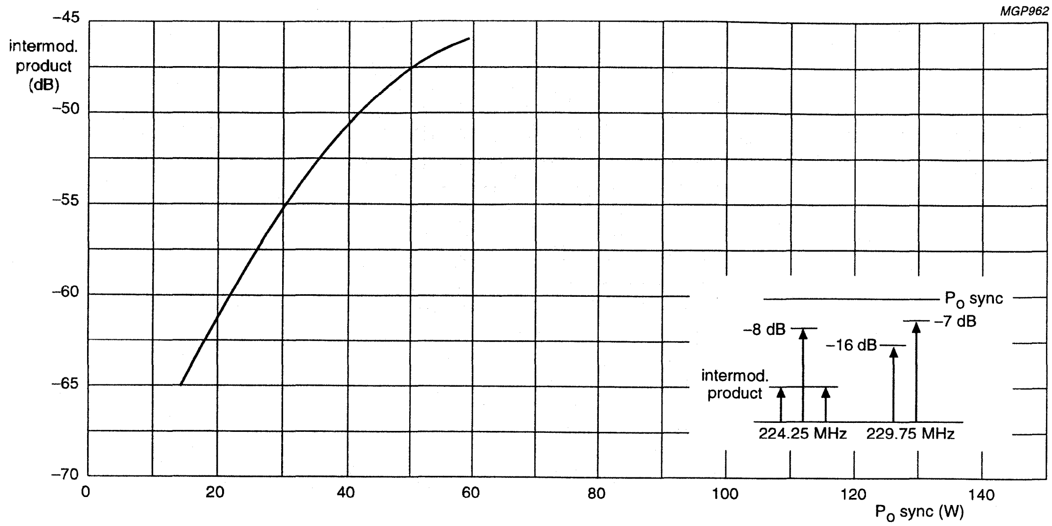
Fig.3 Class A bias circuit for a single transistor BLV33F.





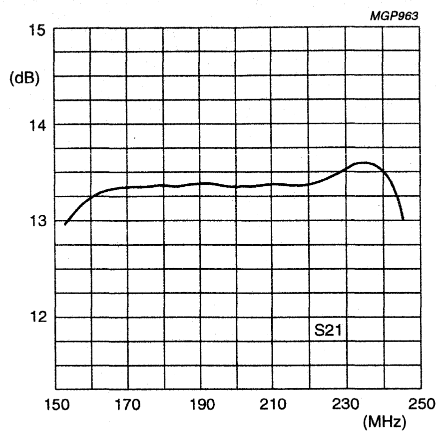
2× BLV33F Class A linear power amplifier.
V_{CE} – 25 V – I_C = 2 × 3.25 A – T_{amb} – 23 °C – Th = 65 °C.

Fig.4 Crossmodulation and intermodulation products of the 2× BLV33F wideband Band III linear power amplifier.

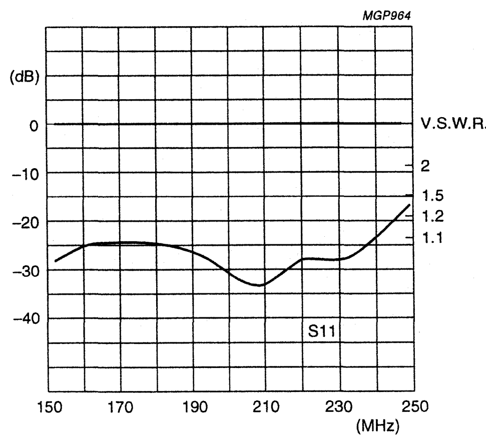


2× BLV33F Band III amplifier.
V_{CE} = 25 V; I_C = 2 × 3.25 A; T_{amb} = 23 °C; Th = 65 °C.

Fig.5 3-tone intermodulation product as function of Po sync. Vision freq. 224 MHz; sound freq 229.5 MHz.

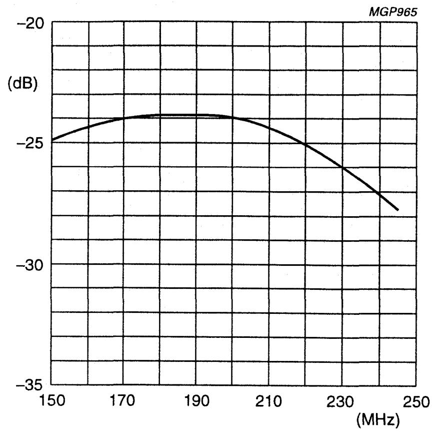


a. Forward transducer gain.

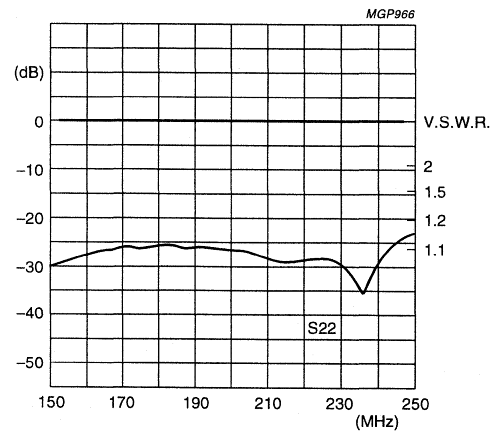


b. Input voltage standing wave ratio.

Fig.6 2× BLV33F wideband Band III power amplifier.



a. Reverse transducer gain.



b. Output voltage standing wave ratio.

Fig.7 2× BLV33F wideband power amplifier.

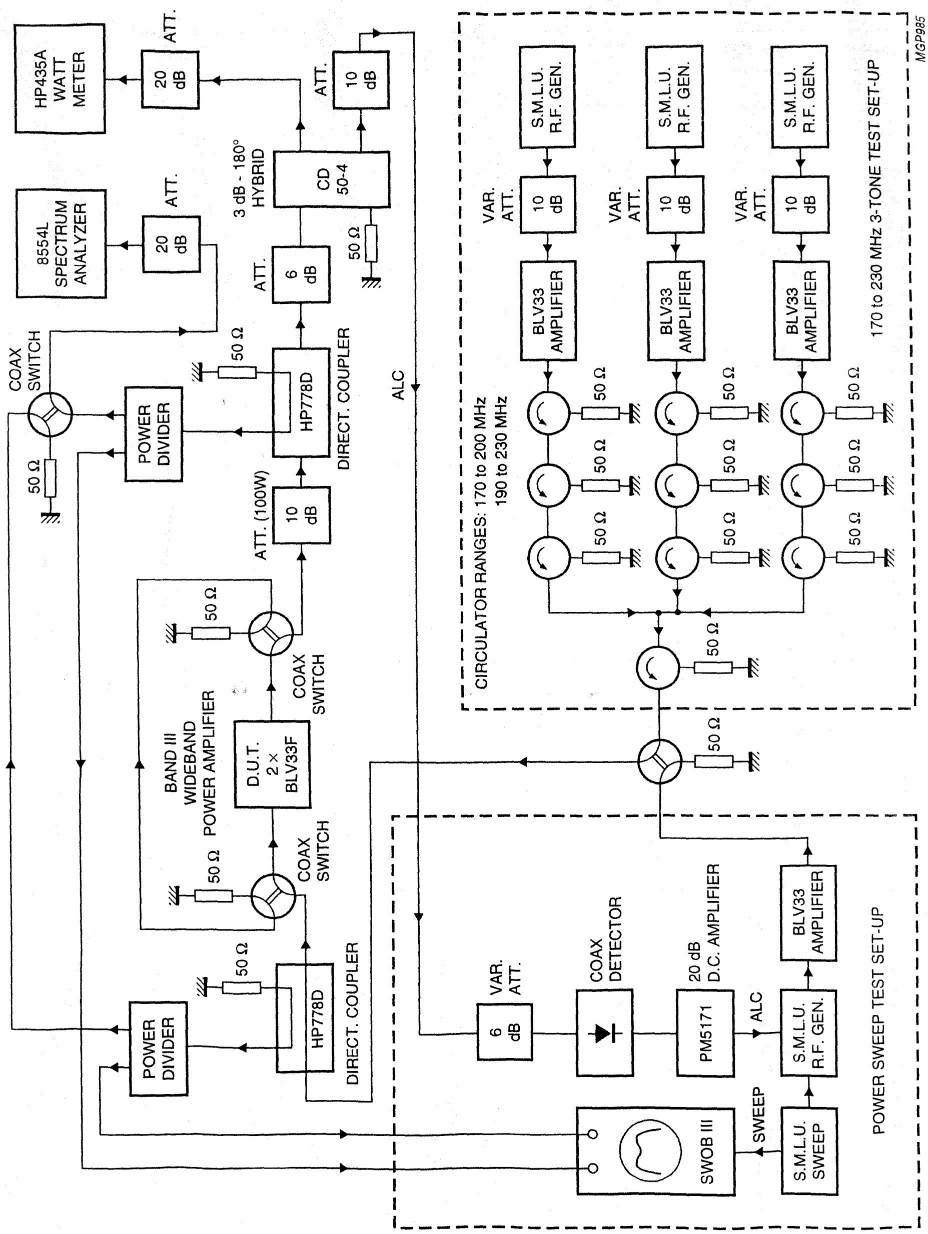


Fig.8 Test set up 2× BLV33F Band III power amplifier.

Unfortunately the numbers in the lay-out of Fig.9 do not correspond with those of the schematic diagram of Fig.1. The reader is referred to the translation Table 5.

Table 5

NUMBER IN LAY-OUT (see Fig.9)	**NUMBER OF SCHEMATIC DIAGRAM** (see Fig.1)
R1	R3
R2	R5
R3	R6
C2	C1
C3	C3
C4	C4
C5	C7
C6	C8
C7	C11
C8	C14
C9	C15
C10	C19
C11	C13
C12	C21
C13	C22
C14	C25
C15	C26
C16	C27
C17	C31
C18	C32
C19	C35
L1	L1
L3	L3
L6	L11
L9	L17

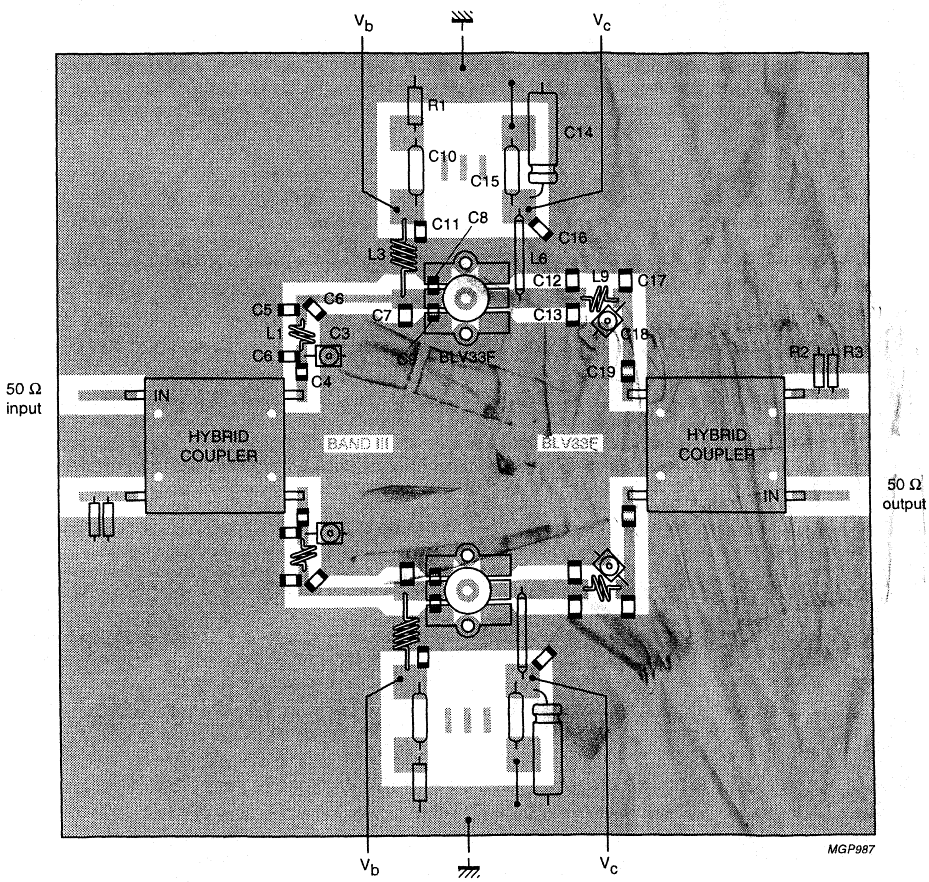


Fig.9 Lay-out of amplifier with situation of components.

1 INTRODUCTION

In this report the design procedures and measurement results are given of a two octave wideband amplifier (covering both the civil and military airbands between 100 and 450 MHz), equiped with two MOSFET devices, which is capable of generating 250 W of output power.

In order to achieve a good broadband capability one has to use devices with the output capacitance reduced to the utmost minimum. While applying PHILIPS' BLF548 MOSFETs it was possible to obtain a respectable powergain of more than 10 dB, throughout the whole band.

The BLF548 is a balanced N-channel enhancement mode vertical D-MOS transistor in a SOT262 package, especially designed for use in wideband amplifiers up to 500 MHz. The transistor is capable to deliver 150 W nominal outputpower at a supply voltage of 28 Volts. Due to the low output capacitance the attainable bandwidth will exceed 300 MHz.

2 DESIGN CONSIDERATIONS

While designing broadband amplifiers, one has to take several things into account:

- To select the right manufacturer, able to supply the products with a good reliability, gives a good support and offers a complete range of transistors e.g. for driverstages.
- To select the right active components, capable to fulfill the desired wishes, such as; high reliability, high powergain, high efficiency, excellent mismatch capabilities, right loadpower, good long-life properties and last but not least; good broadband capability.
- To terminate the transistor with the right load impedance, with other words, to determinate the right output matching network.
- To eliminate the 6 dB/octave gain slope throughout the band of operation, in order to achieve an acceptable gainflatness.
- To find the right input matching network; the input VSWR has to be low in order to achieve a good termination for the driverstage.
- To design the matching networks in such a way that they are capable to handle the, at some points very high, R.F. currents.

A balanced transistor was chosen in order to reduce the second harmonic (due to the push-pull effect) and to reduce the number of required components.

The criteria for chosen MOSFETs over bipolar transistors are; high powergain, high load mismatch capabilities, low noise and easy biasing.

Nowadays three major MOSFET suppliers are involved when Pl = 150 W is needed at f = 500 MHz and Vds = 28 V. Available are; BLF548, industry type A and industry type B. Table 1 gives an overview of the characteristics of these 3 types.

Table 1

	BLF548	TYPE A	TYPE B	UNIT
f	500	400	500	MHz
Gp	>10	>10	>8	dB
ηd	>50	>50	>55	%
Ciss	105	180	140	pF
Coss	90	200	100	pF
Crss	25	20	32	pF
BW	300	133	266	MHz

With: BW = 1/(2π * Rload * Co); Rload = Vds^2/(2 * Pl) and Co = 1.15 * Coss.

BW = bandwidth, Rload = loadresistance, Co = outputcapacitance.

In order to achieve the best possible broadband results, the BLF548 is a very good choice.

Other Philips MOSFETs in the 500 MHz series are, followed by nominal loadpower:

12.5 Volts – single ended

BLF521	2 W
BLF522	5 W

28 Volts – single ended

BLF542	5 W
BLF543	10 W
BLF544	20 W

28 Volts – push-pull

BLF544B	20 W
BLF545	40 W
BLF546	80 W
BLF547	100 W
BLF548	150 W

3 AMPLIFIER CONCEPT

The amplifier concept described in this paper is based upon two identical modular units, each containing one BLF548 MOSFET. Both units are combined by means of two 3 dB – 90° hybrid couplers, which is shown in Fig.1. The main advantage is that the input VSWR will be very good; since it is independent of the mismatch introduced by the units, the 50 Ω termination will cause a good load for the driver stage, e.g. equipped with BLF544.

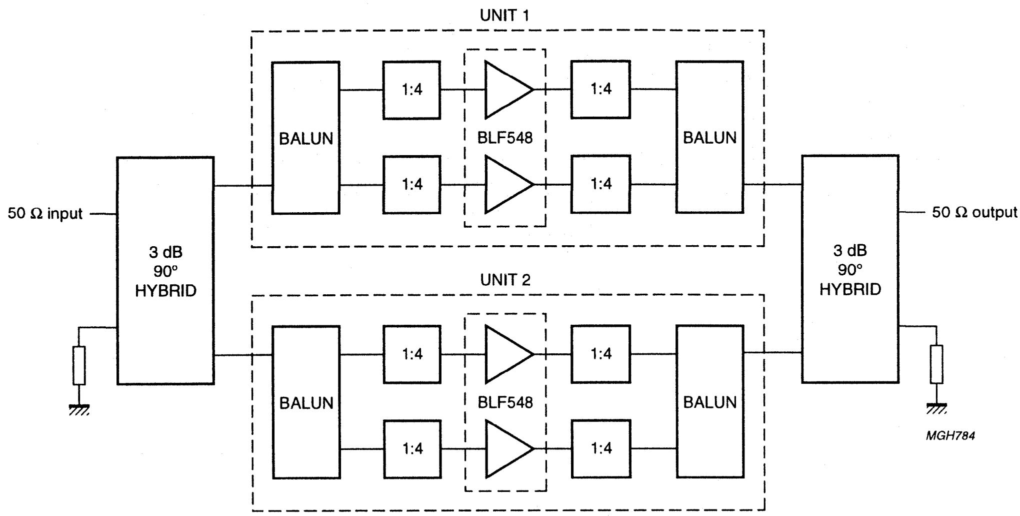


Fig.1 Schematical representation of the concept of the eventual amplifier.

The following seven steps have been followed in order to develop a first prototype of one unit.

1. Determine the BLF548's 150 W output power load impedance between 100 and 500 MHz (50 MHz interval steps) by measurement techniques or simulations. At the moment of writing it was not possible to perform full automatic measurements at frequencies lower than 500 MHz with transistors build in a balanced SOT262 header. Therefore the load impedances have been calculated by means of the electrical equivalent diagram shown in Fig.2.
2. Find the correct output matching network which transforms the 50 Ω termination to the required load impedance for the frequency range 100-500 MHz.
3. Optimize the outputmatching network of step 2 with help of linear simulation software, such as Touchstone (EESOF).
4. Since the matching network will not have an ideal behaviour, it is necessary to determine the actual load impedance of the selected output matching network, again in 50 MHz steps between 100-500 MHz.
5. Calculate (or even better, determine by means of load-pull measurements) both the powergain and input impedance of the transistor by presenting the load impedences, found at step 4, to it. This is very important to investigate the behaviour of the transistor while terminating it with the selected output matching network.
6. Choose the right input matching network which has a minimum returnloss (Rl) at the highest frequency (450 MHz) and a declining Rl for lower frequencies in a way that the gain increase effect for lower frequencies is equalized. Other possibilities, as feedback or frequency dependent damping at the gate side (by means of low Rgs), can be taken into consideration.
7. Optimize the input network for gainflatness by means of linear simulation software (Touchstone, EESOF). Remember the input VSWR throughout the band is taken care of by the use of 90° hybrids, which combine the two modular units.

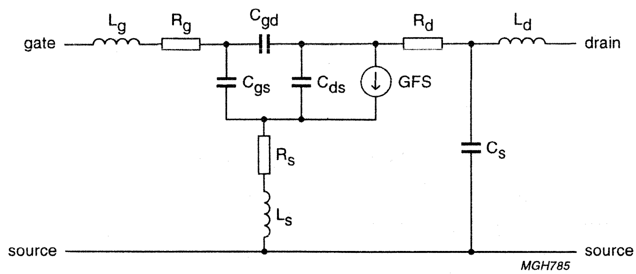


Fig.2 RF Power MOSFET equivalent diagram (one BLF548 section).

At the following pages the design steps are presented which were followed at PHILIPS' laboratories in order to design a 150 W unit. Using the diagram shown in Fig.2, powergain and impedances have been calculated first, using the data given in Table 2.

Table 2

Lg	0.58 nH	
Ls	0.11 nH	
Ld	0.50 nH	
Rg	0.09 Ω	
Rs	0.08 Ω	
Rd	0.19 Ω	
Cgd	29 pF	1.15 × Crss
Cgs	120 pF	1.5 × (Ciss-Crss)
Cds	72 pF	1.15 × (Coss-Crss-Cs)
Cs	2.4 pF	2.4 pF
Gfs'	1.6 S	0.5 × Gfs (for Class B)

Rg, Rd, Rs are derived from Rdson measurements, Gfs and Cs are measured, Cgs, Cds, Cgd derived from measured Ciss, Coss, Crss respectively. Lg, Ls and Ld are calculated.

Some of the assumptions are based on empirical rules and have proven to be correct in the past.

Gp and Zin can now be calculated:

Zin = Ri + jXi

Gp = 10 * ^{10}log (Gfs' × Rload/ω^2 × Ls × Ci)

with;
Xi = ω × Li – 1/(ω × Ci)
Ri = (Gfs' × Ls)/Ci
Li = Lq + (Ls × Cgs)/Ci
Ci = Cgs + Cgd (1 + Gfs' × Rload)
w = 2 πf

Zload is chosen for maximum broadband capability.

Table 3 Calculated powergain, Zin and required Zload (series components)

F (MHz)	PL (W)	Gp (dB)	ZIN (Ω)	ZLOAD (Ω)
100	78.8	26.7	0.43 – j4.1	4.7 + j1.5
150	78.8	23.3	0.43 – j2.5	4.0 + j1.0
200	78.8	20.8	0.42 – j1.7	3.4 + j2.0
250	78.8	18.4	0.43 – j1.1	2.8 + j1.9
300	78.8	17.2	0.43 – j0.7	2.3 + j1.7
350	78.8	15.8	0.43 – j.0.3	1.9 + j1.4
400	78.8	14.5	0.44 – j0.0	1.6 + j1.1
450	78.8	13.4	0.44 + j0.2	1.3 + j0.7
500	78.8	12.4	0.45 + j0.5	1.1 + j0.4

The data is also given in datahandbook *"RF power MOS transistors"* – Philips Components. It can be noticed that without any gaincompensation the powergain difference between 100 and 500 MHz will exceed 10 dB.

To terminate the transistor with the required loadimpedance, with respect to the broadband capability, the unbalanced 50 Ω load has to be transformed as close as possible to the loadimpedance as shown in Table 3. (Note: the impedances shown are based on one section, since the transistor is of a balanced type, Zin and Zload are related to virtual ground).

To reduce the number of components which would be needed in case of a lumped element solution, a coaxial semi-rigid balun is used to transform the unbalanced 50 Ω load into two 25 Ω sections that are 180° apart in phase and 90° away from virtual ground. This is followed by a coaxial 4 : 1 transformer, with a characteristic impedance of 25 Ω.

The result of this is: Rp = ($\sqrt{}$25 × 25)/4 = 6.2 Ω, which is close to the required Rload of the transistor.

In order to give a good description of the outputnetwork, it will be described as a 3-port: one port terminated with 50 Ω unbalanced, the other two terminated with the transistor's outputimpedance (the complex conjugate of loadimpedance). A computer listing of the outputnetwork is given in "Appendix A". After optimizing the network to minimum returnloss (S11), while checking S13, the optimized return loss (in dB) of this network has been determined, see Fig.3. As a next step now the difference between the required and the network related loadimpedance can be (re-) calculated. The result on powergain (Gp) and imputimpedance (Zin) is given in Table 4.

Table 4 Result on Zin and Gp as a result of the presented outputmatching network

F (MHz)	PL (W)	Gp (dB)	ZIN (Ω)	ZLOAD (Ω)
100	78.6	32.7	0.11 – j4.1	4.3 + j1.0
150	78.8	19.7	1.04 – j2.9	4.1 + j0.2
200	78.8	17.3	1.02 – j2.2	3.3 + j0.1
250	78.8	16.0	0.87 – j1.5	2.9 + j0.1
300	78.8	14.9	0.79 – j0.9	2.8 + j0.3
350	78.8	13.5	0.80 – j.0.4	2.8 + j0.4
400	78.8	12.4	0.79 – j0.1	2.5 + j0.2
450	78.8	12.0	0.67 + j0.1	1.9 + j0.1
500	72.0	12.4	0.43 + j0.5	1.1 + j0.6

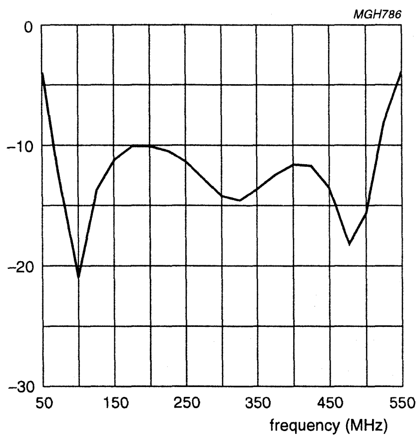


Fig.3 Simulated network response (output side).

4 INPUT CIRCUITRY

Since Zin and Gp are now determined in a accurate way, the inputcircuitry can be determined. Special attention is given to the flatness of the gain as a function of frequency. The input network also consists of a coaxial balum, followed by a 1 : 4 coaxial transformer, both made of semi-rigid coaxial cable. Since Zin is rather low the characteristic impedance of the 1 : 4 transformer was chosen to be 10 Ω.

The result of this is: Rp = ($\sqrt{25} \times 10$)/4 = 3.9 Ω.

In order to compensate for the 6 dB/octave slope, matching to Zin is achieved at 450 MHz. At lower frequencies a mismatch is created, resulting in a decrease of powergain inversely proportional to the increase of the gain related to the transistor's 6 dB/octave slope.

The network listing of the input circuitry, again presented as a 3-port, is given in "Appendix B". The network response (both input returnloss and predicted powergain) is given in Fig.4. Finally the schematic diagram and list of components are given in Fig.5. The unit's layout is given in Fig.6. Note: two toroidal cores around T2 and T3 are used to prevent oscillations.

5 ADJUSTMENT OF THE AMPLIFIER

5.1 Tuning the outputnetwork

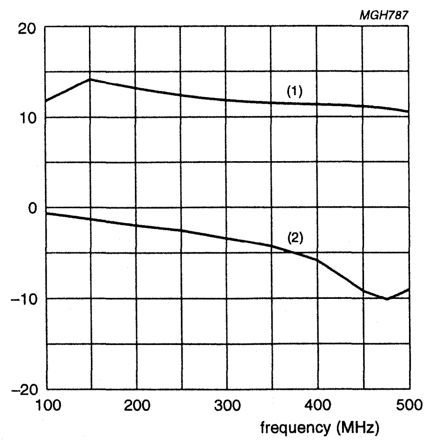
In order to terminate the transistor with the proper load impedance, first the output network has to be tuned.

The transistor was replaced by a dummyload, representing the transistors output impedance under full power conditions. The dummyload was realized after fitting the data of Table 3. To the dummyload model (roughly Rload in parallel with Coss, in series with draininductance Ld). Later the model was compensated for parasitics of both SOT262 header and network components.

Initial settings for each side of the dummyload are:

$Rload = Vds^2/2 \times Pl = 5.2\ \Omega$
$C = 1.15 \times Coss = 104$ pF
$L = Ld = 0.5$ nH

The network listing is given in "Appendix C". The final result, the dummyload lay-out, is given in Fig.7.



(1) DB [S12].
(2) DB [S22].

Fig.4 Simulated network response of inputside (predicted Gp = f(f)).

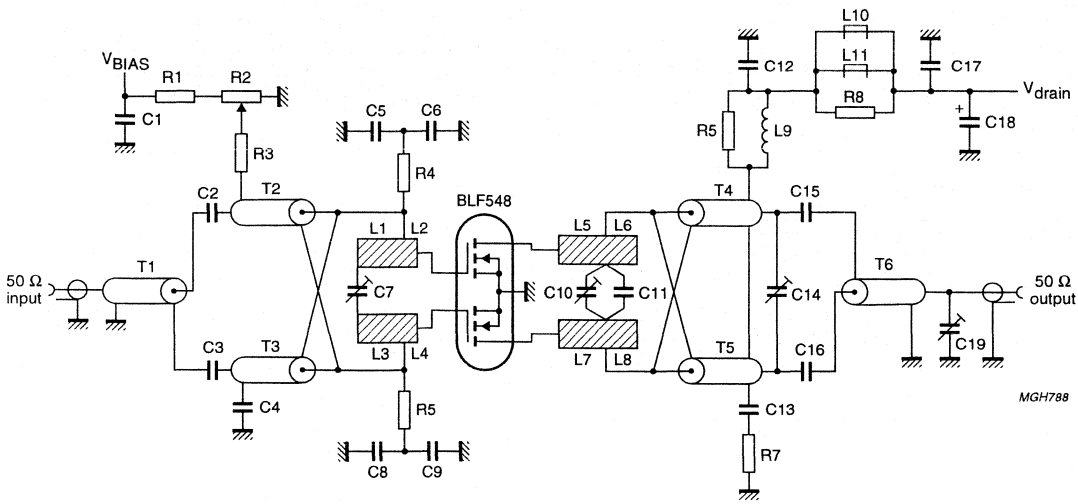


Fig.5 Schematical diagram and list of components of one unit.

List of components

DESIGNATION	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C17	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C2, C3	multilayer ceramic chip capacitor (note 1)	47 pF		
C4, C5, C8	multilayer ceramic chip capacitor (note 1)	820 pF		
C6, C9	multilayer ceramic chip capacitor (note 1)	300 pF		
C7	film dielectric trimmer	2-18 pF		2222 809 09006
C10, C14	film dielectric trimmer	2-9 pF		2222 809 09005
C11	multilayer ceramic chip capacitor (note 2)	39 pF		
C12	capacitor	22 nF		
C13	capacitor	100 nF		
C15, C16	multilayer ceramic chip capacitor (note 1)	120 pF		
C18	63 V electorlytic capacitor	1 μF		2222 685 78108
C19	film dielectric trimmer	1-5 pF		222 808 09004
L1, L3	stripline (note 3)	20 Ω	5 × 8 mm	
L2, L4	stripline (note 3)	20 Ω	2.5 × 8 mm	
L5, L7	stripline (note 3)	20 Ω	11.5 × 8 mm	
L6, L8	stripline (note 3)	20 Ω	4 × 8 mm	
L9	5 turns enamelled Cu wire on R6		1.4 mm	
L10, L11	grade 3B Ferroxcube wideband RF choke			4330 030 36642
T1	semi-rigid coax (note 4)	50 Ω	length 54 mm	
T2, T3	semi-rigid coax (note 4)	10 Ω	length 44 mm	
T4, T5	semi-rigid coax	25 Ω	length 53 mm	
T6	semi-rigid coax	50 Ω	length 74 mm	
R1	0.4 W metal film resistor	19.6 kΩ		2322 151 11963
R2	10 turn potentiometer	5 kΩ		2122 362 00725
R3, R4, R5	0.4 W metal film resistor	2.05 kΩ		2322 151 12052
R6, R7, R8	1.0 W metal film resistor	10 Ω		2322 153 71009

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. American Technical Ceramics type 175B or capacitor of same quality.
3. The striplines are on a double copper-clad PCB with P.T.F.E. fibre-glass dielectric ($\varepsilon_r = 2.2$); thickness 1/32 inch.
4. T2 and T3 are equipped with a Toroidal core, grade 4C6 (cat.no. 4322 020 97171).

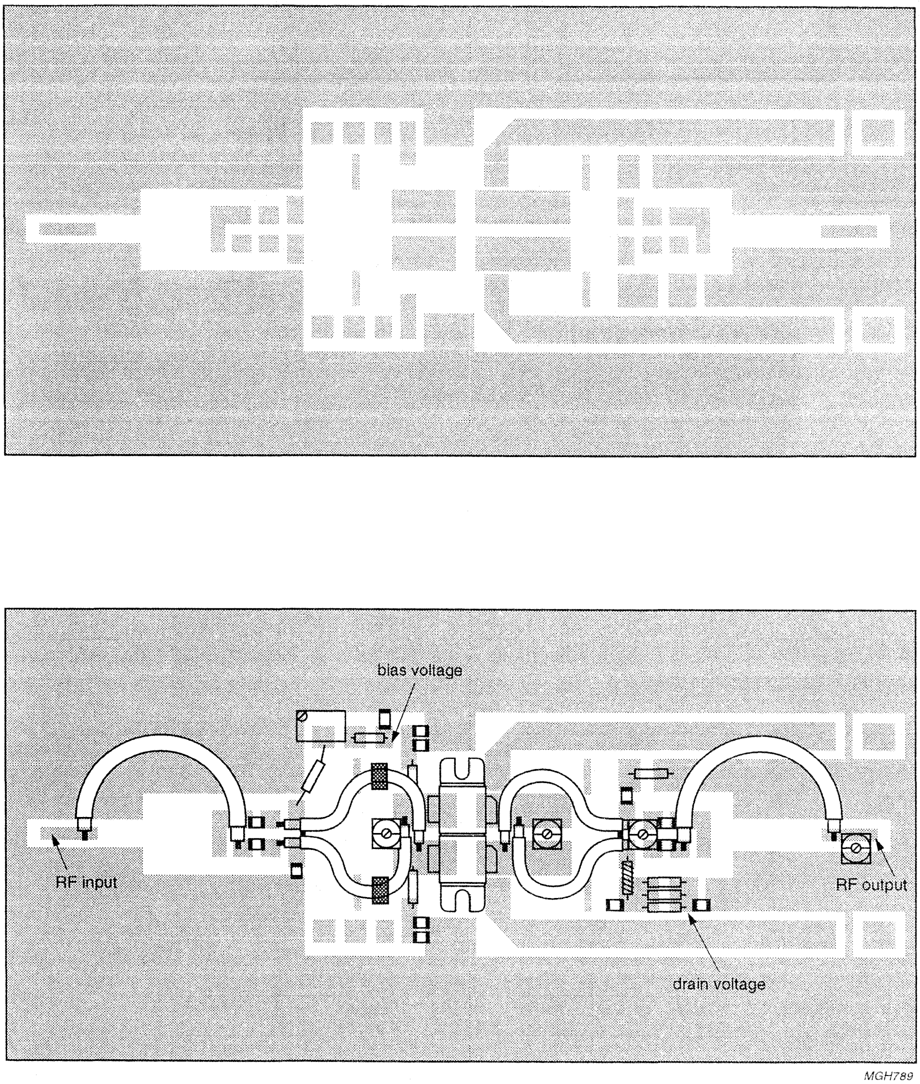


Fig.6 Lay-out of one unit.

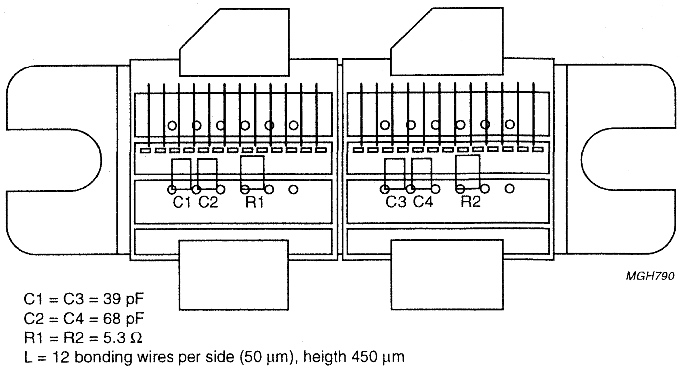


Fig.7 Lay-out of BLF548 dummyload.

By means of a RF-analyzer the predicted frequency response of the network can be reproduced in practice, while tuning C10 and C14 for optimum R1. This is presented in Fig.8. A comparison with the simulated networkresponse (Fig.3) shows a high amount of common behaviour.

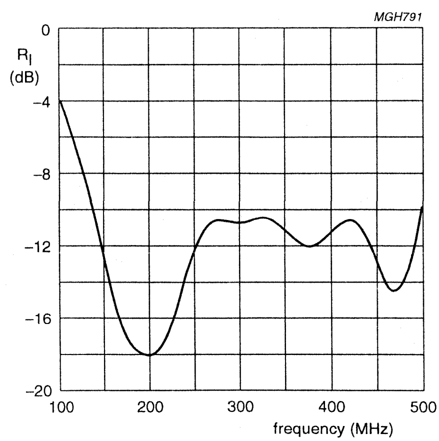


Fig.8 Measured network response of one unit after tuning C10 and C14.

5.2 Testing the unit under RF conditions

After exchanging the dummyload for a BLF548, a frequencysweep under power conditions can be made with help of a network analyzer. The used measurement set-up is given in Fig.9.

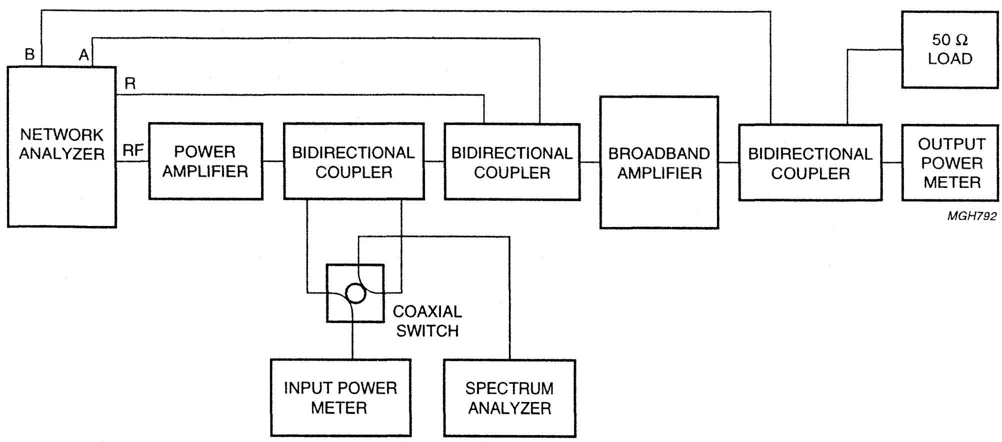
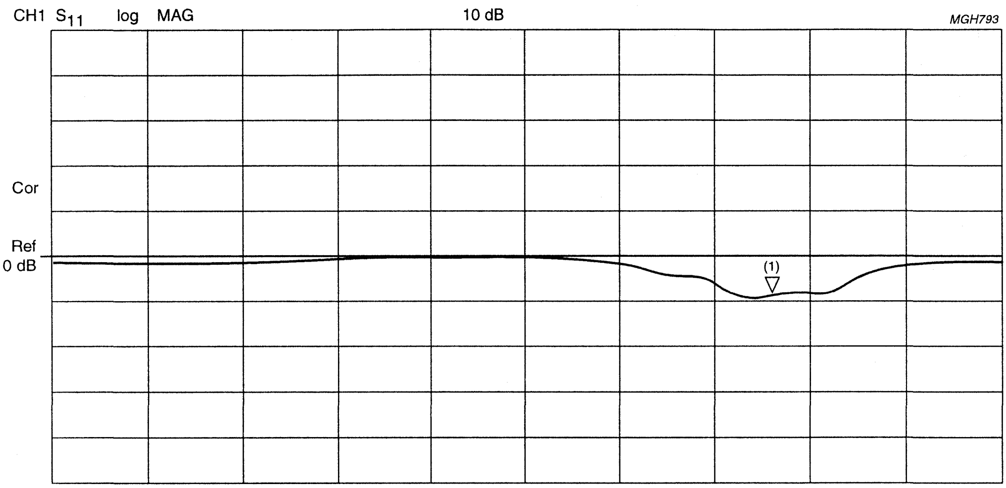


Fig.9 Measurement set-up for frequency sweep under powerconditions.

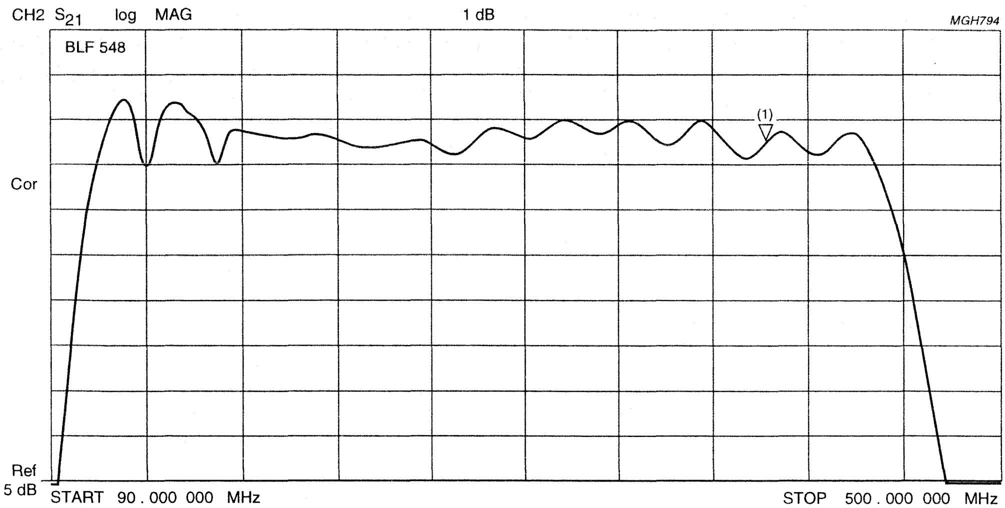
5.3 Tuning the unit's inputnetwork

After supplying both the bias- and drain voltages to the unit and adjusting the drain quiescent current with R2 to 320 mA (160 mA per side), the inputpower (Ps) is applied. Gainflatness is optimized while tuning C7. The unit's input returnloss is given in Fig.10. Pl versus frequency is shown in Fig.11. A comparison with the simulated network response of the inputside (Fig.4) shows a high similarity. Gainflatness within 1 dB is achieved between 100 and 450 MHz.



(1) 400 MHz; –8.3 dB.

Fig.10 Input return loss of one unit (Frequency sweep at Pl = 150 W, for f = 90 to 500 MHz.

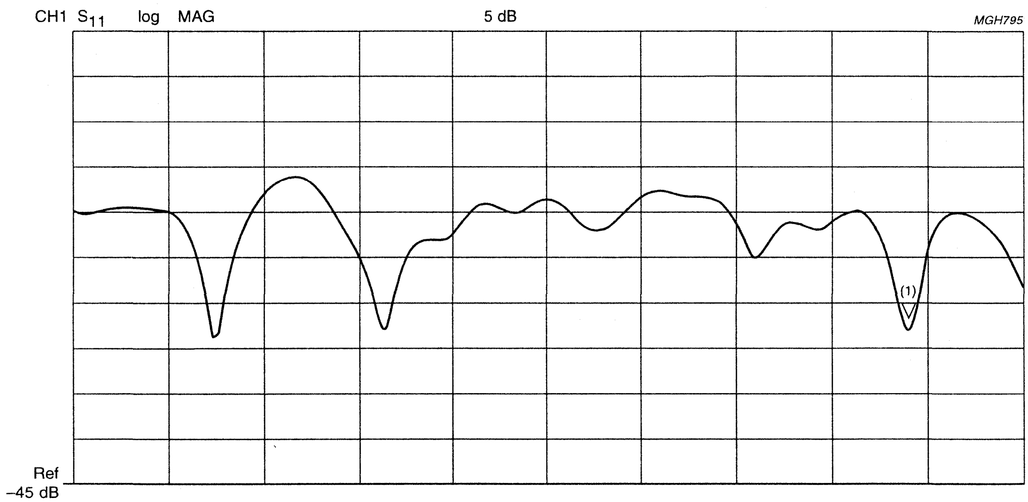


(1) 400 MHz; 12.526 dB.

Fig.11 Powergain of one unit (Frequency sweep at Pl = 150 W, for f = 90 to 500 MHz).

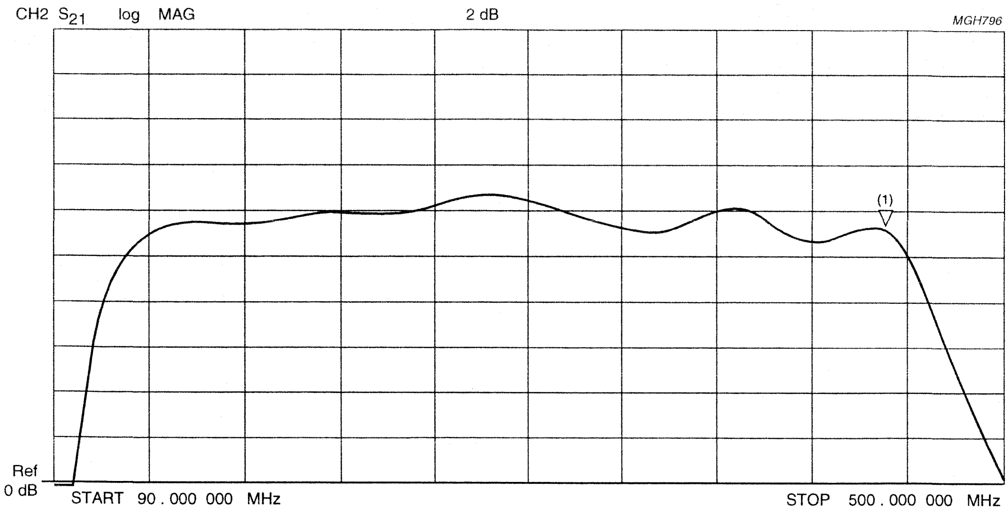
5.4 Combining the units

After tuning the second unit similar as described above, the connection was made to the 90° hybrid couplers. The couplers do contain 4 ports, one at which the input signal is applied (1). The input is devided equally into two ports (3 and 4). Between ports 3 and 4 there is a voltage lag of 90°. Mismatch at ports 3 and 4 do not effect the VSWR of port 1, since port 2 is terminated with a 50 Ω load (KDI-PPT820-75-3 flange mounted). At the output side of the amplifier the units are combined in a similar way. Both input and output hybrids and 50 Ω loads are mounted in a Brass baseplate (dimensions; 200 × 160 × 10 mm), which also serves as a heatspreader for both BLF548 devices. The baseplate is connected to a heatsink which is cooled by means of forced air. Final results are given in Fig.12. (input return loss of the amplifier) and Fig.13 (the amplifier's powergain).



(1) 450 MHz; –28.1 dB.

Fig.12 Input return loss of complete amplifier (Frequency sweep at Pl = 250 W, for f = 90 to 500 MHz).



(1) 450 MHz; 11.1 dB.

Fig.13 Powergain of complete amplifier (Frequency sweep at PI = 250 W, for f = 90 to 500 MHz).

6 CONCLUSIONS

The described procedures shown in this paper, are a great help in designing high-power broadband amplifiers. The differences between theory and practice are relatively small.

The BLF548 is very well suited to perform in multi-octave broadband UHF-amplifiers; at a supply voltage of 28 V, between 100 and 450 MHz, 250 W of outputpower could be generated with a powergain of 11 dB (gainripple smaller than 1 dB). Drainefficiency is 45 to 55% throughout the band. The reduction of the second harmonic is more than 25 dB, with respect to the fundamental. The input returnloss is better than –12 dB.

7 REFERENCES

- Data Handbook SC08b, RF power MOS transistors – Philips Components
- Application Report Bipolar & MOS transmitting transistors – Philips Components
- A look inside those integrated two-chip amps – Joe Johnson – Microwaves feb. 1980
- Apply wideband techniques to balanced amplifiers – Lee B. Max – Microwaves apr. 1980
- Demystifying new generation silicon high power FETs – Steve McIntyre – Microwave Journal apr. 1984
- Anaren – Microwave components catalog no.17A.

8 APPENDIX A

DIM

FREQ	MHz
RES	OH
IND	NH
CAP	PF
LNG	MM

VAR

C1 = 120	!c = 270
L2 = 74	!50
L3 = 53	!50
L10 = 9	!9
L11 = 0.350559	!0.5
R11 = 4.191123	!5.1
C11 = 64.2821 4	!75
L12 = 0.409981	!0.31
W1 = 6	
L22 = 10	
L33 = 66	

CKT

RES	1 0	R = 50	
DEFIP	1	REFIMP	
S1PA	2 0	BLF548OU	
DEF1P	2	BALI	
IND	1 2	L^L11	
RES	2 0	R^R11	
SLC	2 0	L^L12; C^C11	!to determine zload
DEFIP	1	BAL3	
SLC	1 0	L = 0.5 C = 4 !13.5	
COAX	1 2 0 3	DI = 0.91; DO = 2.98; L^L3; ER = 2.03	TAND = 0.0002; RHO = 1
MSUB	ER = 2.2; H = 0.79	T = 0.035	RHO = 0.72; RGH = 1
SLC	2 4	L = 0.5; C^cl	
SLC	3 5	L = 0.5; C^cl	
COAX	4 6 0 8	DI = 1.63	DO = 2.95; L^L2 ER = 2.03; TAND = 0.0002; RHO = 1
COAX	5 8 0 6	DI = 1.63	DO = 2.95; L^L2; ER = 2.03; TAND = 0.0002; RHO = 1
SLC	6 8	L = 0.5; C = 41	!C = 41
SLC	6 8	L = 0.7; C = 8	!C = 0
MLIN	919	w^w1; 1^122	
MLIN	10 20	w^w1; 1^122	
MBEND3	19 29	w^w1	
MBEND3	20 30	w^w1	
MLIN	29 0	w^w1; 1^133	
MLIN	30 0	w^w1; 1^133	
MCLIN	6 8 9 10	W = 8; S = 2.5; L = 12	!L = 13
SLC	9 10	L = 0.5; C = 3	!C = 5
DEF3P	1 9 10	TRAFO	!OUTPUT NETWORK
BAL2	2 0		
TRAFO	3 1 2 0		
DEF2P	1 3	IMP2	
BAL1	1 0		
BAL1	2 0		
TRAFO	3 1 2 0		
DEFIP	3	IMP	

FREQ

SWEEP	50 550 25	
OUT		
IMP RE(Z1)		
IMP IM(Z1)		
IMP DB(S11)	GR1	
IMP S11 SC2		
!IMP VSWR1		
BAL3 RE(Z1)		!TO DETERMIN E
BAL3 IM(Z1)		!ZLOAD
IMP2 DB(S12)		

GRID

RANGE	50 550 50
GR1	–30 0 5

TERM

IMP2	BAL1 REFIMP	!50 Ω PORT1

OPT

RANGE	50 550
!IMP	VSWR1 < 1.6
IMP	MODEL REFIMP

Note

1. Slp file BLF5480U does contain data given in “Appendix C”.

9 APPENDIX B

Input BLF548 application (300 W/28 V/500 MHz); input in 1P file fit between 100 – 500 MHz with 1 : 4 transformer (Zc = 10 Ω) to determine Gp and inputVSWR ZiN and Gp data derived from calculations, which represent the performance of the device after applying the output NEtwork, given in "Appendix A" to IT.

Table 5

DIM			
FREQ	MHz		
RES	OH		
IND	NH		
CAP	PF		
LNG	MM		
VAR			
C1\57.83880	!C = 27		
L2\64.28568	!L = 25		
L3 = 55	!L = 25		
R11 = 0.00020 7	!4.1		
C11 = 241.805 9	!65		
L12 = 0.00004 8	!0.41		
CKT			
RES	1 0	R = 50	
DEF1P	1	REFIMP	!50 Ω LOAD
S1PA	2 0	BLF54812	
DEF1P	2	BAL1	!BLF548's Zin
RES	1 2	R^R11	
SLC	2 0	L^L12; C^C11	
DEF1P	1	BAL3	
GAIN	1 2	A = 22.65; S = –4.79; F = 150	!Gp DATA DERIVED FROM
GAIN	2 3	A = 0; S = 0.5; F = 350	!Table 3
GAIN	3 4	A = 0; S = 1.5; F = 400	!13 dB GAINCORRE CTION SINCE
DEF2P	1 3	GPAF	!2 SECTIONS ARE INVOLVED
SLC	1 0	L = 0.5; C\0.016169 !2	
COAX	1 2 0 3	DI = 0.91; DO = 2.98	L^L3; ER = 2.03; TAND = 0.000 2; RHO = 1
MSUB		ER = 2.2; H = 0.79; T = 0.035; RHO = 0.72; RHG = 1	
SLC	2 4	L = 0.5 C^cl	
SLC	3 5	L = 0.5 C^cl	
COAX	4 6 7 8	DI = 1.15; DO = 1.45; L^L2; ER = 2.03; TAND = 0.0002	RHO = 1
COAX	5 8 7 6	DI = 1.15; DO = 1.45; L^L2; ER = 2.03; TAND = 0.0002	RHO = 1
UNIT	7 0		
SLC	6 8	L = 0.5; C\0.103064 IC – 2.1	
MCLIN	6 8 9 10	W = 8; S = 2.5; L\3.05628 0	
SLC	9 10	L = 0.5; C\0.923788; !c – 3.5	
DEF3P	1 9 10	TRAFO	INPUT NETWORK
BALI	2 0		
TRAFO	3 5 4 0		
GPAF	4 2		
GPAF	5 1		
DEF2P	1 3	IMP2	!TO DETERMINE S11, S12
FREQ			
SWEEP	100 500 25		
OUT			
IMP2 TE(Z2)			
IMP2 IM(Z2)			
IMP2 DB(S22)	GR1	!S11 AT 50 Ω PORT	
IMP2 DB(S12)	GR1	!CALCULATED POWERGAIN	
IMP2 VSWR2			
GPAF DB(S21)		!BLF548's GP	
GRID			
RANGE	100 500 25		
GRI	–20 20 5		
TERM			
IMP2 BAL1 REFIMP			
OPT			
RANGE	150 550		
IMP2 DB(S12) > 11			
IMP2 DB(S12) < 12.4			

Note

1. S1p file BLF548I2 does contain data given in Table 4. Format as shown in "Appendix C".

10 APPENDIX C

Fit dummyloadmodel to calculated BLF548 Zoutput !FIlename: E:\users\blf548ou.s1p
!reference: calculated data derived from transmod program;!Zload converted to Zoutput

DIM				
FREQ	GHZ			
RES	OH			
IND	NH			
CAP	PF			
LNG	MM			
CKT				
MSUB	ER = 6.5	H = 1.02; T = 0.035 ; RHO = 1; RGH = 0		
IND	1 0	L = 0.168		!inductance to ground
RES	1 2	R = 5.28 0		
SLC	1 2	L = 0.3	C = 40	
SLC	1 2	L = 0.3	C\65.8	
CAP	2 0	C = 1		
IND	2 3	L = 0.165		!bonding wires at drainside
MLIN	3 4	W = 10.8	L = 1.6	!metallization of header
DEF1p	4	MOD		!1-port of dummyload
S1PA	1 0	BLF5480 U.s1p		!calculated z-parameters of
DEF1p	1	MES		!BLF548 outputimpedances
FREQ				
SWEEP	0.1	0.5	.050	
OUT				
MOD	RE(Z1)			
MOD	IM(Z1)			
MES	RE(Z1)			
MES	IM(Z1)			
OPT				
MOD MODEL	MES			

Table 6

# GHz Z	RI	R 1			
0.050	5.26	−0.86	! freq	R1	X1
0.075	5.04	−1.22			
0.100	4.73	−1.51			
0.125	4.39	−1.73			
0.150	4.04	−1.87			
0.175	3.70	−1.94			
0.200	3.36	−1.95			
0.225	3.05	−1.92			
0.250	2.76	−1.85			
0.275	2.50	−1.75			
0.300	2.27	−1.63			
0.325	2.06	−1.50			
0.350	1.87	−1.35			
0.375	1.71	−1.21			
0.400	1.56	−1.05			
0.425	1.43	−0.90			
0.450	1.31	−0.74			
0.475	1.21	−0.59			
0.500	1.11	−0.43			
0.525	1.03	−0.28			
0.550	0.95	−0.13			

Note

1. Zload is derived from data given in Fig.3.

BLV859 UHF linear push-pull power transistor

Application Note AN98013

1 ABSTRACT

A broadband linear amplifier design is presented, suitable for application in TV transposers operating in band IV and V (470 to 860 MHz). The design is based on two BLV859 bipolar transistorscombined with quadrature hybrids. Typical results at the recommended class-A bias point (25.5 V/9.1 A) for the total module include 40 W peak sync output power at –54 dB three tone IMD level (fvision = –8 dB, fsound = –10 dB, fsideband = –16 dB) and an average gain of 10.5 dB in the (470 to 860) MHz range.

2 INTRODUCTION

The BLV859 is a bipolar linear push-pull power transistor designed to operate in the 460 to 860 MHz range. With a specified output power of 20 W peak-sync in class-A it is the largest device in the new generation of transposer transistors. The intermodulation distortion level is < –54 dB (fvision = –8 dB, fsound = –10 dB, fsideband = –16 dB) and power gain >10 dB at 860 MHz.

For application in TV transposers for Band IV/V (470 to 860 MHz) a wideband linear power amplifier has been designed with two BLV859 transistors in class-A.

2.1 Amplifier Electrical design objectives

The amplifier operates at a supply voltage of 25.5 V and a total current Ic = 9.1 A (2 × 4.55 A).

Electrical characteristics (Ths = 25 °C, 25.5 V, 9.1 A, 470 to 860 MHz bandwidth)

	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power gain (small signal)	Gp	9.5	–	–	dB
Gain ripple (small signal)	Griple	–	–	±1	dB
Output Power @ 1 dB compression	Pout	60	–	–	W
Intermodulation: (–8 dB/–7 dB/–16 dB, Pref = 40 W)	IMD1	–	–	–50	dB
Intermodulation: (–8 dB/–10 dB/–16 dB, Pref = 40 W)	IMD2	–	–	–53	dB
Input return loss/Output return loss	IRL/ORL	–	–	–15	dB

3 DESIGN OF THE AMPLIFIER

The amplifier consists of 2 balanced circuits, both equipped with a BLV859 and coupled in parallel by means of a wideband 3 dB –90 degree sagewireline coupler at the input and output.

3.1 Mounting the transistors

For good thermal contact, heatsink compound should used when mounting the transistors on a heatsink.

3.2 Balun

Both input and output matching circuits of each BLV859 are connected to a coax BALUN which splits a 50 Ω unbalanced port in two 12.5 Ω ports. The BALUN has a transformation factor of 2.

The construction of the BALUN is described in Fig.4.

Essential for the BALUN is the shortcircuit between the inner and outerlead as can be seen in Figs 1 and 2.

3.3 Bias circuit

Each transistor has its own bias unit to obtain a stable DC setting. With the potentiometers P1 and P2 it's possible to adjust the collector current of both BLV859 transistors. The nominal collector current should be 4.55 A.

The sense resistor in the collector branch is implemented as a folded printed line (L17). In this way we obtain a small sense resistor (approximately 80 m/Ω) that can handle the dissipated power.

3.4 Positioning of the matching capacitors

Figure 2 gives the component layout of the BLV859 amplifier.

Input:
The capacitors (C30, C35, C32 and C39) are situated on a distance of approximately 1 mm from the transistor.
The capacitors (C26, C34, C28 and C38) are situated on a distance of approximately 0.5 mm from the balun.
The position of these capacitors influences the tuning for flat gain.
Output:
The capacitors (C27, C37, C28 and C41) are situated as close as possible to the Balun.
The position of capacitors (C31, C36, C33 and C40) is critical to obtain the S22 contours as described in the amplifier tuning procedure.

Figure 3 gives the dimensions of the BLV859 amplifier printed-circuit board and Fig.5 gives the printed-circuit board layout of the frontside and backside.

3.5 Amplifier tuning procedure

Both amplifiers are separately tuned under small signal conditions by means of a networkanalyzer. The amplifiers are tuned for flat gain over the complete bandwidth (470 to 860 MHz). To obtain a flat gain the input is gradually mismatch. The input returnloss S11 is the main parameter for setting the gain level and flatness.

Tuning of the output will mainly influence IMD and to a lesser extent the gain flatness. To obtain a good IMD performance over the band it's recommended to follow the S22 tuning contours as plotted in Figs 6 to 9. A minimal S22 is required between 700 and 800 MHz (better then −25 dB). (The markers are positioned at 470 MHz (marker 1), 636 MHz (marker 2), 860 MHz (marker 3)). An S22 of −15 to −20 dB is required at the highest frequency (860 MHz) and at midfrequency (636 MHz). An S22 of −12 to −15 dB is required at the lowest frequency (470 MHz).

After individual tuning, both amplifiers can be coupled and the load resistors can be attached. The module is now ready for use and the complete characterization can be started. Figures 10 to 13 show the small signal characterization of the complete module.

4 AMPLIFIER PERFORMANCE

Broadband measurement data are presented in graphs of Figs 14 to 18, IMD and powergain are given at two 3-tone systems, (fv = −8 dB/fsb = −16 dB/fs = −10 dB) and (fv = −8 dB/fsb = −16 dB/fs = −7 dB), over the complete frequency range (470 MHz to 860 MHz).

IMD and powergain are given at two 3-tone systems, (fv = −8 dB/fsb = −16 dB/fs = −10 dB) and (fv = −8 dB/fsb = −16 dB/fs = −7 dB), versus P0_sync at the highest channel (Ch69).

At the nominal Po_sync level of 40 W for which the module is dimensioned the full band performance is as follow:

3 tones (−8/−16/−7) dB: IMD ≤ −50 dB/powergain ≥9.5 dB

3 tones (−8/−16/−10) dB: IMD ≤ −54 dB/powergain ≥9.5 dB

When coupling the amplifiers a degradation in powergain and IMD can be expected. Reasons for this are the amplitude and phase imbalances in the couplers and transistors. Also detuning of the loads of both transistors due to non-perfect 50 Ω coupler parts. At the highest frequency (ch69) only a slight degration in gain and IMD has been noted, in the order of some tents of a dB in Gain and 0.5 dB in IMD. At lower frequencies the degradation can be more or less pronounced. In all cases the IMD and gain will fullfill the minimal requirements (IMD ≤ −53 dB (−8/−16/−10 dB) and a small signal gain ≥9.5 dB) over the band.

5 CONCLUSION

A complete transposer module is presented base on 2 × BLV859, capable of operating in full band IV/V with flat gain and good linearity. Design and tuning procedures described result in a good broadband behavior. High gain ≥9.5 dB and good linearity (Po_sync ≥40 W @ –53 dB (–8/–16/–10) dB has been obtained at the class-A bias point (25 V/9.1 A).

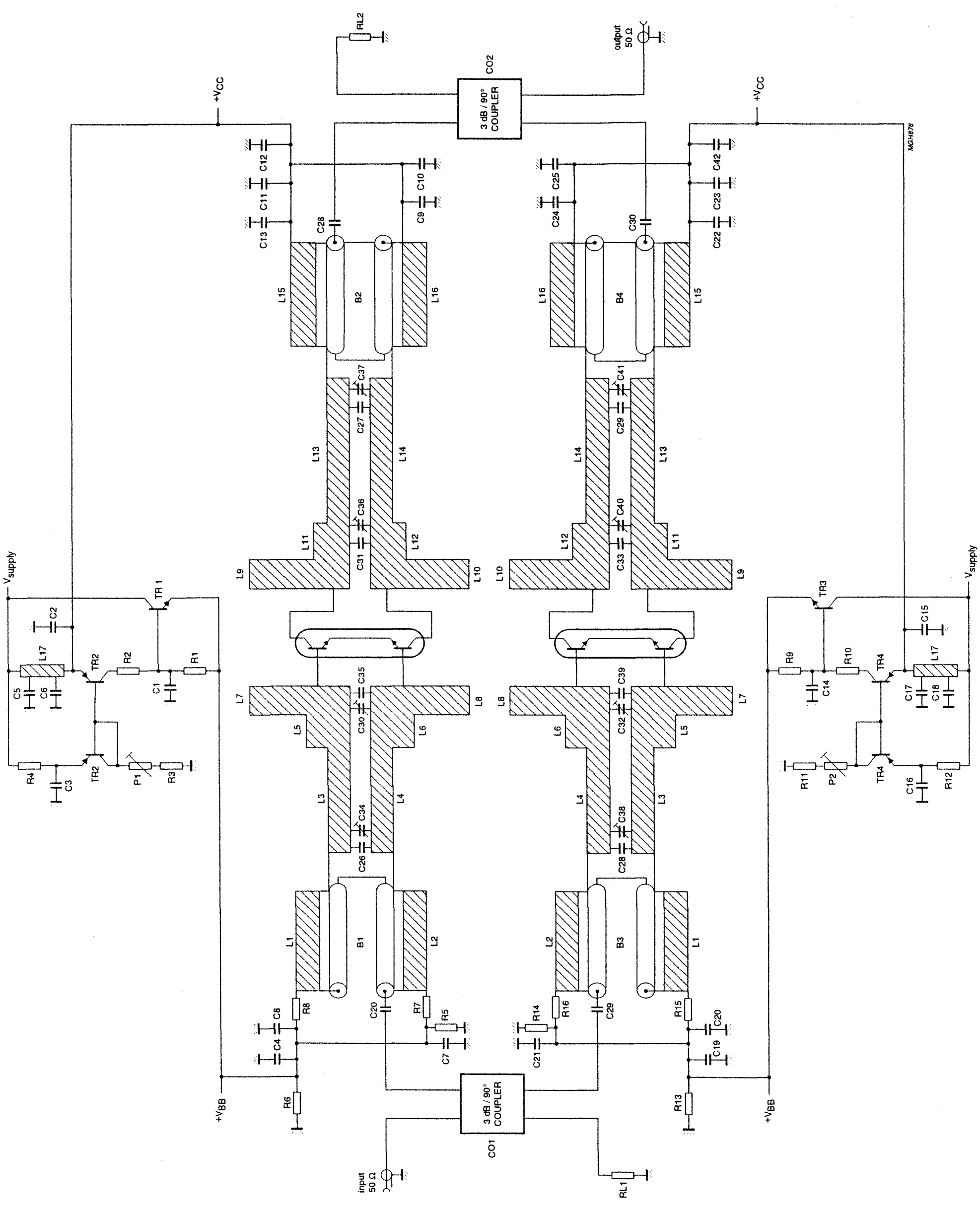


Fig.1 Schematic diagram of the BLV859 amplifier.

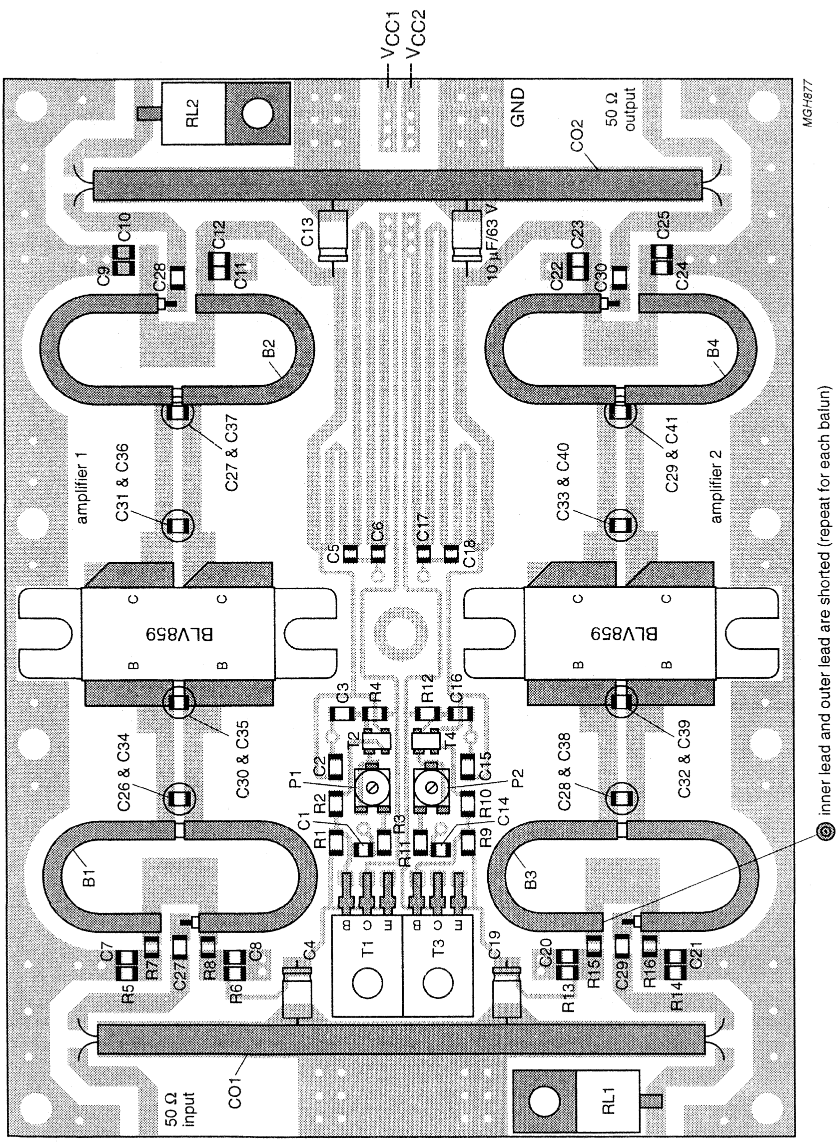


Fig.2 Component layout of the BLV859 amplifier.

See Section 6.

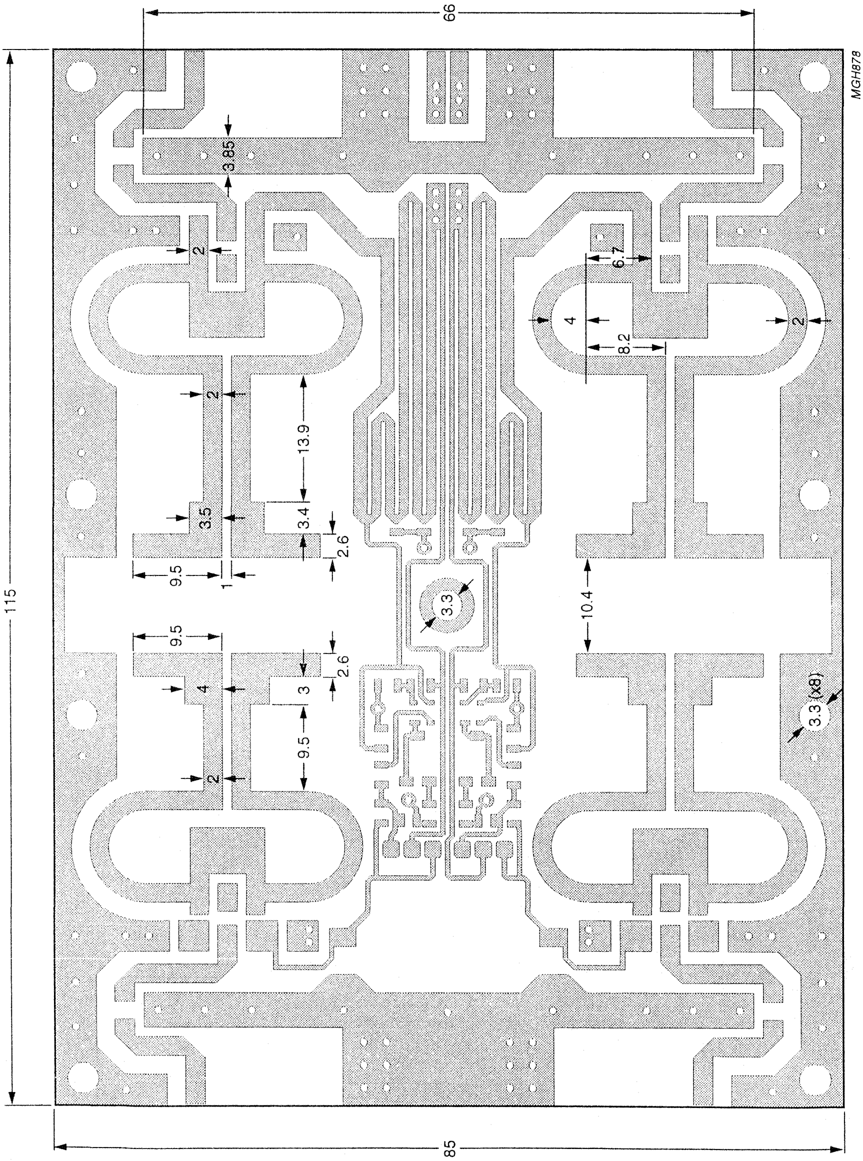


Fig.3 Printed-circuit board Dimension of the BLV859 amplifier.

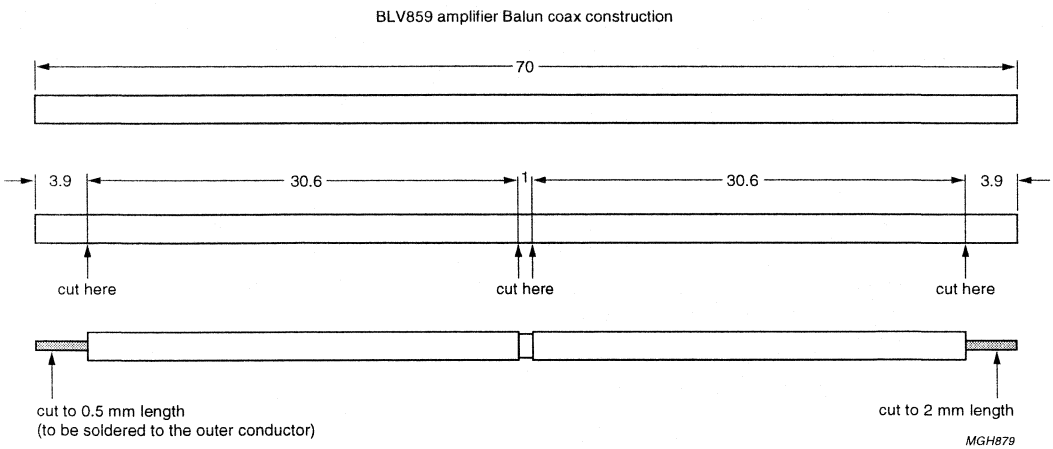
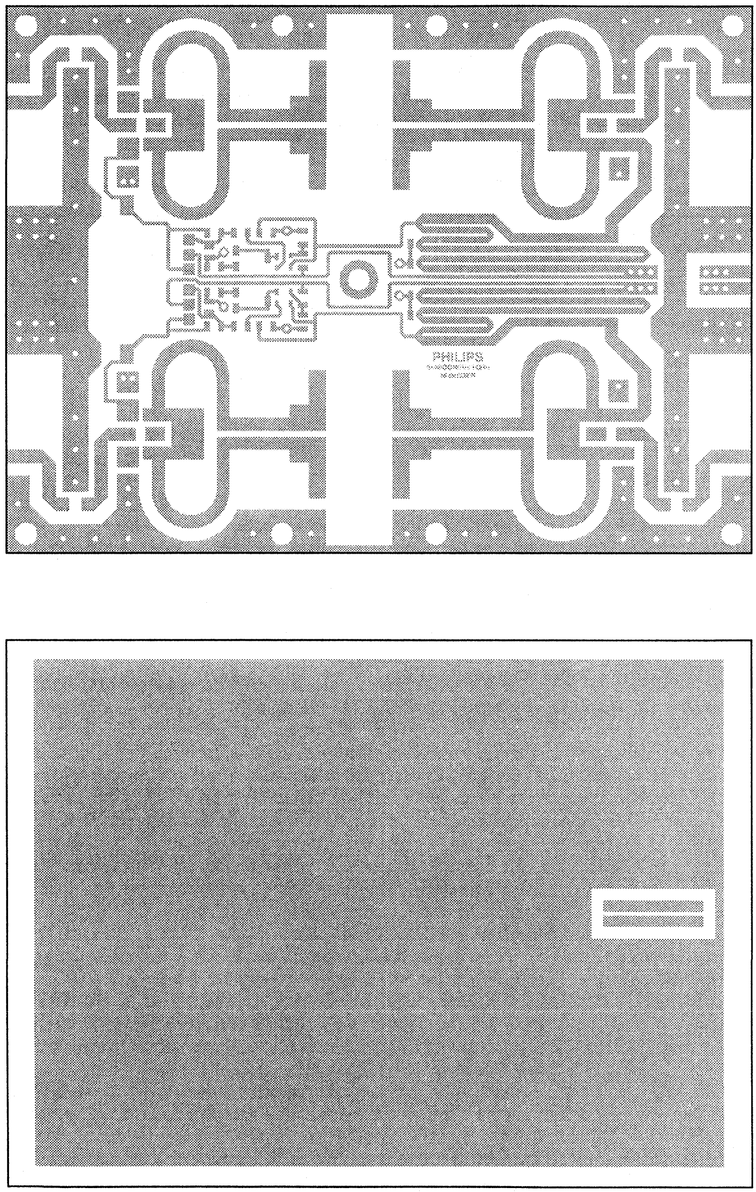
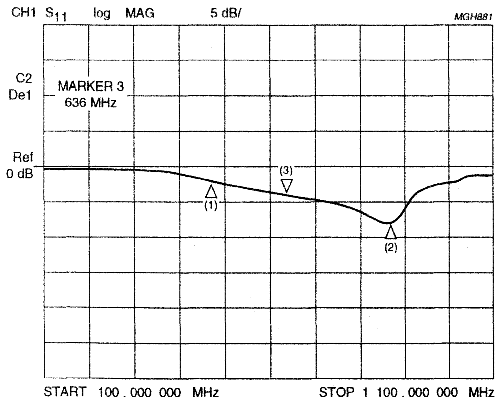


Fig.4 BALUN construction.



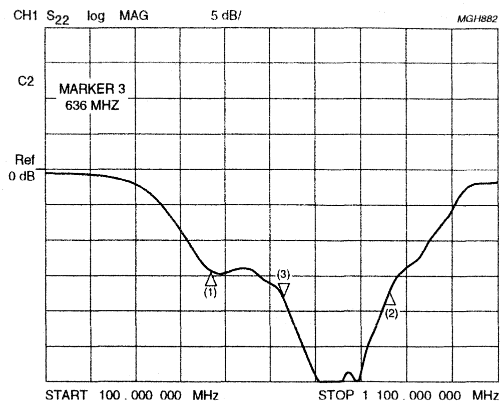
MGH880

Fig.5 Printed-circuit board layout of the frontside and backside (not to scale).



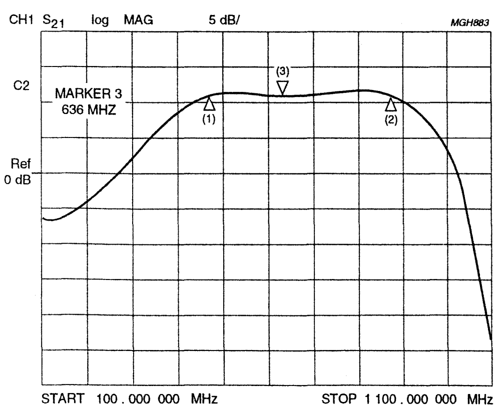
(1) 470 MHz.
(2) 860 MHz.
(3) 636 MHz; −4 dB.

Fig.6 Small signal results of a separated amplifier; a.



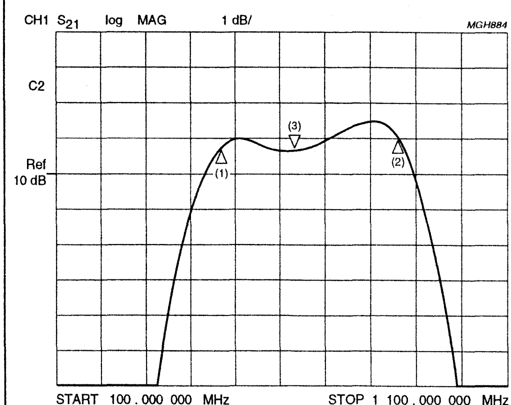
(1) 470 MHz.
(2) 860 MHz.
(3) 636 MHz; −17.8 dB.

Fig.7 Small signal results of a separated amplifier; b.



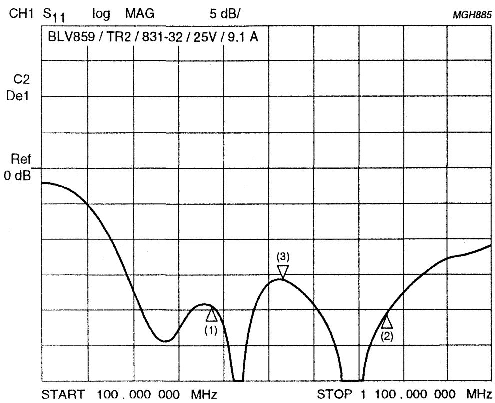
(1) 470 MHz.
(2) 860 MHz.
(3) 636 MHz; −10.55 dB.

Fig.8 Small signal results of a separated amplifier; c.



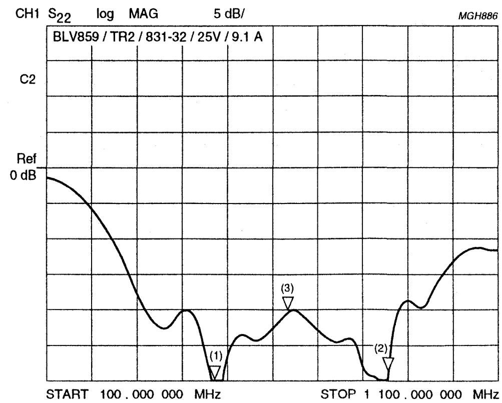
(1) 470 MHz.
(2) 860 MHz.
(3) 636 MHz; −10.65 dB.

Fig.9 Small signal results of a separated amplifier; d.



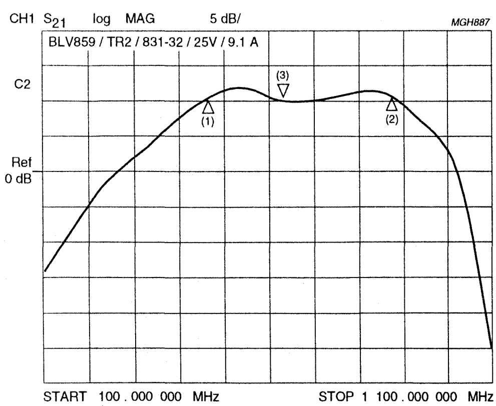
(1) 470 MHz.
(2) 860 MHz.
(3) 636 MHz; −15.8 dB.

Fig.10 Small signal results of the total model; a.



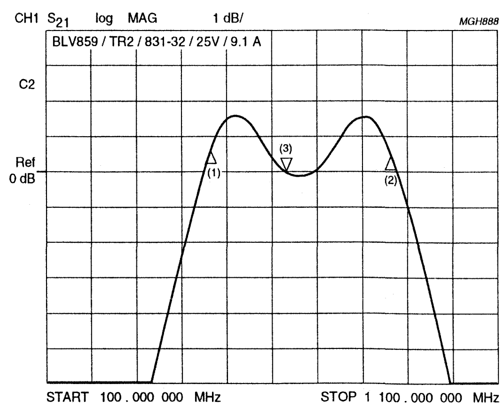
(1) 470 MHz.
(2) 860 MHz.
(3) 636 MHz; −20.3 dB.

Fig.11 Small signal results of the total model; b.



(1) 470 MHz.
(2) 860 MHz.
(3) 636 MHz; −9.6 dB.

Fig.12 Small signal results of the total model; c.



(1) 470 MHz.
(2) 860 MHz.
(3) 636 MHz; −9.7 dB.

Fig.13 Small signal results of the total model; d.

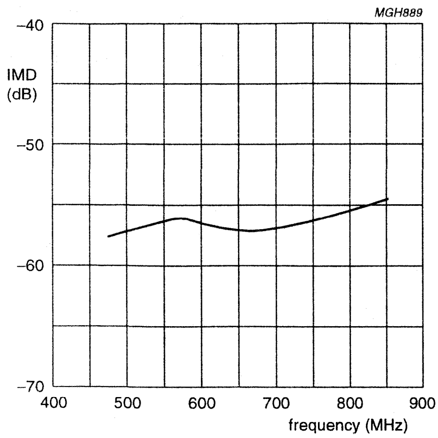


Fig.14 IMD versus frequency for the complete module (Po_sync = 40 W, 3 tones fv = −8 dB, fs = −16 dB, fsb = −10 dB).

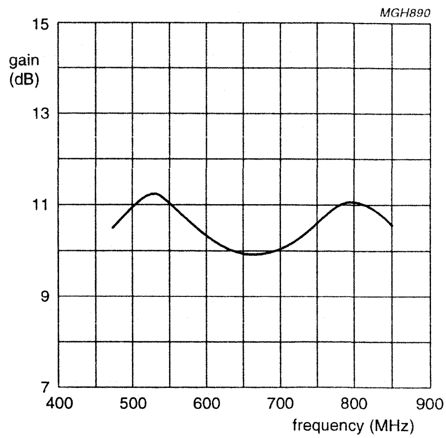


Fig.15 Gain versus frequency for the complete module (Po_sync = 40 W, 3 tones fv = −8 dB, fs = −16 dB, fsb = −10 dB).

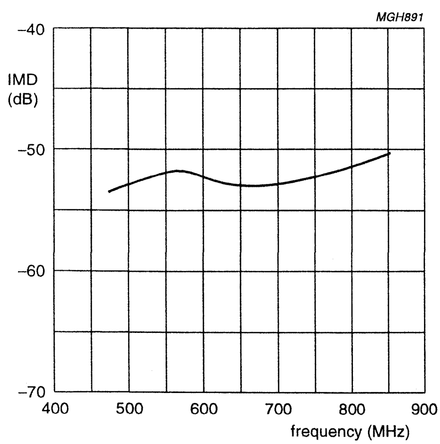


Fig.16 IMD versus frequency for the complete module (Po_sync = 40 W, 3 tones fv = −8 dB, fs = −16 dB, fsb = −7 dB).

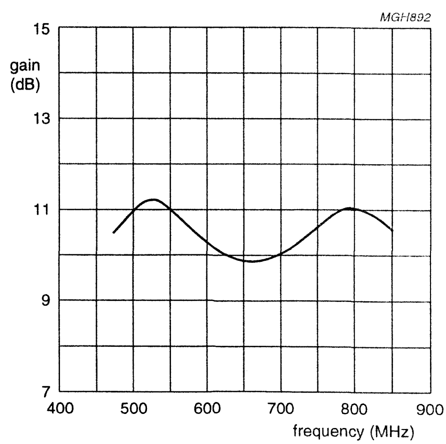


Fig.17 Gain versus frequency for the complete module (Po_sync = 40 W, 3 tones fv = −8 dB, fs = −16 dB, fsb = −7 dB).

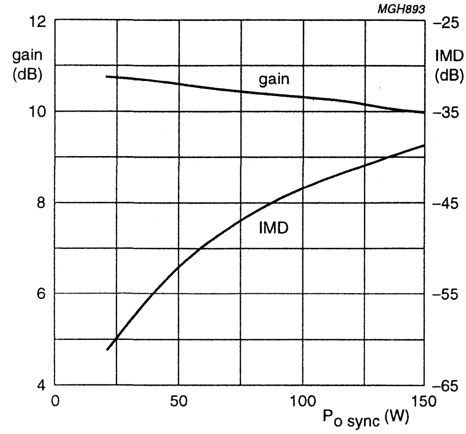


Fig.18 Gain & IMD versus Po_sync for the complete module (3 tones fv = –8 dB, fs = –16 dB, fsb = –10 dB).

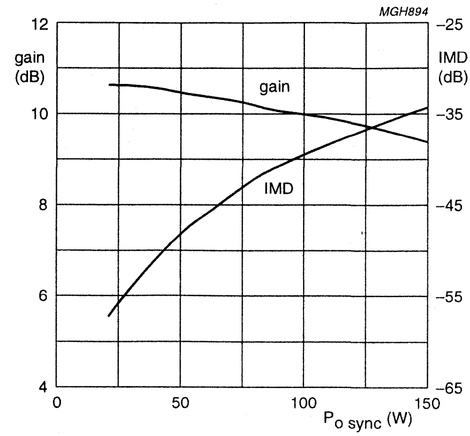


Fig.19 Gain & IMD versus Po_sync for the complete module (3 tones fv = –8 dB, fs = –16 dB, fsb = –7 dB).

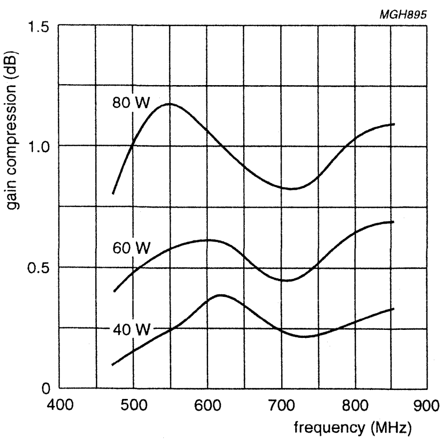


Fig.20 Gain compression for the complete module/Single tone measurement.

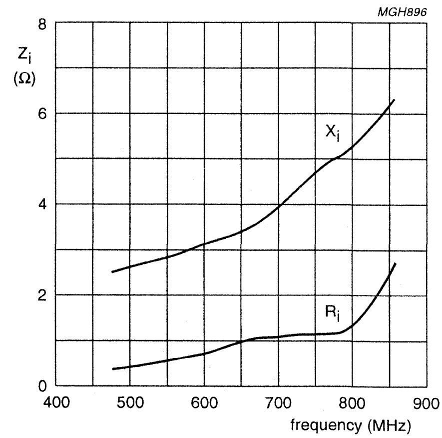


Fig.21 Input impedance (per section).

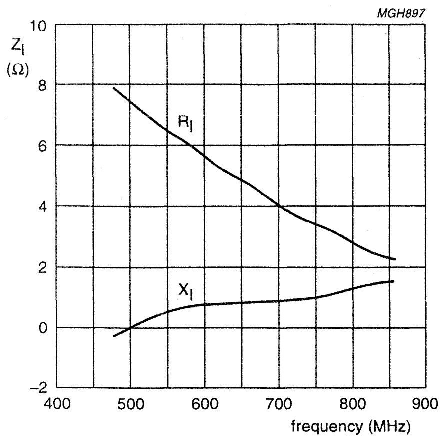


Fig.22 Output impedance (per section).

6 APPENDIX 1

Component list BLV589 module

COMPONENT	DESCRIPTION	VALUE	DIMENSION	12 NC
C1, C2, C3, C5, C6, C14, C15, C16, C17, C18	multilayer ceramic chip capacitor	15 nF	0805	222259016629
C4, C19	solid aluminium capacitor	25 V/47 µF		222203036479
C13, C22	solid aluminium capacitor	63 V/10 µF		222203038109
C7, C8, C20, C21	multilayer ceramic chip capacitor	10 nF	0805	222259016627
C9, C10, C11, C12, C23, C24, C25, C42	multilayer ceramic chip capacitor	100 nF	1206	222259116641
C31, C33, C35, C39	multilayer ceramic chip capacitor (note 1)	12 pF		
C26, C37, C28, C41	multilayer ceramic chip capacitor (note 1)	9.1 pF		
C27, C29, C30, C32, C34, C36, C38, C40	capacitance trimmer REF: 9402 1 Firm: Tekelec	1 to 5 pF		
C27, C28, C29, C30	multilayer ceramic chip capacitor (note 1)	47 pF		
R1, R9	SMD resistor	220 Ω	0805	232273422201
R2, R10	SMD resistor	1.8 Ω	0805	232273421808
R3, R11	SMD resistor	2.7 kΩ	0805	232273422702
R4, R12	SMD resistor	33 Ω	0805	232273423309
R7, R8	SMD resistor	3.3 Ω	0805	232273423308
P1, P2	RG4M08-102VM-TG Firm: muRata Potentiometer	1kΩ		
T1, T3	NPN transistor	BD139		933091220112
T2, T4	double PNP transistor	BVC62		532213060505
B1, B2, B3, B4	semi rigid coax balun UT70-25	ZO = 25 Ω ±1.5 Ω	70 mm	
L1, L2, L15, L16	Striline (note 2)	50 Ω	width 2 mm/length 30.6 mm	
L3, L4	Striline (note 2)	50 Ω	width 2 mm/length 9.5 mm	
L5, L6	Striline (note 2)	32.4 Ω	width 4 mm/length 3 mm	
L7, L8, L9, L10	Striline (note 2)	16.2 Ω	width 9.5 mm/length 2.6 mm	
L11, L12	Striline (note 2)	35.7 Ω	width 3.5 mm/length 3.4 mm	
L13, L14	Striline (note 2)	50 Ω	width 2 mm/length 13.9 mm	
L17	Striline (note 2)		width 1 mm/length 120 mm	

Notes

1. ATC capacitor type 100 A or capacitor of same quality.
2. Printed-circuit board Firm: Rogers ULTRALAM 200 (B0300M1046QB) (ε_r = 2.55) thickness = 0.76 mm.

A broadband 150 W amplifier for band IV & V TV transmitters based on the BLV862

Application Note
AN98014

1 ABSTRACT

A broadband amplifier design is presented based on the BLV862, capable of operating in full band IV & V (470 – 860 MHz) with flat gain and high output power in class-AB. A single amplifier configuration is presented and characterized for aural and vision amplification. This amplifier is able to deliver 150 W CW power and up to 200 W peak-sync power at 1 dB compression point into a 50 W load. For combined vision and sound amplification two-tone and 3-tone performance is presented as well.

Two of these amplifiers have been combined with external quadarture hybrids to demonstrate the power capability of two BLV862. Results include 300 W CW power at 1 dB compression.

The circuit is a compact design on a PTFE-glass laminate with an $\varepsilon_r = 2.55$ and a thickness of 0.51 mm (20 mils).

2 INTRODUCTION

For application in TV-transmitter output stages a broadband high power amplifier design is described with the BLV862 transistor. The design objective based on a single BLV862 is given in Table 1

In the next sections some background on the BLV862 transistor and amplifier design is given. The tuning procedure used for this amplifier is described and its performance for aural and vision amplification presented. Because of the increasing interest for combined amplication of sound and vision also two and 3-tone performance is presented.

Finally full band performance data of two BLV862 amplifiers combined with quadrature hybrids is given.

Table 1 Electric characteristics (V_{CC} = 28 V; Icq = 800 mA)

	SYMBOL	VALUE	UNIT
Frequency band	B	470 – 860	MHz
Output power @ 1 – dB compression; note 1	P_{out}	>150	W
Power gain	G_P	>8	dB
Gain ripple	$G_{P\text{-ripple}}$	±0.5	dB
Efficiency	η	>45	%
Input Return loss	IRL	–8	dB

Note

1. $P_{OUT\text{-ref}}$ = 40 W (CW).

3 TRANSISTOR DESCRIPTION

3.1 Main properties of the BLV862

The BLV862 is a 150 W transistor incorporated in a gemini package SOT262B. A simplified outline of this package is shown in Fig.1. The emitter is connected to the flange and the collector leads are internally parallelled for DC because of the output matching applied. Therefore the collector currents cannot be measured separately.

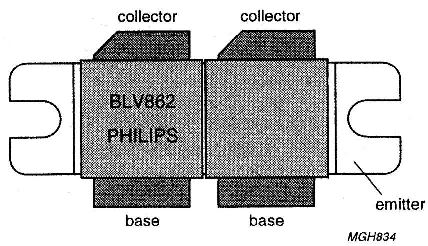


Fig.1 SOT262B package outline of the BLV862.

The active part of the BLV862 consists of four dies with a 6 µm emitter-pitch technology. It incorporates high value postillion emitter ballasting resistor for an optimum temperature profile in class-AB as well as class-A operation. Combined with gold metallization it offers a high degree of reliability and ruggedness. The main transistor data is summarized in Table 2.

Table 2 RF performance of BLV862

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_P (dB)	Eff (%)	$G_{p\text{-}comp\cdot}$ (dB)	$R_{thj\text{-}hs}$ (K/W)
Class-AB	860	28	150	>8 dB	>45%	<1 dB	<0.65

3.2 Internal matching

The BLV862 is internally matched to increase the useable bandwidth and to elevate the device terminal impedance. Figure 2 shows the equivalent circuit of one BLV862 section, with its matching circuitry. The input is pre-matched with two lowpass LC-sections to get low-Q transformation steps and high intermediate impedance level at the base terminals.

The output is post-matched with a collector-to-collector shunt inductor which is designed to resonate with the transistor output capacitance at the low end of the band. This results in an increased broadband capability and increased impedance level at the transistor output.

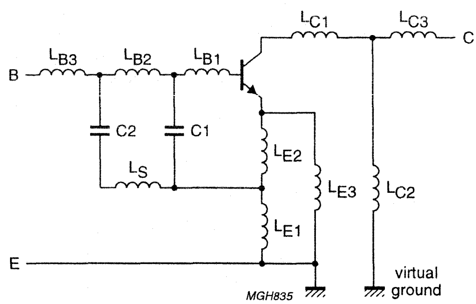


Fig.2 Internal circuit topology of one section of BLV862.

3.3 Gain and impedance data

The gain and impedance data are listed in the Table 3 and curves are given in "Appendix B". This data has been measured in a fixture tuned for maximum gain at rated output power for each frequency. The impedance data given is from base-base and collector-collector.

Table 3 Conditions: V_{CC} = 28 V; I_{cq} = 800 mA; P_L = 150 W

f	G_P	Z_{IN} (Ω)		Z_L (Ω)	
MHz	**dB**	**Re (Z_{IN})**	**Im (Z_{IN})**	**Re (Z_L)**	**Im (Z_L)**
470	12.47	1.01	2.95	4.45	0.83
567	11.63	1.06	4.24	3.22	1.58
665	11.39	2.27	5.96	2.47	0.24
762	10.97	6.96	7.23	1.96	−0.63
860	10.83	6.68	−1.20	1.47	−0.62

4 AMPLIFIER DESIGN

The total description of the amplifier is given in"Appendix A1" to "Appendix A4". The amplifiers input and output matching networks contain mixed microstrip-lumped elements networks to transform the terminal impedance levels to approx. 25 Ω balanced. The remaining transformation to 50 Ω unbalanced is obtained by 1 : 2 balun transformers. The baluns B_1 and B_2 are 25 Ω semi-rigid coax cables with an electrical length of 45° at 636 MHz, soldered over the whole length on top of microstrip lines L_2 and L_{19} of 1.8 mm width. To restore the balance in the circuit two stubs L_1 and L_{20} with the same length have been added. For low frequency stability enhancement the input balun stubs are connected to the point of symmetry by means of 0.5 Ω series resistors. To avoid input signal damping the stubs are decoupled to ground with 1 nF capacitors. The point of symmetry at the input and output balun is used to feed the base and collector from a single bias circuit. Large capacitors are added to these points to improve the amplifiers video response.

The PCB laminate utilized is PTFE-glass with an ε_r = 2.55 and a thickness of 0.51 mm. Specification of all components are given in "Appendix A4".

4.1 Input network

The input network is designed for high gain match and flat overall gain versus frequency. This is achieved by a three section lowpass filter with and a series capacitor at 50 Ω input impedance level. Two variable capacitors are included for fine tuning of the matching @ 860 MHz and flatness adjustment of the gain. See circuit diagram in "Appendix A1". The capacitor C7 is placed close to the base of the BLV862 to maintain low Q transformation.

4.2 Output network

The output network is designed for high output power and efficiency over the full bandwidth. RF dissipation in shunt capacitors is a critical factor in the design of the output network. To minimize the power loss in these components the loaded Q's have been kept as low as possible. This is achieved with the use of a three-section semi-low pass network combined with stubs close to the collectors. The most critical component is the first shunt capacitor from the collectors. The current in this capacitor is at maximum level when operated at the high end of the band at a power level of 150 W (CW). To minimize the loss two high Q capacitors ATC180R are used in parallel. Experiments with lower Q capacitors ATC100B resulted in high losses leading to desoldering of the capacitors at full power level.

4.3 Biascircuit

The class-AB bias circuit used is shown in Fig.3. This circuit has a very low power consumption allowing the use of low power SMD chip resistors. Two NPN transistors BD139 are used. T2 is chosen to operate in the reverse mode in order to have its lower collector to base diode voltage to track the base-emitter voltage of the BLV862. R7 mainly compensates for the difference between these two values. T2, T3 and BLV862 have been mounted on the same heatsink to have good temperature compensation. R8 is incorporated to protect T3 in case of short circuit in the BLV862. For large variations in base currents the V_{BE} level of the BLV862 will show small variations due to this resistor and R2//R3 and R4//R5, see "Appendix A1". No adverse effect will results from this. Capacitor C18 bypass any RF leakage to T2. The bias circuit is fully integrated on the amplifier board, see "Appendix A2".

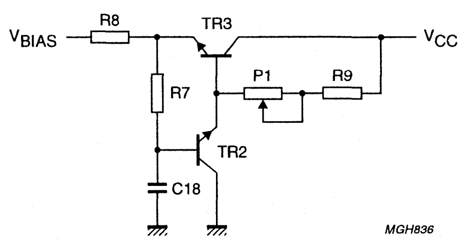


Fig.3 Class-AB biascircuit.

5 PERFORMANCE OF A SINGLE AMPLIFIER CONFIGURATION

The amplifier tuning is done under class-A small-signal conditions and characterized under large signal class-AB conditions from 470 – 860 MHz. The conditions used are:

Table 4 Test conditions

	SMALL SIGNAL	LARGE SIGNAL
Class of operation	A	AB
Collector-emitter voltage	28 V	28 V
Quiescent current (Icq)	2.5 A	0.8 A
Source/Load impedance	50 Ω	50 Ω
Heatsink temperature	25 °C	25 °C

5.1 Small Signal Response

Tuning the amplifier under small-signal class-A conditions to obtain optimum large signal performance was found to be a very suitable and save technique for the BLV862. The best small-signal response was determined experimentally. The S_{11}, S_{22} and S_{21} response resulting in optimum large signal performance is given in “Appendix C1”. The input is tuned for maximum gain and a flat respons over the whole frequency band (470 – 860 MHz). The output is tuned to get at least 10 dB returnloss over the band.

5.2 Large Signal Response

After the small-signal class-A tuning the amplifier was biased into class-AB and large signal measurements were done. Gain, efficiency, input return loss and compression was determined versus frequency at a power level of 150 W (CW). The data is summarized in “Appendix C2”.

The gain level is 8.5 dB on average with a ripple of ±0.5 dB. Efficiency over the whole band is above the 50% level. The minimum efficiency occurs at 762 MHz. See “Appendix C2”. The gain compression at the lower and higher end of the band is about 1 dB while at the centre this is 0.5 dB referenced to a 40 W output power level. The input return loss is up to 3.5 dB at the lower end and 8.5 dB at the upper end of the frequency range.

5.3 3 dB Input Overdrive Capability Test

An input overdrive test has been performed on the amplifier to test its capability to withstand 3 dB overdrive. P_{OUT} vs P_{IN} measurements have been done from zero to 3 dB above its normal drive level for 150 W power output. The amplifier has proven to withstand a drive level of 46 W for several minutes without degradation of the transistor. The power level associated with this level was 200 W. “Appendix E” presents the recorded data.

5.4 Amplitude and Phase Transfer Characteristic

A power sweep measurement has been performed using a network analyzer to determine the input/output transfer characteristics of the amplifier. The linearity of the amplifier is described in terms of the input/output amplitude transfer function known as AM-AM conversion or differential gain and the input/output phase transfer function known as AM-PM conversion or ICPM (incidental carrier phase modulation). The total setup for power sweep is reflected on “Appendix G1”. the sweep range of the network analyzer was set for –10 dBm to +14 dBm.

“Appendix G2” shows the power sweep output from the network analyzer in a multiple sweep format to show the effect of various bias levels in class-AB. Any deviation from a straight line is a measure of non-linearity in the amplifier. Slight gain variations are to be expected at turn on. Important points for observation are the 1 dB gain compression point and the phase deviation at 1 dB gain compression referenced to the maximum phase in the linear gain region. The phase shift is about 6° at the 1 –dB compression point for 800 mA bias level. The stop between sweep power level was measured at 165 W and coincides with the 1 dB compression point.

5.5 Intermodulation

Because of the increasing interest for combined carrier options we have determined the linear performance of the amplifier for 2-tone and 3-tone operation. IMD has been measured at 860 MHz for different tone levels. Since the bias level dependency was found not to be very strong only results at 800 mA are presented.

Two tone and three tone IMD-measurement have been performed as defined in Fig.4. For two tone performance two carriers have been chosen which represents the vision and sideband carriers. Three tone measurement is done with an additional carrier which represents the sound carrier. The different tone systems used are listed below.

Table 5 Survey of used tone systems for intermodulation measurements

SYSTEM	AMPLITUDE VISION	AMPLITUDE SIDEBAND	AMPLITUDE SOUND	UNIT
A	−8	−16	−10	dB
B	−5	−17	−10	dB
C	−3	−20	−10	dB
Tones	855.25	859.68	860.75	MHz

IMD-performance is depicted as a function of the output peak-sync power (P_{SYNC}) in “Appendix D1” and “Appendix D2”.

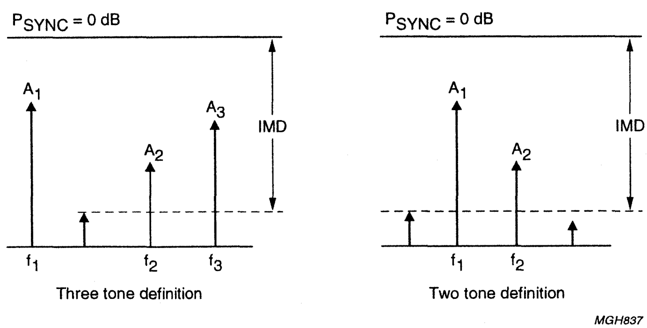


Fig.4 Definition for IMD-measurement.

5.6 TV-measurements

The amplifier is also characterized with a PAL composite TV signal (without soundcarrier) according CCIR standard G. The TV test setup used, is depicted in “Appendix F1”. The following important characteristics have been measured in channel 69:

- Differential gain (level dependence of gain)
- Differential phase (level dependence of phase)
- Sync compression
- Peak output power @ 1 dB compression.

5.6.1 DIFFERENTIAL GAIN

Differential gain is present if chrominance gain is dependent on luminance level. These amplitude errors are a result of the systems inability to uniform process the high-frequency chrominance signal at all luminance levels. Differential gain is expressed in percentage of the chrominance gain at blanking levels. Differential gain is expressed in percentage of the chrominance gain at blanking level. The input video waveform used for differential gain evaluation is a modulated staircase with 10% rest carrier as given in “Appendix F2”.

“Appendix F2” and “Appendix F3” depicts the differential gains in channel 69 at a peak-sync power level of 150 W for several bias levels.

5.6.2 DIFFERENTIAL PHASE

Differential phase is present if a signals chrominance phase is affected by luminance level. This phase distortion is a result of a systems inability to uniform process the high-frequency chrominance information at all luminance levels. The amount of differential phase distortion is expressed in degrees. Differential phase data for the same conditions are also given in “Appendix F2” and “Appendix F3”.

5.6.3 SYNC COMPRESSION VS PEAK-SYNC POWER

One effect produced by non-linearity above the blanking level is compression of the sync pulse. This effect is compensated in transmitters by making the sync pulses correspondingly greater before amplification.

The degree of this so called sync-stretching required, depends on the sync compression due to the non-linearity in the amplifier.

Evaluation of the sync compression is done using a input video waveform at black level, see “Appendix F4”. The sync power is calculated by from the measured average output power and the sync-to-bar ratio after demodulation. The sync-to-bar ratio is measured with the video waveform on line 18 containing a 100% white-bar. With this available ratio the sync amplitude can be calculated referenced to a 1 V sync-to-bar top level. The sync content is then normalized to a 1.11 V RF amplitude. An undistorted signal corresponds to 27% sync content.

The sync power can then also be determined from the obtained sync level. The formula and definitions used for this calculation are given below (1) and in Fig.5. The output sync pulse content versus Psync power is presented in “Appendix F4”.

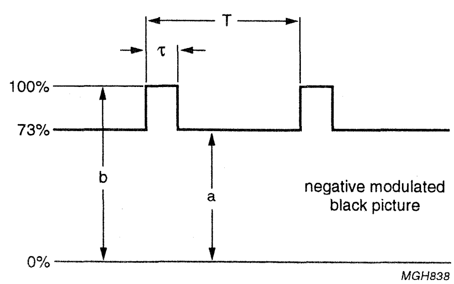


Fig.5 Composite video signal with black level for determining sync-peak power.

$$P_{RMS} = \frac{U_{RMS}^2}{R} = \frac{\left(\sqrt{\frac{1}{T}\int_0^{\tau} b^2 \cdot dt + \frac{1}{T}\int_{\tau}^{T} a^2 \cdot dt}\right)}{R} = \frac{\frac{\tau}{T} \cdot b^2 + \left(1 - \frac{\tau}{T}\right) \cdot a^2}{R} \qquad P_{SYNC} = \frac{b^2}{R} \quad \Bigg\} \; k = \frac{P_{SYNC}}{P_{RMS}} = \frac{1}{\frac{\tau}{T} + \left(1 - \frac{\tau}{T}\right) \cdot \left(\frac{a}{b}\right)^2} \tag{1}$$

If there is no compression (a = 73% and b = 100%) then k = 0.567 and sync-power corresponds to $P_{SYNC} = P_{RMS}/0.567$. If there is a maximum sync-compression, which means that a = b, then k = 1 and as a result P_{SYNC} will be equal to P_{RMS}. In practice the allowable sync compression is bound to a maximum since sync-stretching is limited.

5.6.4 PEAK OUTPUT POWER AT 1 dB COMPRESSION

"Appendix F4" shows the gain versus Psync power for channel 69. The input video signal is at black level. The 1 dB compression point is approximately 190 W Psync.

6 DUAL AMPLIFIER CONFIGURATION

Two single amplifiers were combined using external quadrature couplers as depicted in Fig.6. Broadband CW measurements has been performed to test the capability of the combined BLV862 amplifiers. The conditions for each amplifier are listed in "Performance of a single amplifier configuration".

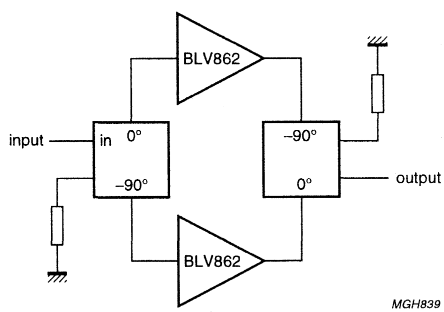


Fig.6 Dual amplifier configuration of BLV862.

6.1 Small Signal Response

The small signal plots in class-A of the combined amplifiers are given in "Appendix H1". Only a gain loss of 0.5 dB has been observed. On the otherhand the input and output is now perfectly matched. The gain-ripple is still acceptable which is approximately ±1 dB.

6.2 Large Signal Response

The large signal gain in class-AB is above 7 dB and 300 W. Gain compression at different frequencies has been determined. At a loadpower of 300 W the gain compression is about ±1 dB over the whole frequency range. See "Appendix H2".

Efficiency of the combined amplifiers is within the specifications which is >45%. As mentioned before. at 762 MHz the efficiency reaches its lowest value, but still >45%. See “Appendix H2”.

7 CONCLUSIONS

A complete TV transmitter amplifier has been designed and characterized based on the BLV862, capable of operating in full band IV & V with flat gain and high output power in class-AB. With one BLV862 it is possible to generate 150 W CW power at 1 dB compression with a gain of >8 dB and an efficiency of >45%. Two amplifiers combined with quadrature couplers have shown to deliver 300 W CW power at 1 dB compression with >7 dB gain and 45% efficiency.

TV-measurements have been performed showing a 1 dB compression point close to 200 W Psync from one BLV862. The prototype has been reproduced five times with very good repeatability.

8 REFERENCES

1. TEKTRONIX: “Television measurements – PAL systems”
2. Rhode & Schwarz Sound and Broadcasting: “Rigs and Recipes how to measure and monitor...”.

9 APPENDIX

- A1: Schematic diagram of the BLV862 amplifier
- A2: Component layout of the BLV862 amplifier and Layout of the BLV862 amplifier
- A4: List of components
- B: Gain and input-output impedance of two sections
- C1: Small signal respons of the BLV862 amplifier in class-AB operation
- C2: CW results of the BLV862 amplifier
- D1: Two tone intermodulation in class-AB
- D2: Three tone intermodulation in class-AB
- E: 3 dB input overdrive capability test
- F1: TV measurement setup
- F2: Differential Gain and Phase
- F3: Differential Gain and Phase
- F4: Sync compression vs. peak-sync power
- G1: Setup for phase linearity measurement
- G2: Gain and phase deviation
- H1: Small signal respons of two BLV862 amplifiers in class-AB combined with 3 dB quadrature hybrids
- H2: RF performance of two BLV862 amplifiers combined with 3 dB quadrature hybrids.

10 APPENDIX A1

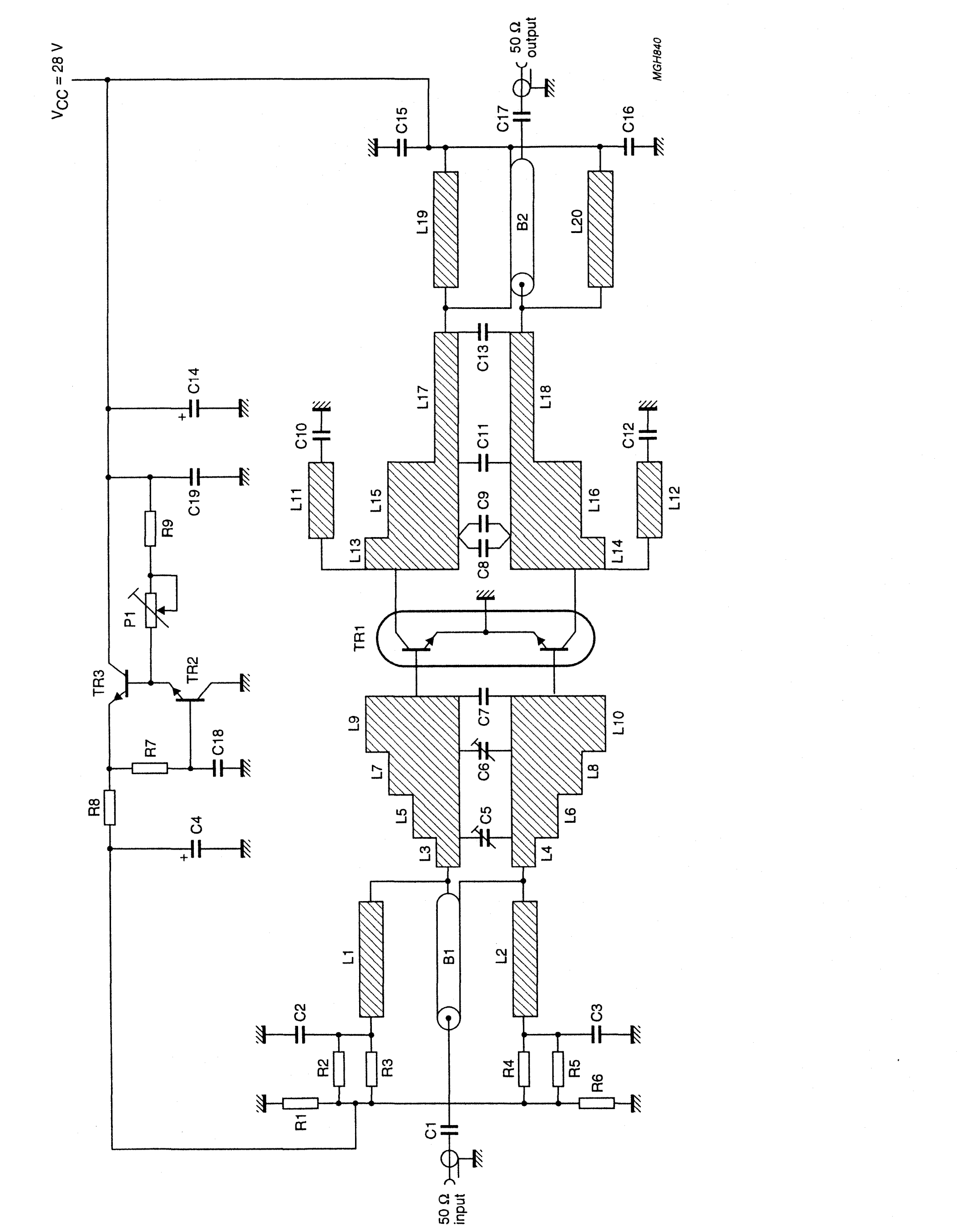


Fig.7 Schematic diagram of the BLV862 amplifier.

11 APPENDIX A2

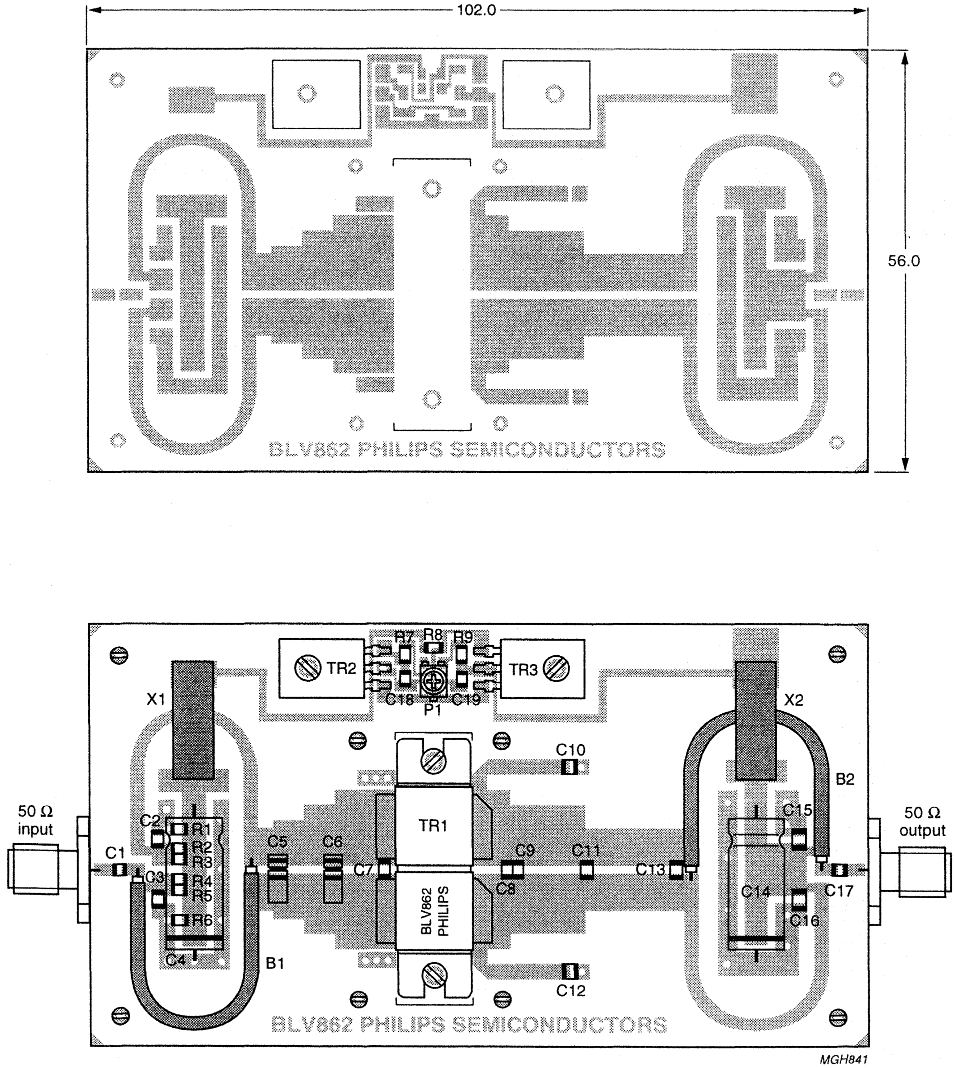


Fig.8 Component layout of the BLV862 amplifier.

12 APPENDIX A4

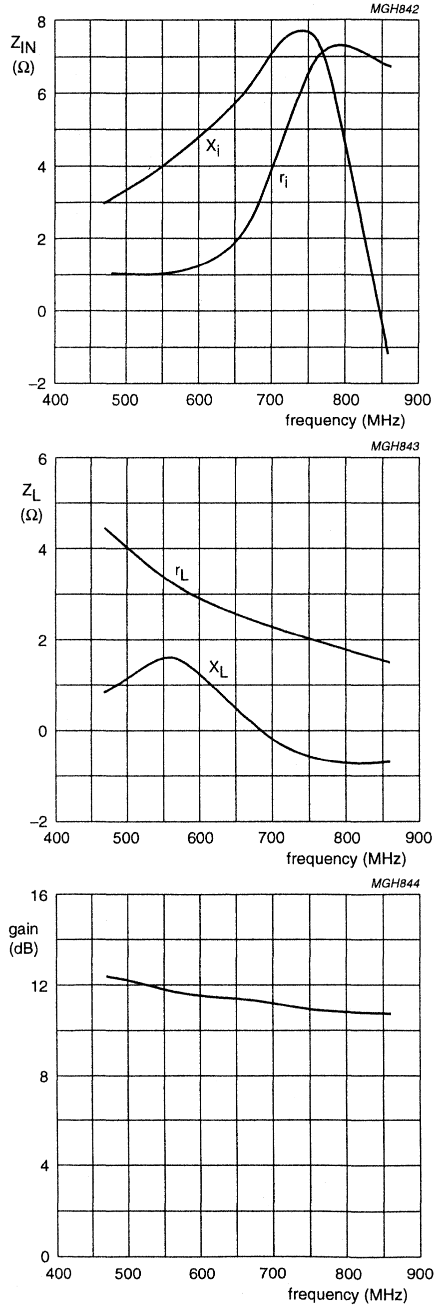
List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1	Multilayer ceramic chip capacitor; note 1	10 pF		
C2, C3	Multilayer ceramic chip capacitor	1 nF		222285247102
C4	Solid aluminium capacitor	220 µF/16 V		222203135221
C5, C6	Multilayer ceramic chip capacitor; note 2 + Tekelec trimmer	6.8 pF/0.6 – 4.5 pF		
C7	Multilayer ceramic chip capacitor; note 2	13 pF		
C8, C9	Multilayer ceramic chip capacitor; note 3	10 pF		
C10 C12	Multilayer ceramic chip capacitor; note 1	100 pF		
C11	Multilayer ceramic chip capacitor; note 2	8.2 pF		
C13	Multilayer ceramic chip capacitor; note 2	3.9 pF		
C14	Solid aluminium capacitor	100 µF/40 V		222203137101
C15, C16	Multilayer ceramic chip capacitor	100 nF		222285247104
C17	Multilayer ceramic chip capacitor; note 1	22 pF		
C18	Multilayer ceramic chip capacitor; note 1	100 pF		
C19	Multilayer ceramic chip capacitor	15 nF		222285247153
R1, R6	SMD resistor	100 Ω	805	212211803881
R2, R3, R4, R5, R8	SMD resistor	1 Ω	805	212211804562
R7	SMD resistor	47 Ω	805	212211804598
R9	SMD resistor	1.2 kΩ	805	212211804579
P1	Potentiometer	5 kΩ		
T1	NPN push-pull RF-transistor	BLV862		934038450112
T2, T3	NPN transistor	BD139		933091220112
B1	Semi rigid coax balun UT70-25	Z = 25 ±1.5 Ω	47.0 mm	
B2	Semi rigid coax balun UT70-25	Z = 25 ±1.5 Ω	48.7 mm	
X1, X2	Copper ribbon hairpin			
L1, L2	Stripline; note 4		47.0 × 1.8 mm	
L3, L4	Stripline; note 4		2 × 5 mm	
L5, L6	Stripline; note 4		4 × 6 mm	
L7, L8	Stripline; note 4		4 × 8 mm	
L9, L10	Stripline; note 4		8.1 × 10 mm	
L11, L12	Stripline; note 4		15 × 2 mm	
L13, L14	Stripline; note 4		5 × 10 mm	
L15, L16	Stripline; note 4		10 × 8 mm	
L17, L18	Stripline; note 4		12.9 × 5 mm	
L19, L20	Stripline; note 4		48.7 × 1.8 mm	

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. American Technical Ceramics type 180R or capacitor of same quality.
4. The striplines are on a double copper-clad PCB: PTFE-glass material (TLX8) from Taconic (epsilon of 2.55).

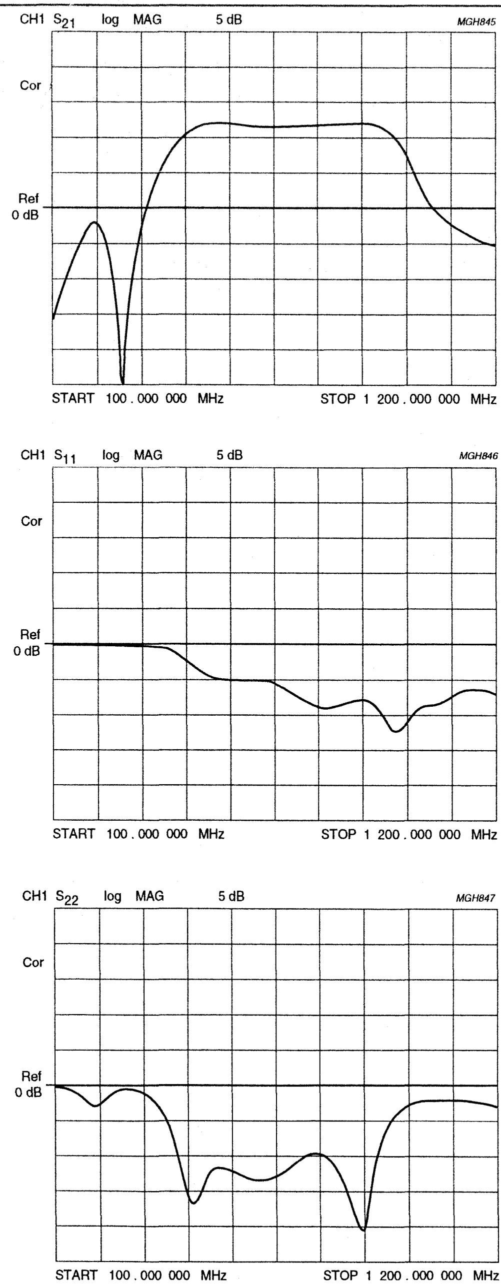
13 APPENDIX B



V_{CC} = 28 V; I_{cq} = 800 mA;
P_{OUT} = 150 W; T_{hs} = 25 °C.

Fig.9 Gain and input-output impedance of two sections.

14 APPENDIX C1

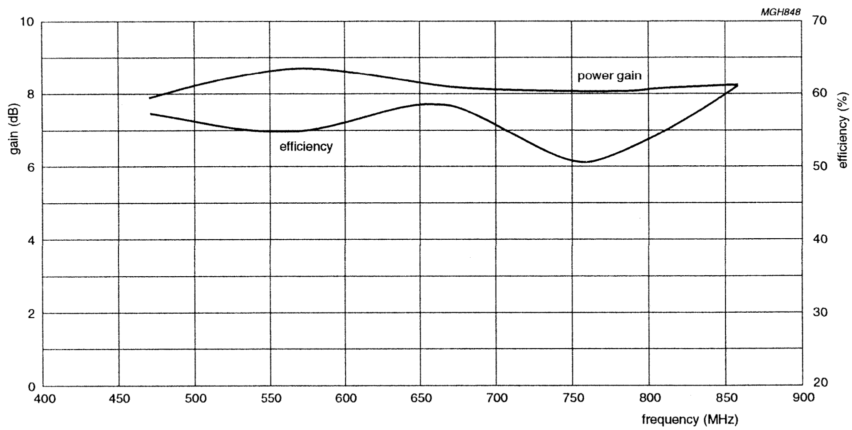


V_{CC} = 28 V; I_{cq} = 2.5 A; T_{hs} = 25 °C.

Fig.10 Small signal respons of the BLV862 amplifier in class-AB operation.

15 APPENDIX C2

FREQ (MHz)	P_{OUT} (W)	PIN-F (W)	PIN-R (W)	Ic (A)	Gp (dB)	EFF (%)	IRL (dB)	COMP. (dB)
470	150	24.40	11.00	9.31	7.89	57.54	−3.46	−1.05
567	150	20.04	7.20	9.77	8.74	54.83	−4.45	−0.47
665	150	22.50	6.40	9.12	8.24	58.74	−5.46	−0.54
762	150	23.00	3.65	10.55	8.14	50.78	−7.99	−0.56
860	150	22.20	3.14	8.75	8.30	61.22	−8.49	−0.86



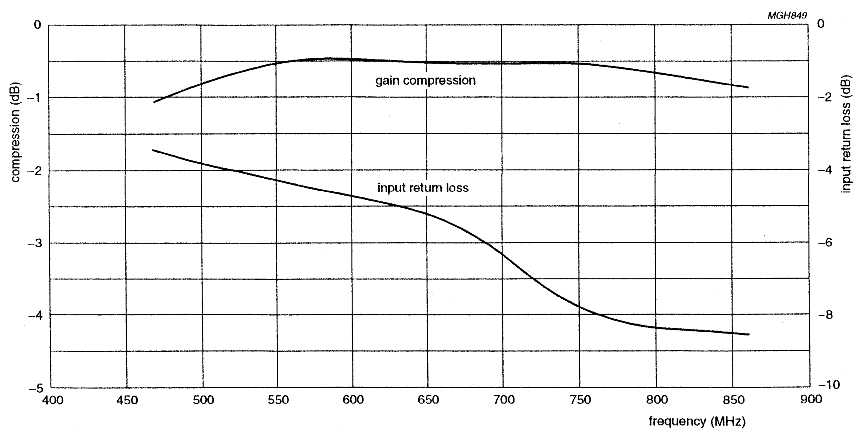
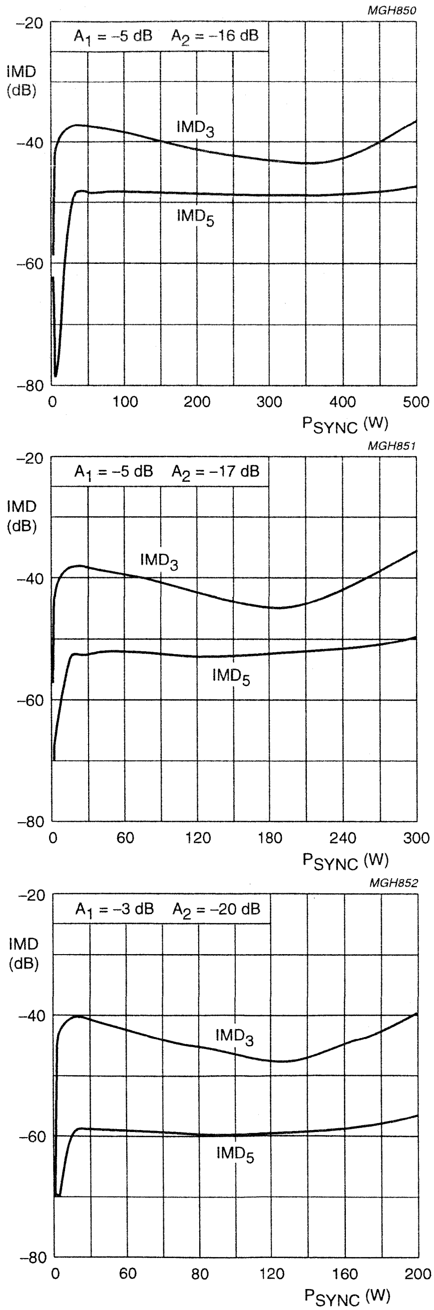


Fig.11 CW results of the BLV862 amplifier.

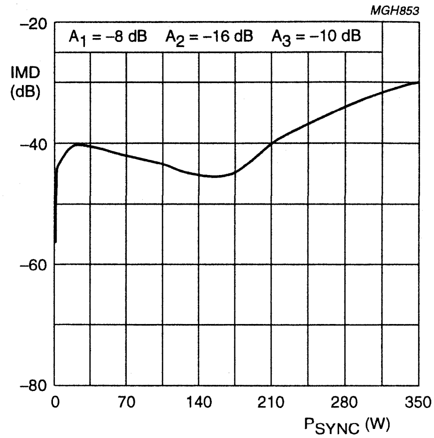
16 APPENDIX D1

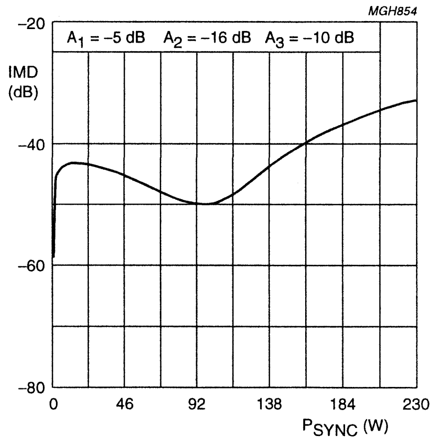


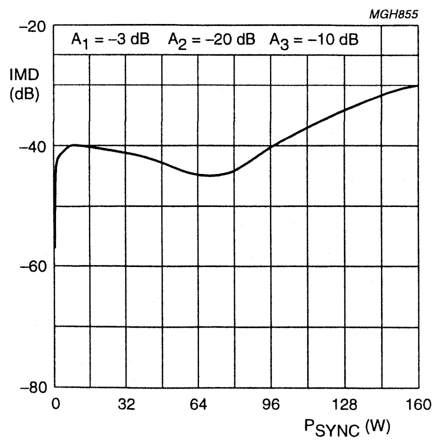
V_{CC} = 28 V; I_{cq} = 800 mA; T_{hs} = 25 °C.

Fig.12 Two tone intermodulation in class-AB.

17 APPENDIX D2



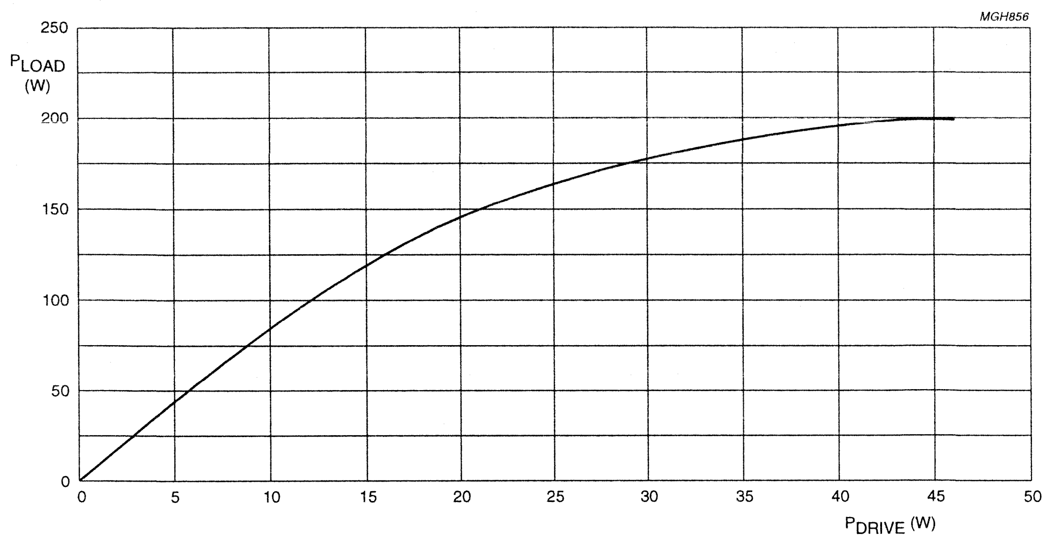




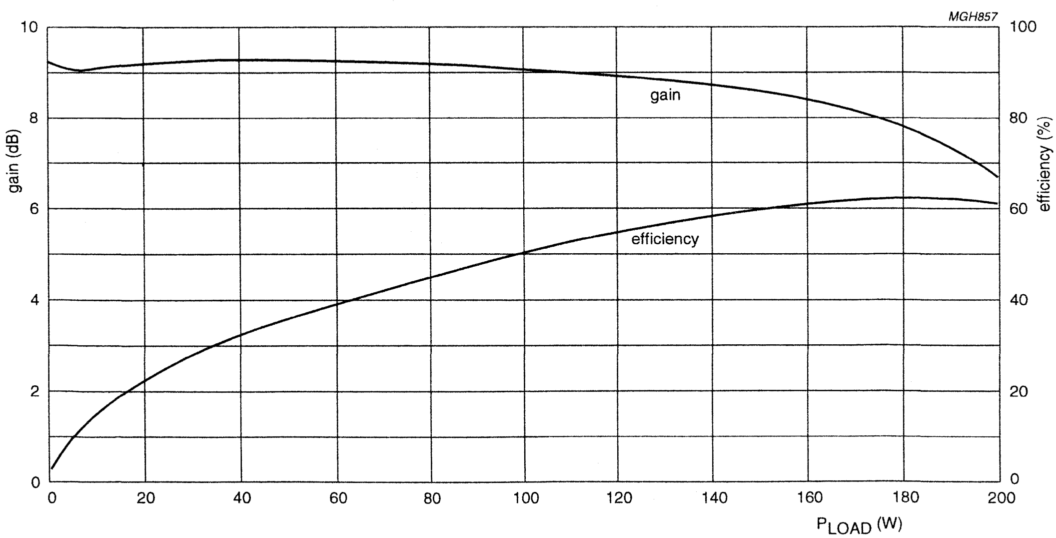
V_{CC} = 28 V; I_{cq} = 800 mA; T_{hs} = 25 °C.

Fig.13 Three tone intermodulation in class-AB.

18 APPENDIX E



a. Loadpower vs. input power.



b. Gain and efficiency vs. loadpower.

V_{CC} = 28 V; I_{cq} = 800 mA; freq. = 860 MHz; T_{hs} = 25 °C.

Fig.14 3 dB input overdrive capability test.

19 APPENDIX F1

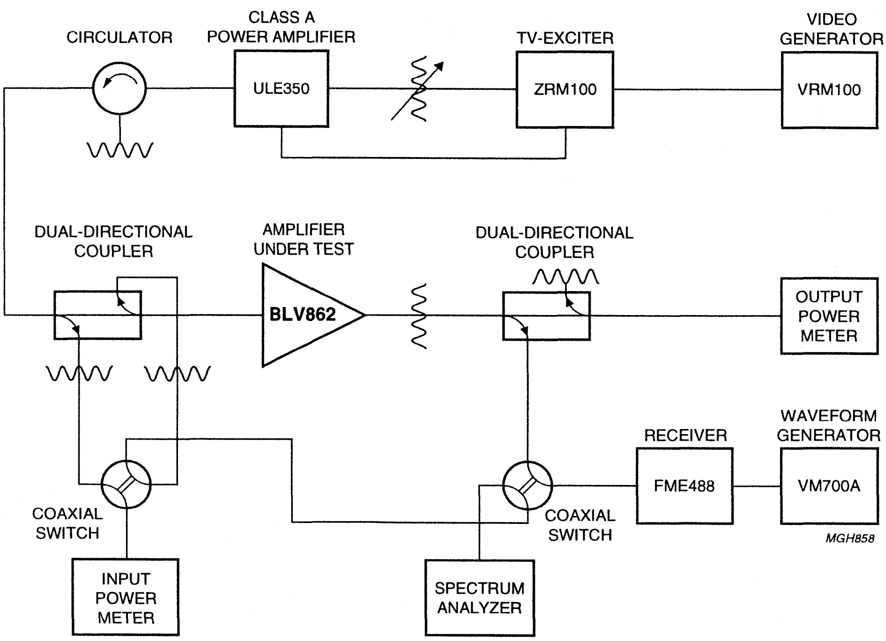
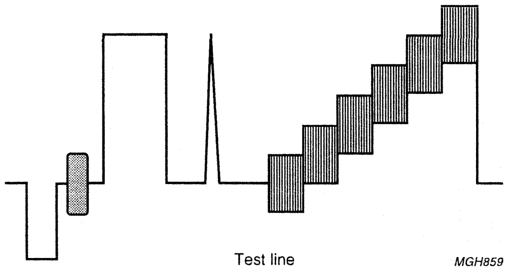
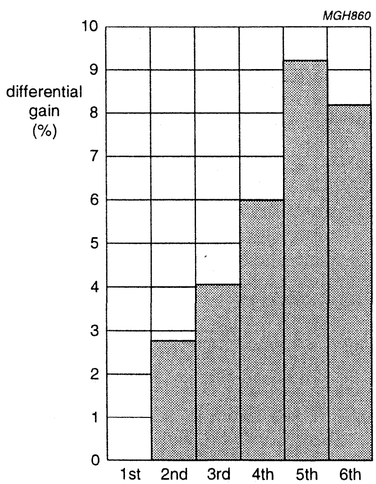


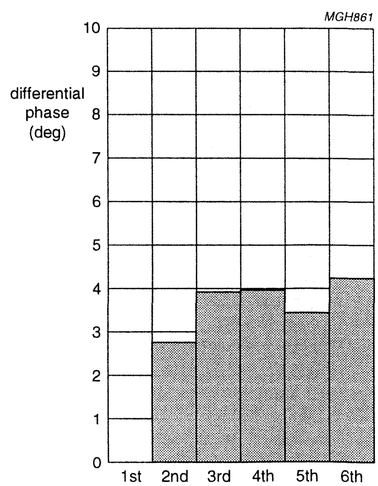
Fig.15 TV measurement setup.

20 APPENDIX F2



Channel 69; $P_{o,sync}$ = 150 W; 10% residual carrier; V_{CC} = 28 V; T_{hs} = 25 °C; Picture content: colour bar.





I_{cq} = 800 mA.

Fig.16 Differential Gain and Phase.

21 APPENDIX F3

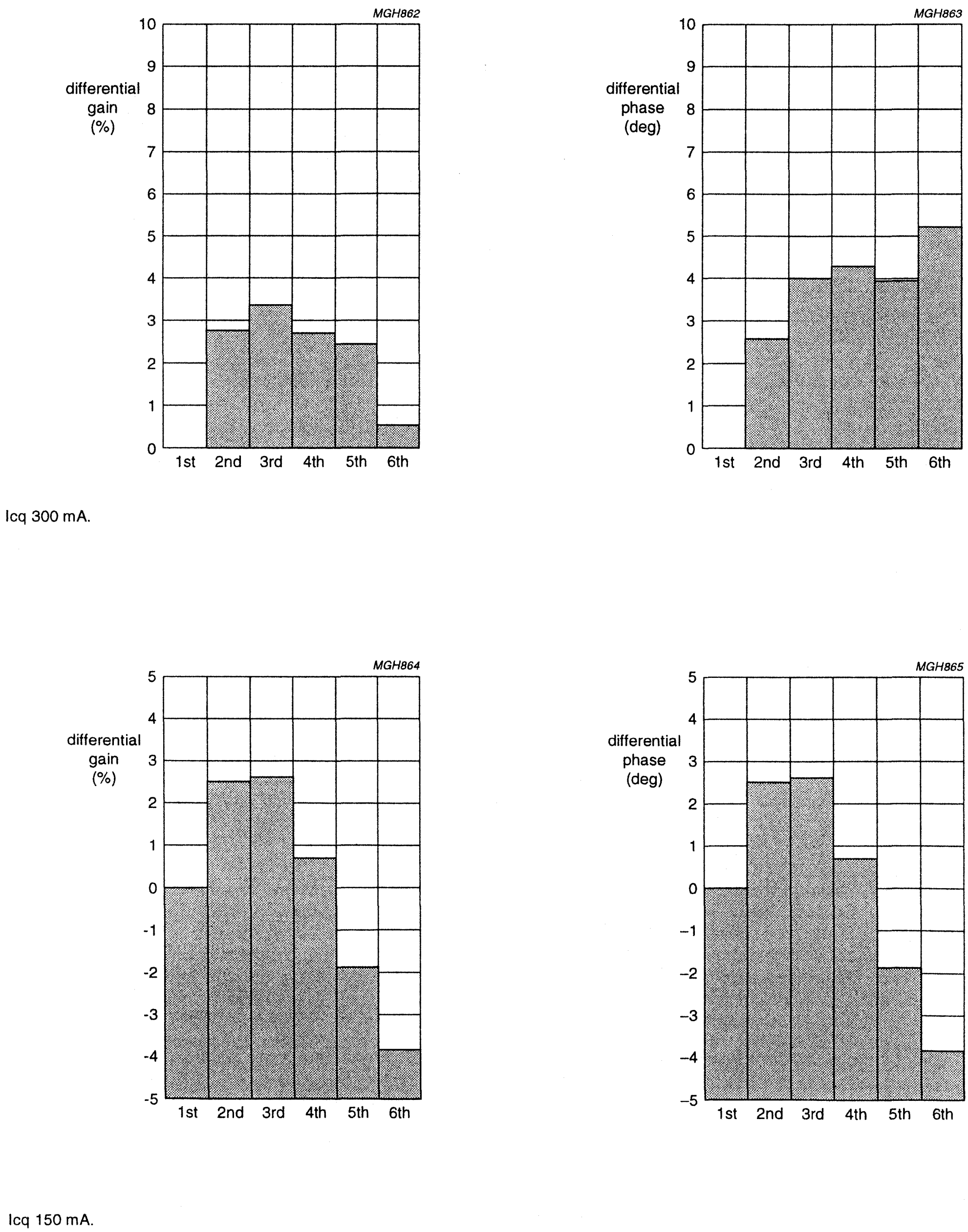
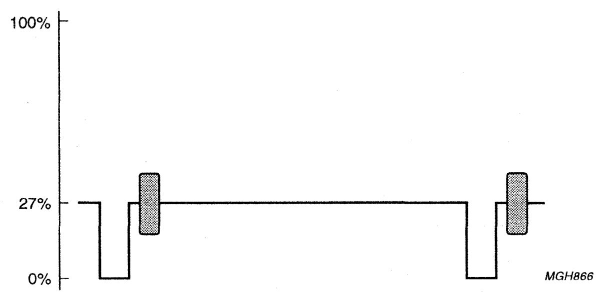


Fig.17 Differential Gain and Phase.

22 APPENDIX F4



Test conditions: channel 69; black level; V_{CC} = 28 V; I_{cq} = 800 mA; T_{hs} = 25 °C.

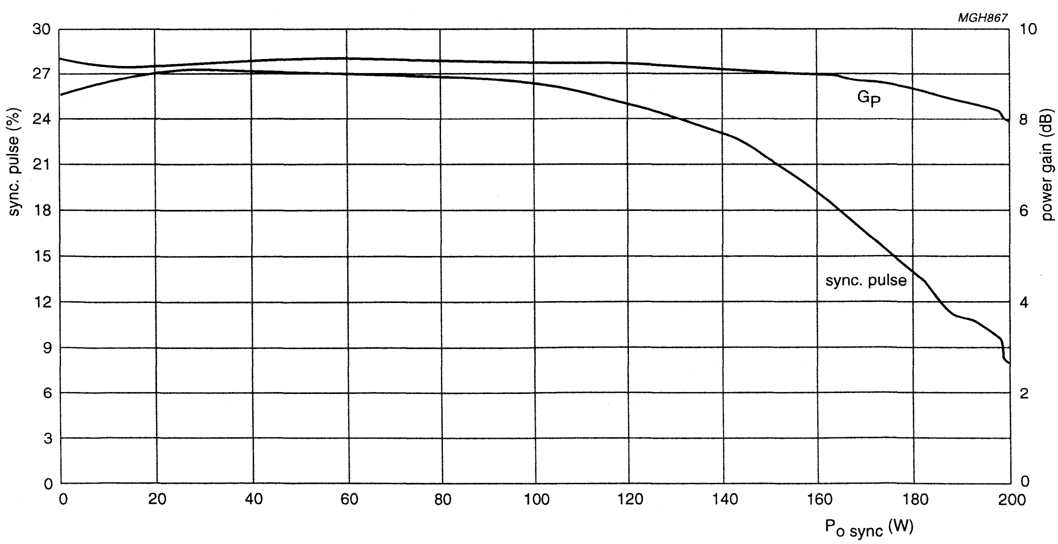


Fig.18 Sync compression vs. peak-sync power.

23 APPENDIX G1

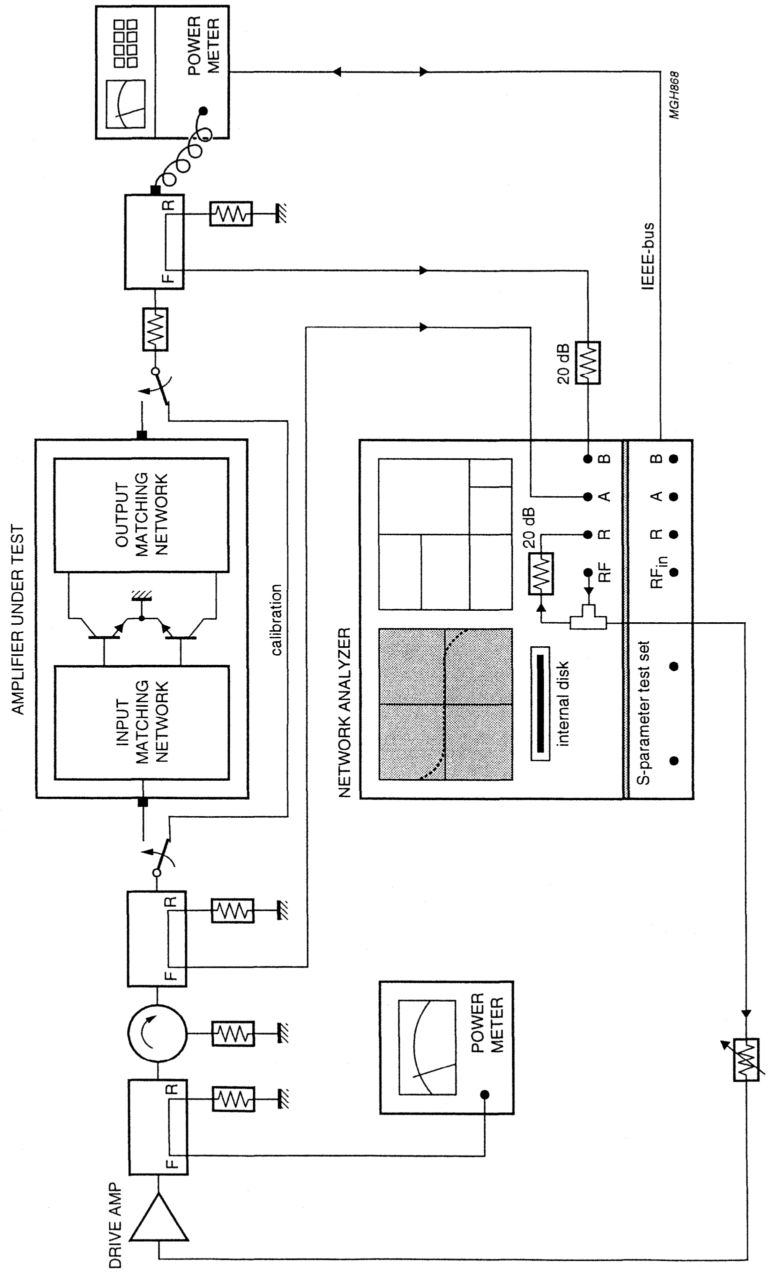


Fig.19 Setup for phase linearity measurement.

24 APPENDIX G2

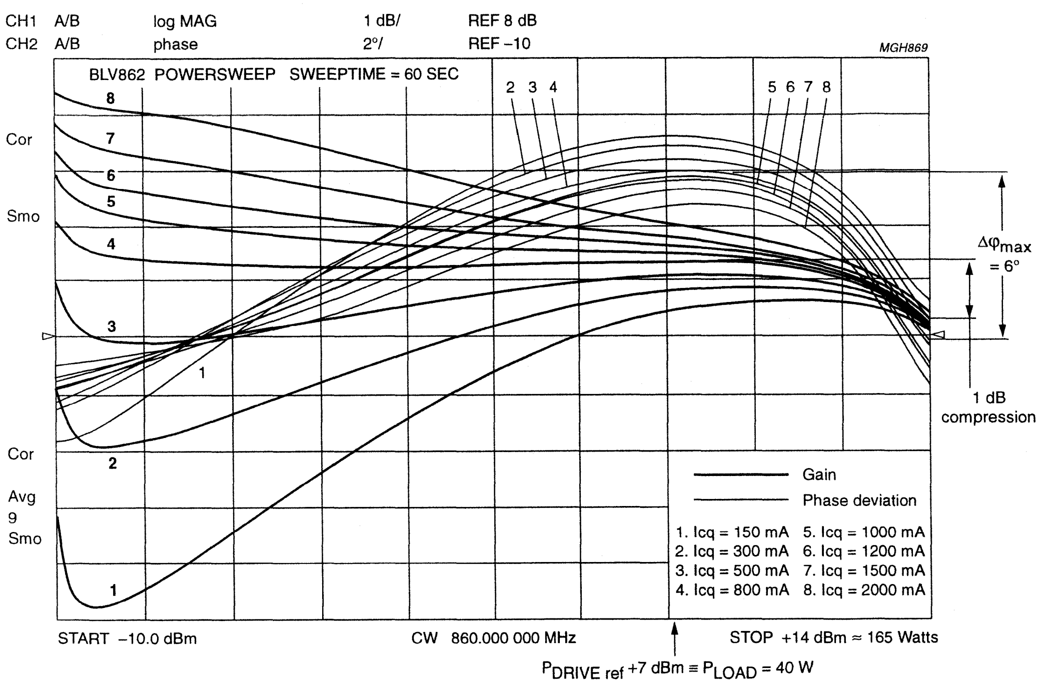
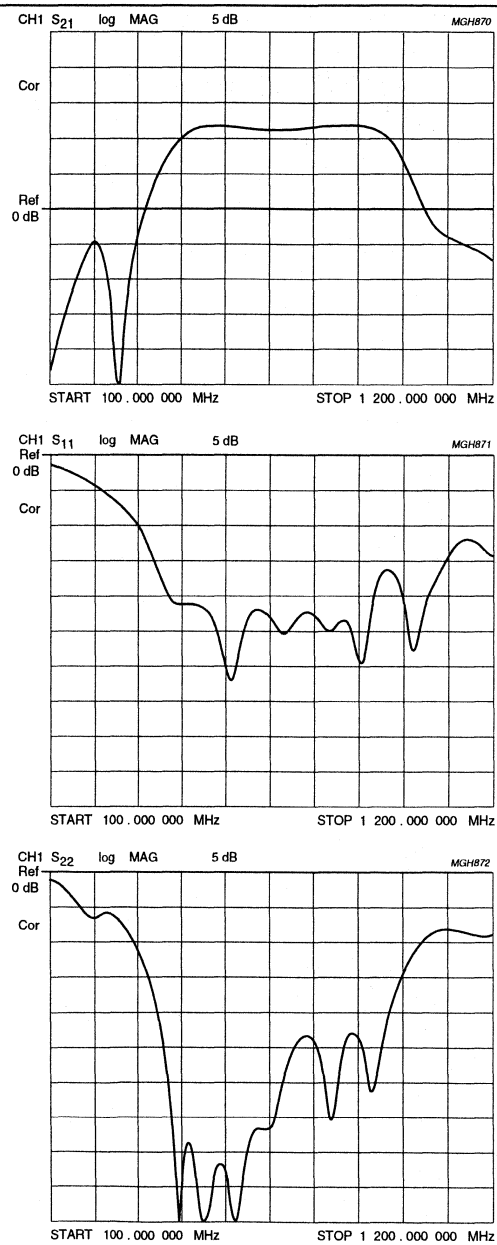


Fig.20 Gain and Phase deviation.

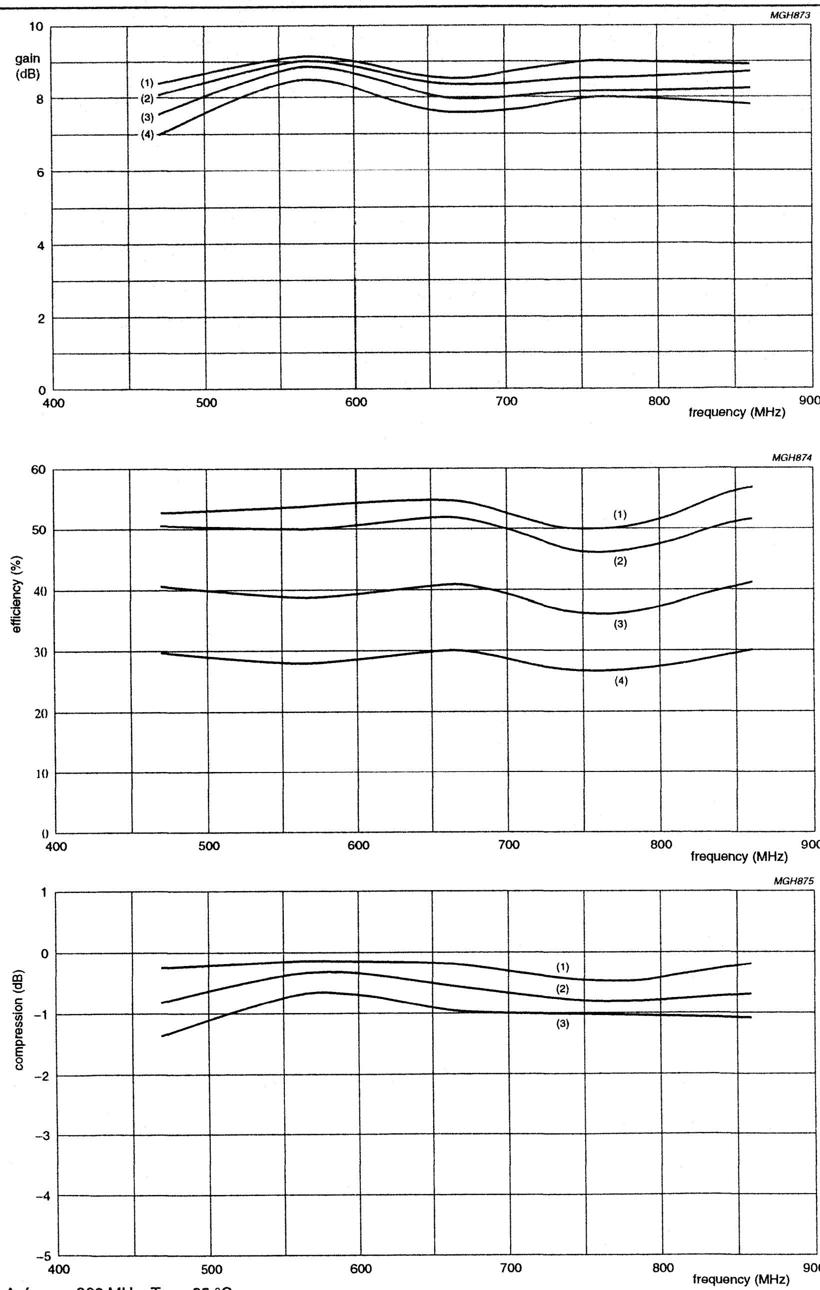
25 APPENDIX H1



V_{CC} = 28 V; I_{cq} = 2.5 A (each amplifier); T_{hs} = 25 °C.

Fig.21 Small signal respons of two BLV862 amplifiers in class-AB combined with quadrature hybrids.

26 APPENDIX H2



(1) P_L = 80 W.
(2) P_L = 150 W.
(3) P_L = 250 W.
(4) P_L = 300 W.

(1) P_L = 80 W.
(2) P_L = 150 W.
(3) P_L = 250 W.
(4) P_L = 300 W.

(1) P_L = 150 W.
(2) P_L = 250 W.
(3) P_L = 300 W.

V_{CC} = 28 V; I_{cq} = 800 mA; freq. = 860 MHz; T_{hs} = 25 °C.

Fig.22 RF performance of two BLV862 amplifiers combined with 3 dB quadrature hybrids.

A broadband 3 W amplifier for band IV/V TV transposers based on the BLW898

Application Note
AN98015

1 ABSTRACT

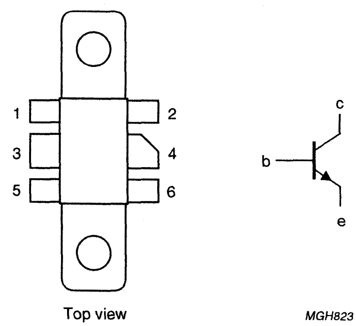
A broadband linear amplifier design is presented, suitable for application in TV transposers, operating in band IV and V (470 – 860) MHz. The design is based on a BLW898 bipolar transistor. Typical results at the recommended class-A bias point (25 V/1.1 A) for the total module include a 3-tone IMD level of –64 dB (fvision = –8 dB, fsideband = –16 dB and fsound = –10 dB) and an average gain of 10.5 dB at 3 W peak-sync output power in the (470 – 860) MHz frequency range.

2 INTRODUCTION

The BLW898 is a bipolar linear power transistor designed to operate in the (470 – 860) MHz range. The transistor is encapsulated in a SOT171A 6-lead rectangular flange package with a ceramic cap, see Fig.1.

The specified output power is 3 W peak-sync in class-A. The intermodulation distortion level (IMD) < –63 dB (fvision = –8 dB, fsideband = –16 dB and fsound = –10 dB) and gain >10 dB at 860 MHz.

For application in TV transposers for Band IV/V (470 – 860) MHz a wideband linear power amplifier has been designed operating in class-A. It is suitable for driving higher power stages in TV-transposers.



Pinning

PIN	DESCRIPTION
1	emitter
2	emitter
3	base
4	collector
5	emitter
6	emitter

Fig.1 Simplified outline and symbol.

3 AMPLIFIER ELECTRICAL DESIGN OBJECTIVES

Electrical characteristics (Ths = 25 °C; 25 V; 1.1 A; (470 – 860) MHz).

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Transducer power gain (small signal)	Gp	10	–	–	dB
Gain ripple (small signal)	Gripple	–	–	±1	dB
Intermodulation (–8 dB/–16 dB/–7 dB, Peak-sync = 3 W; note 1	IMD1	–	–	–60	dB
Intermodulation (–8 dB/–16 dB/–10 dB, Peak-sync = 3 W; note 1	IMD2	–	–	–63	dB
Output return loss	ORL	–	–15	–	dB

Note

1. Peak-sync is a reference power level for TV-signals, in this case used for a 3 carrier signal.

4 DESIGN OF THE AMPLIFIER

The amplifier consists of a BLW898 plus an input and output matching circuit. The input is gradually mismatched and therefore not matched to 50 Ω. To obtain a good input matching a balanced circuit with two BLW898 transistor is necessary. A schematic diagram of the BLW898 amplifier is given in Fig.2. A components list is given in “Appendix 1”.

4.1 Mounting the transistor

For good thermal contact, heatsink compound should be used when mounting the transistor on a heatsink.

4.2 Positioning of the matching capacitors (see Figs 3 and 4)

Input:

The capacitors C4 + C5 are situated as close as possible near the transistor

The capacitors C2 + C3 are situated on a distance of approx. 19 mm from the transistor

The position of the ‘input’ capacitors influence the tuning for flat gain.

Output:

The capacitors C6 + C7 are situated on a distance of approx. 10.5 mm from the transistor

The capacitors C8 + C9 are situated on a distance of approx. 21 mm from the transistor

Capacitor C11 is placed approx. 11.5 mm from stripline L3

The position of the ‘output’ capacitors is critical to obtain the S22 contours as described in the amplifier tuning procedure.

Note:

- RF choke L6 is placed approx. 5 mm from the transistor base.
- Stripline L5 is situated 2.8 mm from the transistor and 2.8 mm from L4.

5 AMPLIFIER TUNING PROCEDURE

The amplifier is tuned under small signal conditions by means of a networkanalyzer. The amplifier is tuned for flat gain over the complete bandwidth (470 – 860) MHz. To obtain a flat gain, the input is gradually mismatched. The input returnloss S11 is the main parameter for setting the gain level and flatness.

Tuning of the output will mainly influence IMD and to a lesser extent the gain flatness.

To obtain a good IMD performance over the band it is recommended to follow the S22 tuning contours as plotted in Figs 5, 6 and 7.

An S22 of about –15 dB is required over the complete bandwidth.

6 AMPLIFIER PERFORMANCE

Broadband measurement data is presented in Figs 8, 9 and 10.
Gain/IMD are measured versus frequency (470 – 860) MHz and versus peak-sync level (at ch69).
Gain/IMD are given at two 3-tone systems:

- fv = –8 dB/fsb = –16 db/fs = –10 dB
- fv = –8 dB/fsb = –16 db/fs = –7 dB.

Figure 3 gives gain compression (CW) versus frequency.

At a nominal peak-sync level of 3 W for which the module is dimensioned the performance in the (470-860) MHz band is as follows:

- 3-tone system: (–8/–16/–7) dB; IMD ≤61 dB/gain >10 dB
- 3-tone system: (–8/–16/–10) dB; IMD ≤64 dB/gain >10 dB.

(for both systems ripple ≤1.5 dB)

7 CONCLUSION

A broadband amplifier is presented based on a BLW898, capable of operating in full band IV/V with flat gain and good linearity. Design and tuning procedure described result in good broadband behaviour.

A typ. gain of 10.5 dB with good linearity (peak-sync = 3 W @ –64 dB (–8/–16/–10) dB 3-tone system) has been obtained at the class-A bias point (25 V/1.1 A).

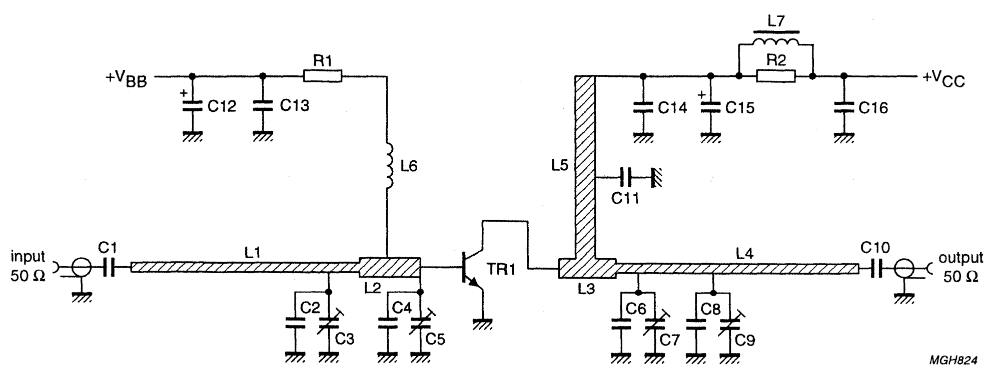


Fig.2 Schematic diagram of the BLW898 amplifier.

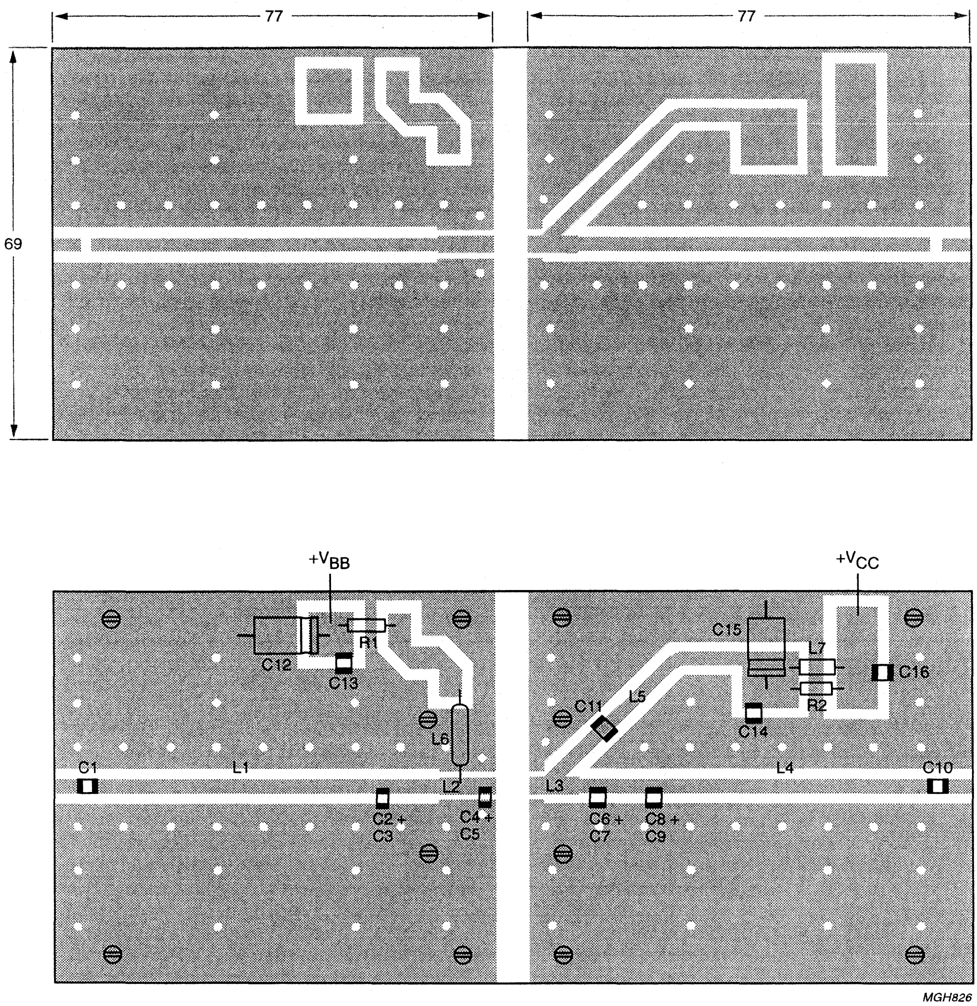


Fig.3 Component layout of the BLW898 amplifier.

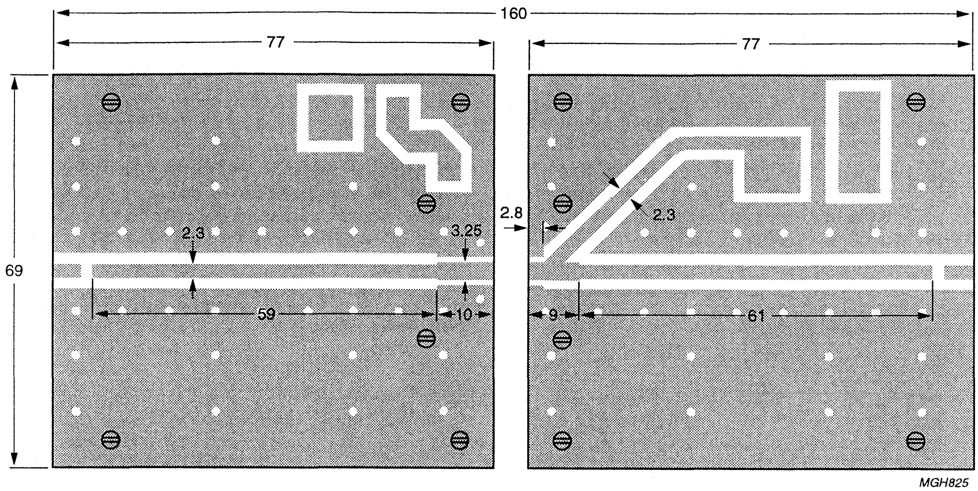
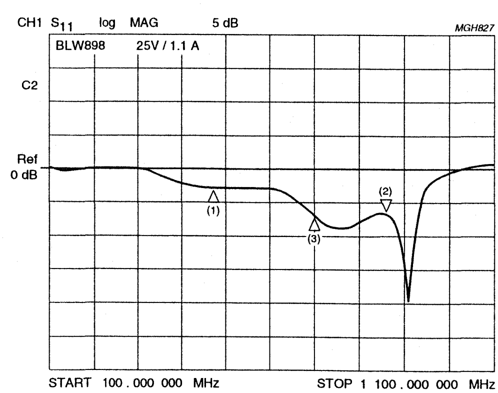
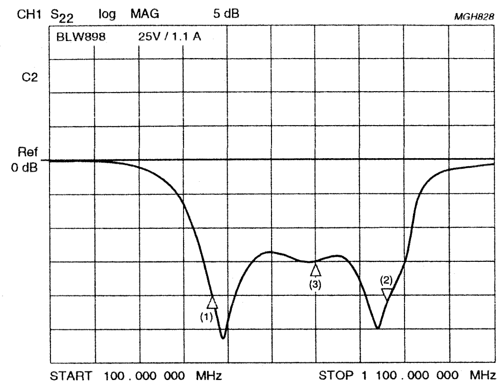


Fig.4 Dimensions of the BLW898 amplifier.



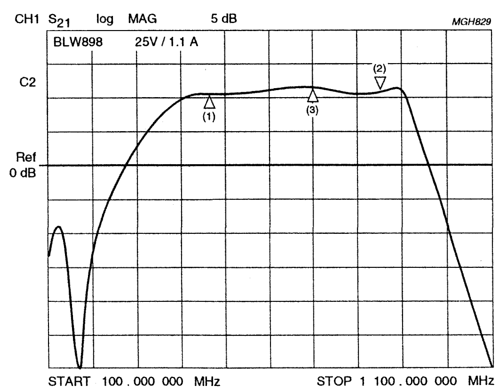
(1) 470 MHz; −3.0 dB.
(2) 600 MHz; −7.0 dB.
(3) 860 MHz; −7.0 dB.

Fig.5 Small signal results.



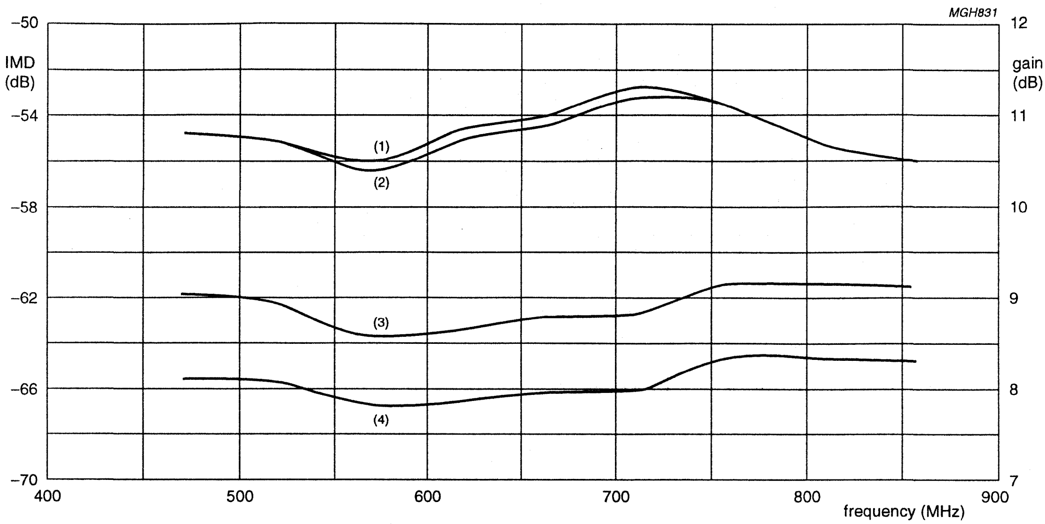
(1) 470 MHz; −20.8 dB.
(2) 600 MHz; −20.8 dB.
(3) 860 MHz; −15.0 dB.

Fig.6 Small signal results.

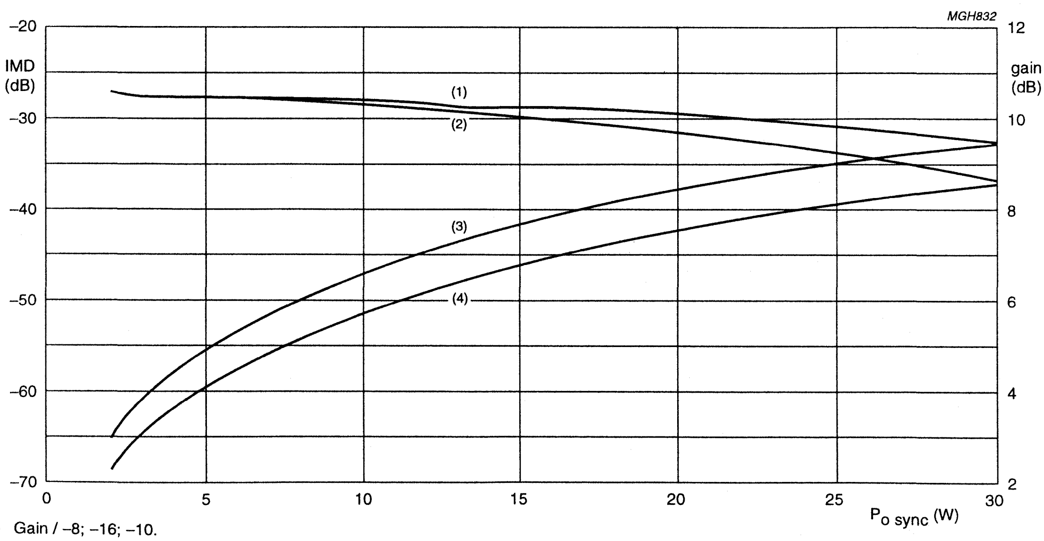


(1) 470 MHz; −10.5 dB.
(2) 600 MHz; −10.5 dB.
(3) 860 MHz; −11.3 dB.

Fig.7 Small signal results.

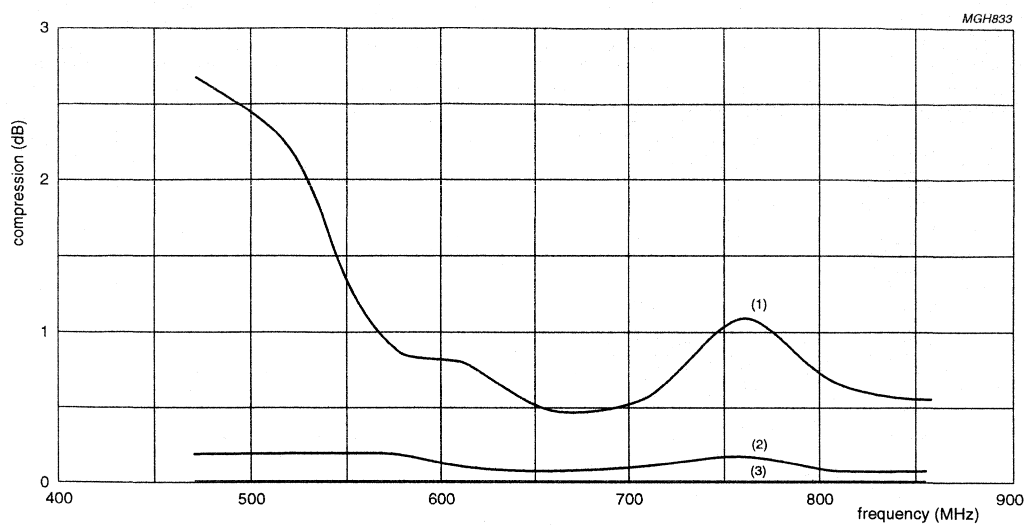


(1) Gain / −8; −16; −10.
(2) Gain / −8; −16; −7.
(3) IMD / −8; −16; −7.
(4) IMD / −8; −16; −10.



(1) Gain / −8; −16; −10.
(2) Gain / −8; −16; −7.
(3) IMD / −8; −16; −7.
(4) IMD / −8; −16; −10.

Fig.9 Demoboard BLW898; Gain/IMD vs Po_sync/Ths = 25 C; 25 V/1.1 A/ch69.



(1) PL = 1 W.
(2) PL = 5 W.
(3) PL = 10 W.

Fig.10 Demoboard BLW898; CW gain compression; 25 V/1.1 A/Ths = 25 C.

8 APPENDIX 1

Component list

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
C1	multilayer ceramic chip capacitor, note 1	11 pF	
C2	multilayer ceramic chip capacitor, note 1	1.5 p	
C3, C5, C7, C9	Tekelec Giga trimmer 37271	0.6 – 4.5 pF	
C4	multilayer ceramic chip capacitor, note 1	15 p	
C6	multilayer ceramic chip capacitor, note 1	7.5 p	
C8	multilayer ceramic chip capacitor, note 1	2.7 p	
C10	multilayer ceramic chip capacitor, note 1	5.1 p	
C11	multilayer ceramic chip capacitor, note 1	270 p	
C12, C15	solid aluminium capacitor	47 μF; 63 V	
C13, C14, C16	multilayer ceramic chip capacitor	10 n	0805
L1	stripline, note 2	2.3 × 59 mm	50 Ω
L2	stripline, note 2	3.25 × 10 mm	40 Ω
L3	stripline, note 2	3.25 × 9 mm	40 Ω
L4	stripline, note 2	2.3 × 61 mm	50 Ω
L5	stripline, note 2	2.3 × 41.5 mm	50 Ω
L6	RF choke	220 nH	
L7	grade 4S2 ferrocube wideband RF choke (12NC: 4330 030 36301)		
R1	metal film resistor	10 Ω; 0.6 W	
R2	metal film resistor	50 Ω; 0.6 W	

Notes

1. ATC capacitor type 100B or capacitor of same quality.
2. PCB manufacturer: Rogers Ultralam 2000 (BO300M1046QB) (ε_r = 2.55, thickness 0.76 mm), (stripline value: width × length).

A linear 20 W broadband amplifier for band IV/V TV transposers based on the BLV857

Application Note
AN98016

1 ABSTRACT

A broadband linear amplifier design is presented, suitable for application in TV transposers, operating in band IV and V (470 to 860) MHz. The design is based on two BLV857 bipolar transistors combined with quadrature hybrids. Typical results at the recommended class-A bias point (25.5 V/4.5 A) for the total module include a 3-tone IMD level of –54 dB (fvision = –8 dB, fsideband = –16 dB and fsound = –10 dB) and an average gain of 12 dB at 20 W peak-sync output power in the (470 to 860) MHz frequency range.

2 INTRODUCTION

The BLV857 is a bipolar linear push-pull power transistor designed to operate in the (470 to 860) MHz range. The transistor is encapsulated in a SOT324B 4-lead rectangular flange package with a ceramic cap, see the simplified outline and symbol below. The emitters are internally connected to the flange. The specified output power is 10 W peak-sync in class-A. The intermodulation distortion level (IMD) < –54 dB (fvision = –8 dB, fsideband = –16 dB and fsound = –10 dB) and gain >10 dB at 860 MHz. The main application is aimed at final stages of medium power TV transposers.

Pinning SOT324B

PIN	DESCRIPTION
1	collector 1
2	collector 2
3	base 1
4	base 2
5	emitter

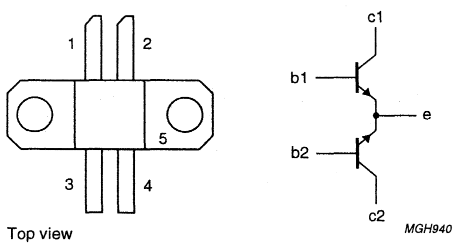


Fig.1 Simplified outline and symbol.

For application in TV transposers Band IV/V a wideband linear power amplifier has been designed with two BLV857 transistors operating in class-A.

3 AMPLIFIER ELECTRICAL DESIGN OBJECTIVES

The amplifier operates at a supply voltages of 25.5 V and a total current of 4.5 A (BLV857 operating point: Vce = 25V, Ic = 2.2A).

Electrical characteristics (Ths = 25 °C, 25.5 V, 4.5 A, (470 to 860) MHz)

	SYMBOL	MIN.	TYP.	MAX.	UNIT
Transducer power gain (small signal)	Gp	10	–	–	dB
Gain ripple (small signal)	Gripple	–	–	±1	dB
Intermodulation (–8 dB /–16 dB /–7 dB, Peak-sync = 20 W	IMD1	–	–	–51	dB
Intermodulation (–8 dB /–16 dB /–10 dB, Peak-sync = 20 W	IMD2	–	–	–54	dB
Input return loss/Output return loss	IRL/ORL	–	–	–15	dB

Note

1. Peak-sync is a reference power level for TV signals, in this case used for a 3 carrier signal.

4 DESIGN OF THE AMPLIFIER

The amplifier consists of 2 balanced circuit, both equipped with a BLV857 and coupled in parallel by means of a wideband 3 dB/90 degrees Sagewireline coupler at the input and output.

4.1 Mounting the transistors:

For good thermal contact, heatsink compound should be used when mounting the transistors on a heatsink.

4.2 Balun

Both input and output matching circuits of each BLV857 are connected to a coax balun which splits a 50 Ω unbalanced port in two 12.5 Ω ports. The balun has a transformation factor of 2. The electrical length of the coax line is 45 degrees at 860 MHz. The construction of the balun is described in “Appendix 4”. Essential for the balun is the short-circuit (at one side) between the inner and outerlead as can be seen in “Appendix 1” and “Appendix 2”.

4.3 Bias circuit: (“Appendix 1” and “Appendix 2”)

Each transistor has its own bias unit to obtain a stable DC setting. With the potentiometers P1 and P2 it is possible to adjust the collector current of both BLV857 transistors. The nominal collector current should be 2.2 A. The sense resistor in the collector branch is implemented as a folded printed line (L17). In this way we obtain a small sense resistor (approx. 80 mΩ) that can handle the dissipated power.

4.4 Positioning of the matching capacitors: (“Appendix 1” and “Appendix 2”)

Input: The capacitors C25 and C55 are situated on a distance of approx. 1 mm from the transistor. The capacitors C23, C24, C53 and C54 are situated on a distance of approx. 6 mm from the transistor. The capacitors C21, C22, C51 and C52 are situated as close as possible near the balun B1. The position of the ‘input’ capacitors influence the tuning for flat gain.

Output: The capacitors C26, C27, C56 and C57 are situated on a distance of approx. 8 mm from the transistor. The capacitors C28, C29, C58 and C59 are situated as close as possible near the balun B2. The position of the 'output' capacitors is critical to obtain the S22 contours as described in the amplifier tuning procedure.

4.5 Amplifier tuning procedure: ("Appendix 6" and "Appendix 7")

Both amplifiers are separately tuned under small signal conditions by means of a networkanalyzer. The amplifiers are tuned for flat gain over the complete bandwidth (470 to 860) MHz. To obtain a flat gain the input is gradually mismatched. The input returnloss S11 is the main parameter for setting the gain level and flatness.

Tuning of the output will mainly influence IMD and to a lesser extent the gain flatness. To obtain a good IMD performance over the band it is recommended to follow the S22 tuning contours (of a single amplifier) as plotted in "Appendix 6". An S22 of −15 to −20 dB is required over the complete bandwidth.

After individual tuning, both amplifiers can be coupled and the load resistors can be attached. The module is now ready for use and the complete characterization can be started. "Appendix 7" shows the small signal characterization of the complete demo amplifier.

4.6 Amplifier performance

Broadband measurement data are presented in Figs 1 to 4 of "Appendix 8". Gain / IMD are measured versus frequency (470 to 860) MHz and versus peak-sync level (at ch69). Gain / IMD are given at two 3-tone systems:

- fv = −8 dB / fsb = −16 dB / fs = −10 dB
- fv = −8 dB / fsb = −16 dB / fs = −7 dB.

Figure 4 gives gain compression (CW) versus frequency.

When coupling the amplifiers a degradation in powergain and IMD can be expected (see also Fig.2 in "Appendix 8", gain/IMD of a separate amplifier). Reason: extra insertion loss, amplitude and phase imbalances in the couplers/transistors, detuning of the transistor load by the non ideal coupler impedance. Over the complete frequency band, a degradation of about 0.5 dB in gain and 2 dB in IMD has been noted. The IMD level at the highest frequencies is just within specification of the −8, −16 and −10 3-tone system. If more margin on the IMD spec is required an exchange between gain and IMD is possible.

At a nominal peak-sync level of 20 W for which the module is dimensioned performance in the (470 to 860) MHz band is as follows:

- 3 tone system: (−8/−16/−7) dB: IMD ≤50 dB / gain >11.5 dB
- 3 tone system: (−8/−16/−10) dB: IMD ≤50 dB / gain >11.5 dB.

(For both systems ripple ≤1.5 dB)

5 CONCLUSION

A complete transposer module is presented based on two BLV857, capable of operating in full band IV/V with flat gain good linearity. Design and tuning procedure described results in good broadband behaviour. A typ. gain of 12 dB with good broadband behaviour. A typ. gain of 12 dB with good linearity (peak-sync = 20 W @ −54 dB (−8/−16/−10) dB 3-tone system) has been obtained at the class-A bias point (25.5 V/4.5 A).

6 APPENDICES

1. Schematic diagram of the BLV857 demo amplifier
2. Component layout of the BLV857 demo amplifier
3. Dimensions of the BLV857 demo amplifier PCB
4. Construction instructions of the balun

5. PCB layout of the frontside and the backside
6. Small signal results of a separated amplifier
7. Small signal results of the complete demo amplifier
8. Fig.1: Gain/IMD vs frequency of a separate amplifier (10 W peak-sync.)
   Fig.2: Gain/IMD vs frequency of a complete demo amplifier (20 W peak-sync.)
   Fig.3: Gain/IMD vs peak-sync at ch69 of a complete demo amplifier
   Fig.4: Gain compression (CW) vs frequency (complete demo amplifier)
9. Components list.

7 APPENDIX 1

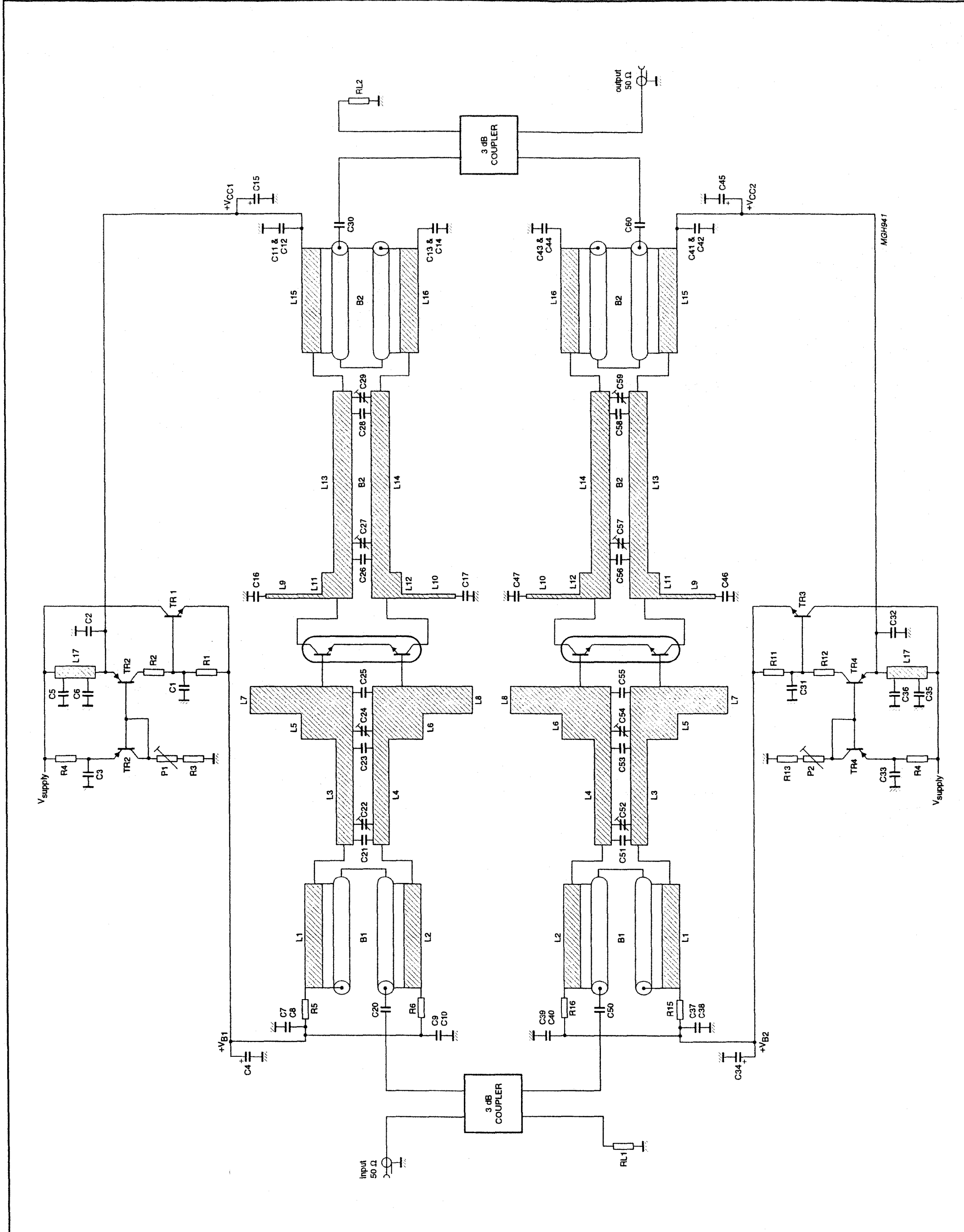


Fig.2 Schematic diagram of the BLV857 demo amplifier.

8 APPENDIX 2

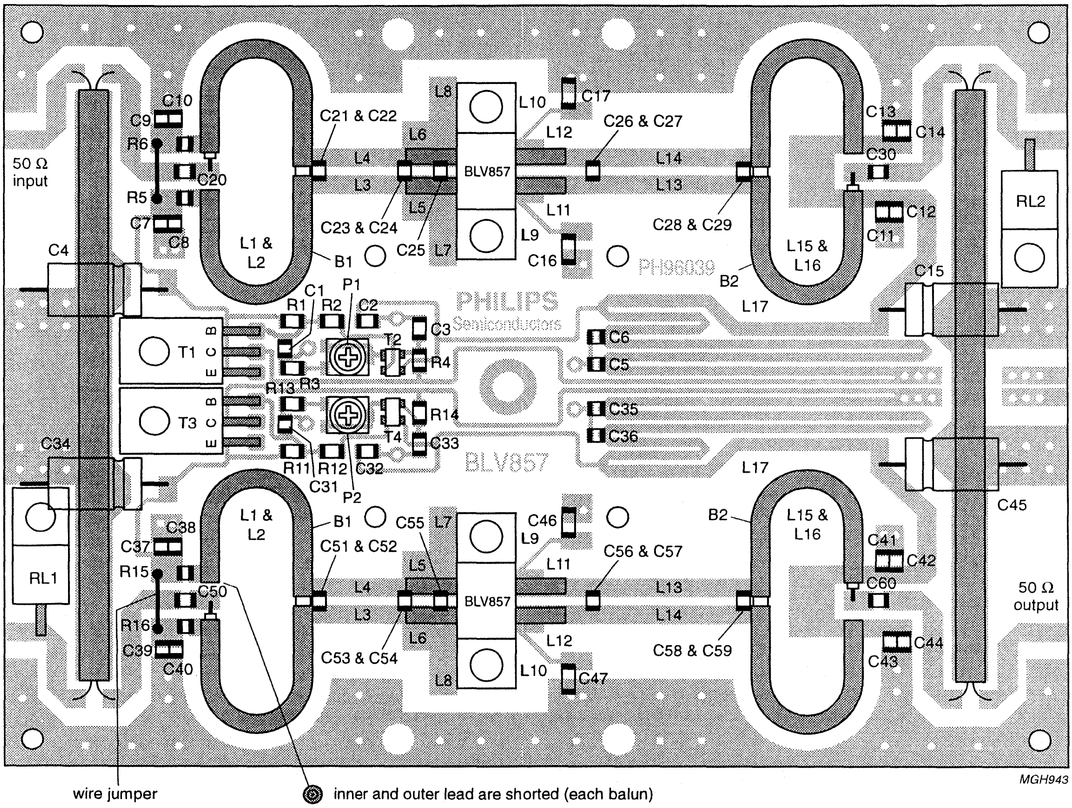


Fig.3 Component layout of the BLV857 demo amplifier.

9 APPENDIX 3

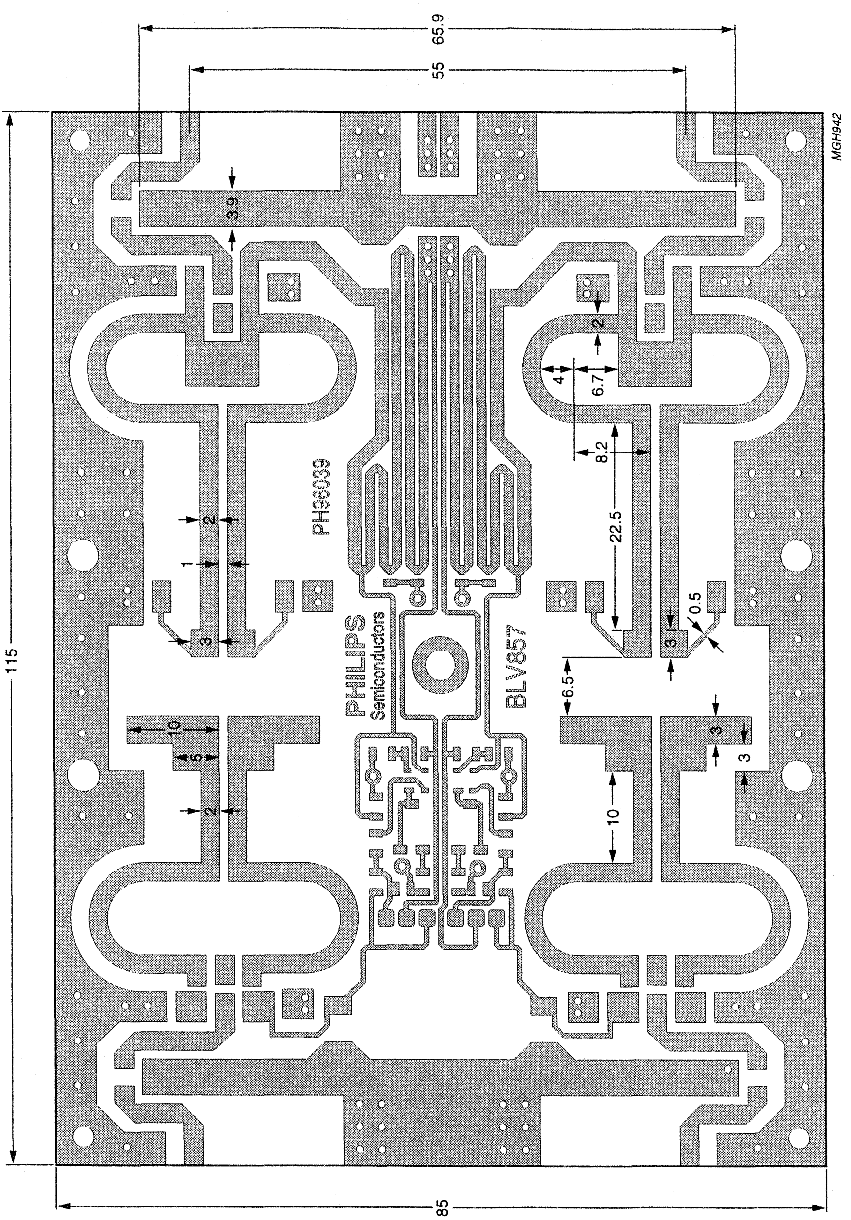
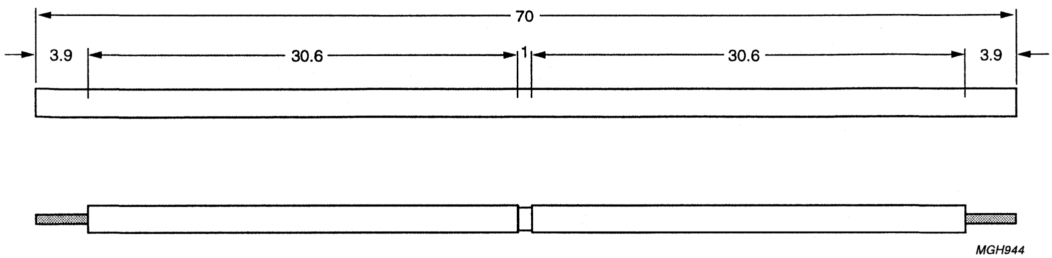


Fig.4 Dimensions of the BLV857 demo amplifier PCB.

Dimensions in mm.

10 APPENDIX 4

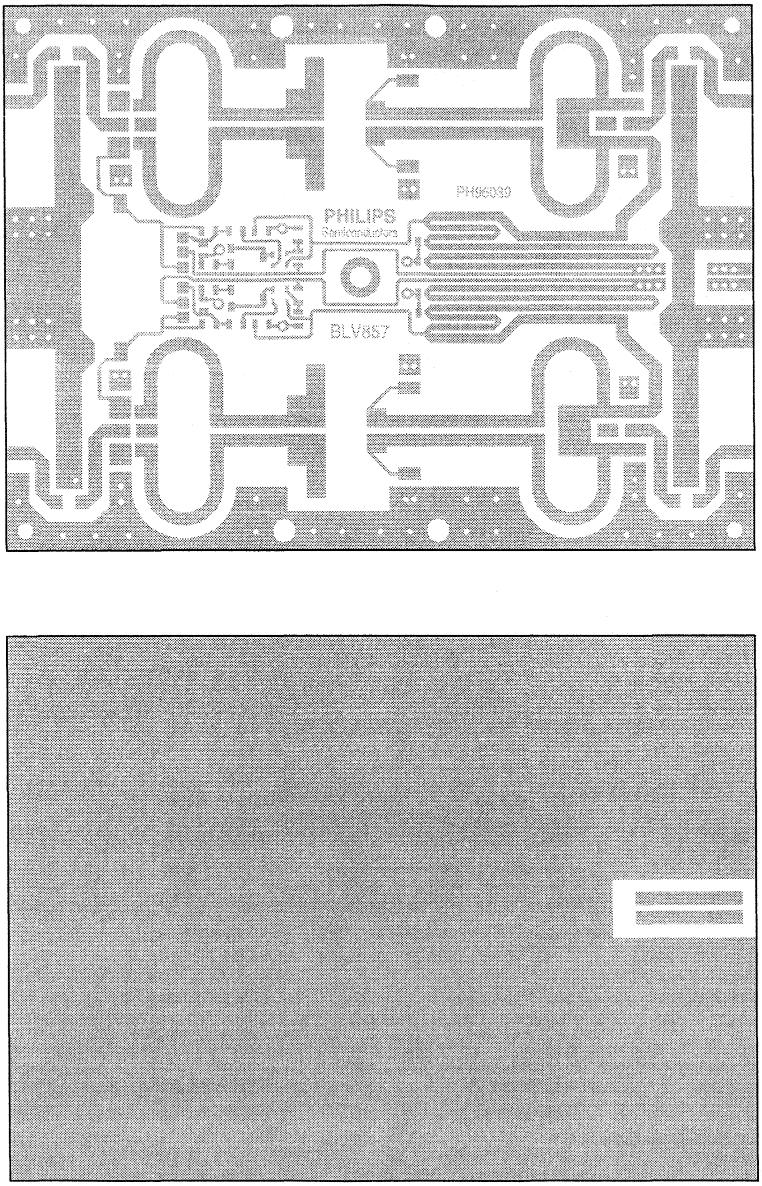
BLV857 amplifier balun construction



Dimensions in mm.

Fig.5 Construction instructions of the balun.

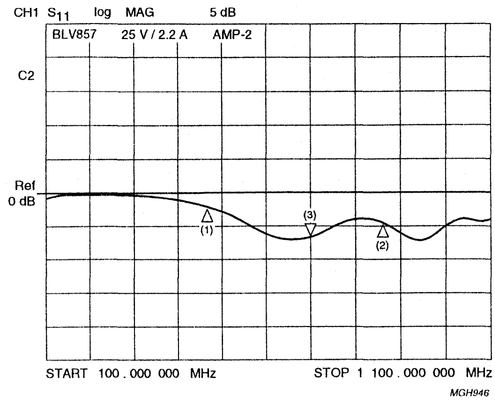
11 APPENDIX 5



MGH945

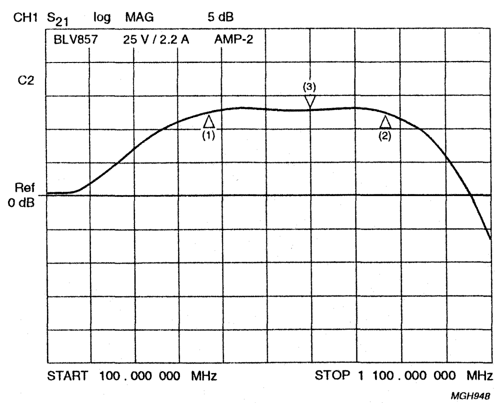
Fig.6 PCB lay out frontside and backside.

12 APPENDIX 6



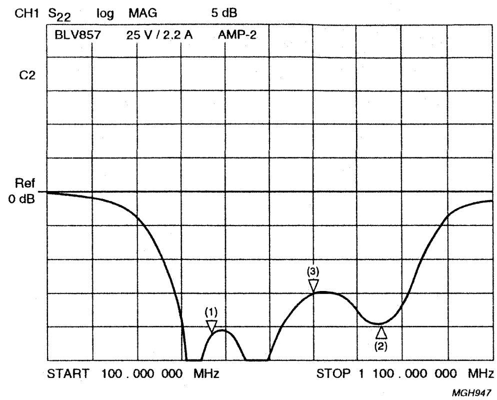
(1) 471 MHz.
(2) 700 MHz.
(3) 855 MHz.

Fig.7 Small signal results of a separated amplifier; a.



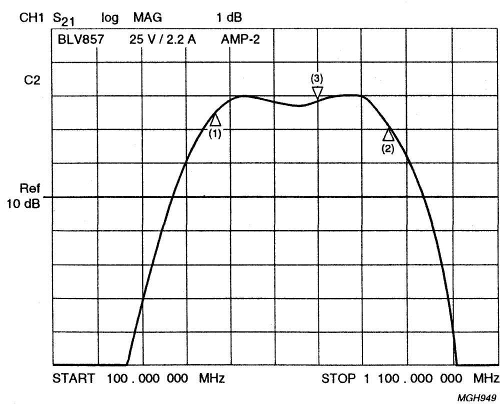
(1) 471 MHz.
(2) 700 MHz.
(3) 855 MHz.

Fig.8 Small signal results of a separated amplifier; b.



(1) 471 MHz.
(2) 700 MHz.
(3) 855 MHz.

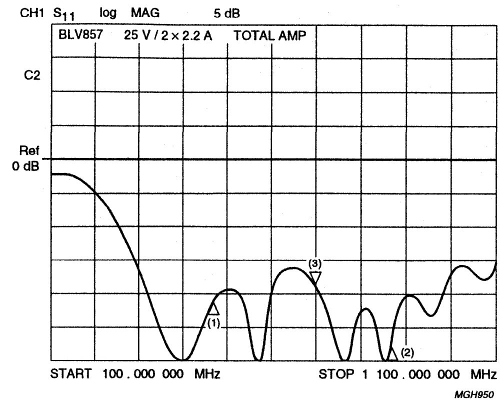
Fig.9 Small signal results of a separated amplifier; c.



(1) 471 MHz.
(2) 700 MHz.
(3) 855 MHz.

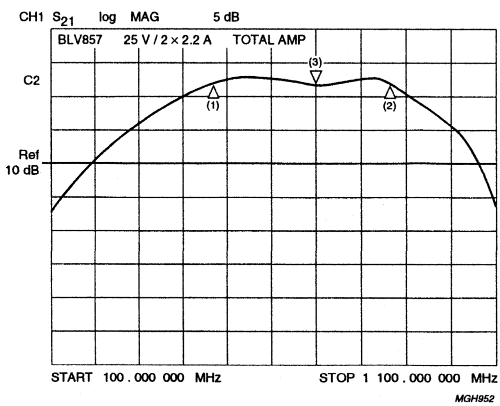
Fig.10 Small signal results of a separated amplifier; d.

13 APPENDIX 7



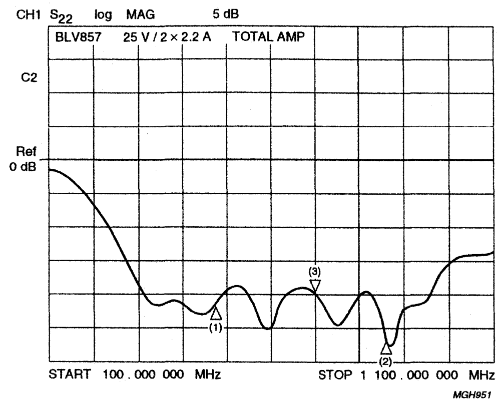
(1) 471 MHz.
(2) 700 MHz.
(3) 855 MHz.

Fig.11 Small signal results of the complete; a.



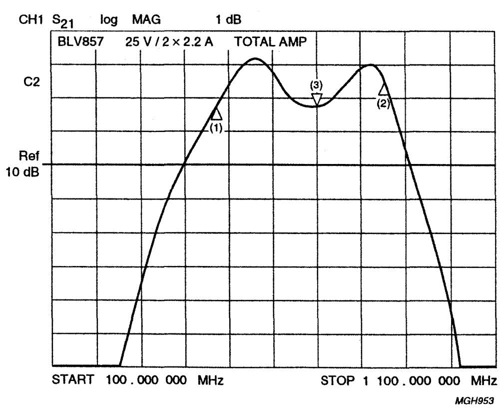
(1) 471 MHz.
(2) 700 MHz.
(3) 855 MHz.

Fig.12 Small signal results of the complete; b.



(1) 471 MHz.
(2) 700 MHz.
(3) 855 MHz.

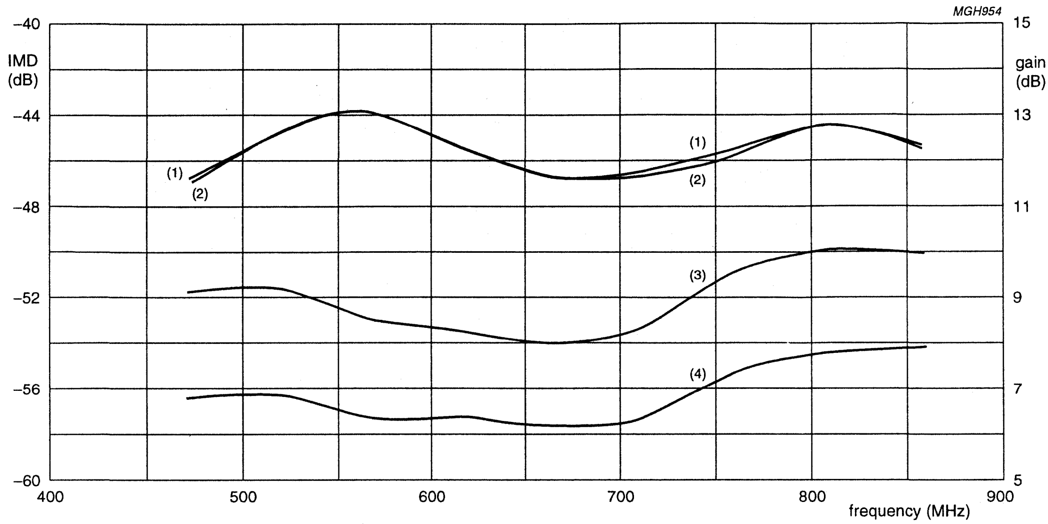
Fig.13 Small signal results of the complete; c.



(1) 471 MHz.
(2) 700 MHz.
(3) 855 MHz.

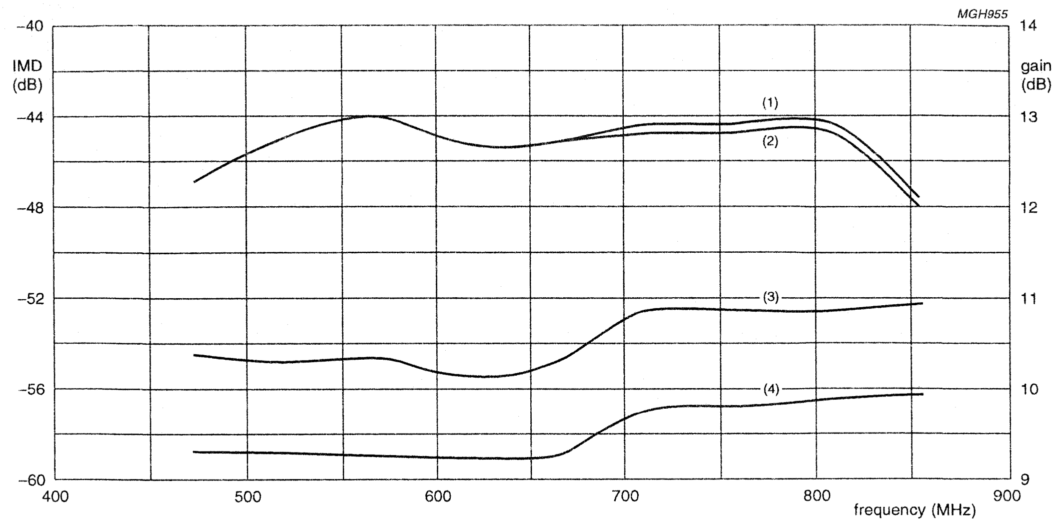
Fig.14 Small signal results of the complete; d.

14 APPENDIX 8



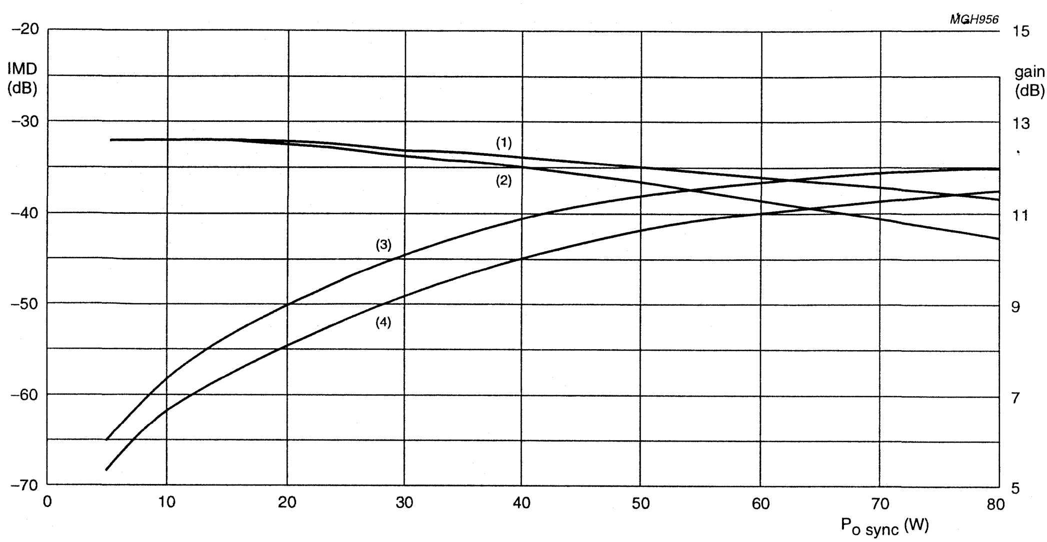
(1) Gain 3-tone system; −8, −16 and −10.
(2) Gain 3-tone system; −8, −16 and −7.
(3) IMD 3-tone system; −8, −16 and −7.
(4) IMD 3-tone system; −8, −16 and −10.

Fig.15 Demo amplifier 2× BLV857 IMD/Gain vs Freq/Ths = 25 C; 25 V/2 × 2.2 A/Po_sync = 20 W.



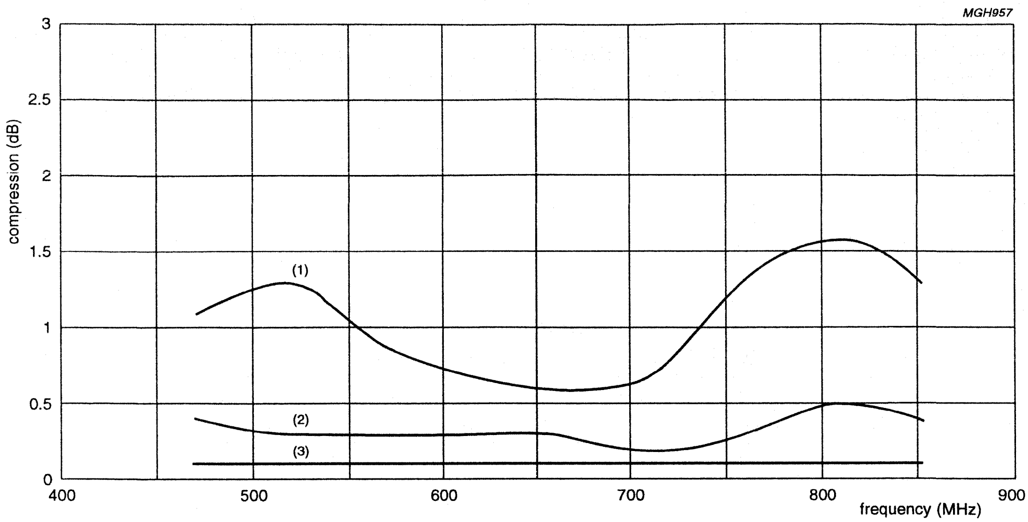
(1) Gain 3-tone system; −8, −16 and −10.
(2) Gain 3-tone system; −8, −16 and −7.
(3) IMD 3-tone system; −8, −16 and −7.
(4) IMD 3-tone system; −8, −16 and −10.

Fig.16 Demo amplifier 2× BLV857 CW gain compression 25 V/2.2 A/THs = 25C.



(1) Gain 3-tone system; –8, –16 and –10.
(2) Gain 3-tone system; –8, –16 and –7.
(3) IMD 3-tone system; –8, –16 and –7.
(4) IMD 3-tone system; –8, –16 and –10.

Fig.17 Demo amplifier 2× BLV857 IMD/Gain vs Po_sync; 25 V/2 × 2.2 A/ch69/THs = 25C.



(1) Gain compression; Po = 10 W.
(2) Gain compression; Po = 20 W.
(3) Gain compression; Po = 30 W.

Fig.18 Demo amplifier 2× BLV857 CW gain compression 25 V/2.2 A/THs = 25 C.

15 APPENDIX 9

Component list

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C31, C32, C33, C34, C35, C36, C37, C38, C39 and C40	multilayer ceramic chip capacitor	10 nF	0805
C4 and C34	solid aluminium capacitor	25 V; 4.7μF	
C11, C12, C13, C14, C16, C17, C41, C42, C43, C44, C46 and C47	multilayer ceramic chip capacitor	100 nF	1206
C15 and C45	solid aluminium capacitor	63 V; 10 μF	
C20 and C50	multilayer ceramic chip capacitor, note 1	47 pF	
C30 and C60	multilayer ceramic chip capacitor, note 1	100 pF	
C21 and C51	multilayer ceramic chip capacitor, note 1	9.1 pF	
C22, C23, C52 and C53	Tekelec Giga trimmer 37271	0.6 to 4.5 pF	
C24 and C54	multilayer ceramic chip capacitor, note 1	3.0 pF	
C25 and C55	multilayer ceramic chip capacitor, note 1	15 pF	
C26 and C56	multilayer ceramic chip capacitor, note 1	11 pF	
C27, C28, C57 and C58	Tekelec Giga trimmer 37271	0.6 to 4.5pF	
C29 and C59	multilayer ceramic chip capacitor, note 1	9.1 pF	
L1, L2, L15 and L16	stripline, note 2	50 Ω	2 × 30.6 mm
L3 and L4	stripline, note 2	50 Ω	2 × 10 mm
L5 and L6	stripline, note 2	26.5 Ω	5 × 3 mm
L7 and L8	stripline, note 2	15 Ω	10 × 3 mm
L9 and L10	stripline, note 2	104 Ω	0.5 × 6 mm
L11 and L12	stripline, note 2	38.8 Ω	3 × 3 mm
L13 and L14	stripline, note 2	50 Ω	2 × 22.5 mm
L17	stripline, note 2	76.2 Ω	1 × 120 mm
B1 and B2	semi rigid coax balun UT70-25	25 Ω	70 mm
T1 and T3	NPN transistor	BD139	
T2 and T4	double PNP transistor	BVC62	
R1 and R11	SMD resistor	220 Ω	0805
R2 and R12	SMD resistor	1.8 Ω	0805
R3 and R13	SMD resistor	4.3 Ω	0805
R4 and R14	SMD resistor	33 Ω	0805

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
R5, R6, R15 and R16	SMD resistor	3.3 Ω	0805
P1 and P2	potmeter	2 kΩ	
RL1 and RL2	load resistor	50 Ω/30 W	

Notes

1. ATC capacitor type 100A or capacitor of some quality.
2. PCB manufactorer: Rogers Ultralam 2000.
   ε_r = 2.55, thickness 0.76 mm.
   Stripline value: width × length.
3. 3 dB/90 degrees wireline coupler: Sage Laboratories BHCb2-50.

A linear broadband 12 W amplifier for band IV/V TV transposers based on the BLV58

Application Note
AN98028

1 ABSTRACT

A broadband linear amplifier design is presented, suitable for application in TV transposers operating in bands IV and V (470 – 860 MHz). The design is based on a single BLV58 bipolar transistor in push pull configuration. Results at the published class A bias point (25 V/3.2 A) for the BLV58 include 12 W peak sync output power at –52 dB three tone IMD level and 11 dB gain in the (470 – 860) MHz range. Po-sync level improved by 4 W at 26 V/3.8 A.

2 INTRODUCTION

For solid state TV transposers Philips introduced the BLV58, a bipolar linear push-pull power transistor designed to operate in the 470 – 860 MHz range. Narrowband intermodulation distortion level is < –45 dB and powergain >10 dB at 860 MHz.

In this application note an amplifier design is to be discussed which demonstrates the broadband capabilities of a BLV58 in push-pull configuration. Special attention is paid to the broadband tuning procedure for good and reproducible linearity. Fullband performance data are presented measured with two different 3-tone systems at two bias levels.

3 GENERAL CONSIDERATIONS

UHF solid state TV transposers for service in band 4 and 5 are commonly realized using broadband amplifiers which are capable to handle both bands. The typical frequency range is 470 – 860 MHz or channel 21 to 69. Some transposers also service additional channel at the high end of band V. But these are quite rare. High powers are obtained by combining power from several lower power modules. The basic low power module consists of two push-pull amplifier combined using 3 dB quadrature hybrids. The push-pull amplifier is designed for flat gain response by allowing input mismatch which gradually improves with frequency. To have good input return loss throughout the band two of these push-pull amplifiers are combined using 3 dB quadrature hybrids.

Low and flat intermodulation distortion (IMD) is required throughout the band. As linearity performance is strongly determined by the collector loading, special attention must be paid to the tuning procedure for obtaining minimum and reproducible IMD response.

The class-A bias point used for this design is that published in the datasheet. However broadband performance has been evaluated at elevated bias levels within the DC safe operating area. Some means of bias temperature compensation is applied to achieve thermal stability.

4 AMPLIFIER DESCRIPTION

Figure 1 shows the schematic of the total push pull amplifier without the biasing circuitry. It utilizes mixed lumped and distributed low pass/high pass impedance matching sections for maximum bandwidth. The low pass sections consists of shunt capacitors and series transmission lines. The high pass sections consist of series capacitors and short circuited stubs. The stubs also form a part of the balance to unbalance(balun) transformers. The length of the stubs is less than 1/8 wavelength at 470 MHz. Balance is maintained by loading both the outer and inner conductors with identical stubs. The series capacitors also act as DC blocking.

The board material used for this amplifier is ULTRALAM 2000 from ROGERS Corp. which has a good price/performance ratio and good mechanical stability. It is a PTFE based substrate with $\varepsilon_r = 2.55$ and 30 mils (0.76 mm) thickness.

The printed-circuit board layout is shown in Figs 2 and 3 shows the component layout diagram. The list of components is given on page 7.

5 LOAD NETWORK DESIGN

The theoretical design was based on load impedance data from the datasheet. The conjugate of the broadband load impedance for one section was modelled as shown in Fig.4. R represents the load resistance to obtain good linearity, C the effective output capacitance of the transistor and L the bonding wires and package lead inductance.

With the component values given in Fig.4 a good broadband fit is obtained with the published load impedance. Minimum distortion is obtained when the effective load impedance presented to the chip is real or nearly real as possible.

A semi-low pass Chebychev matching network with three sections combined with a single high pass section is used to match R to 25 Ω. C and L of the model are absorbed in the matching network forming one section of the low pass. The initial component values were optimized for good full band match using CAD techniques.

6 INPUT NETWORK DESIGN

For achieving gain versus frequency levelling a lossless impedance matching network is applied which provide variation of reflected input power as a function of frequency. The BLV58 exhibit an approximate –4 dB per octave powergain roll off in the frequency range of interest. As solving the problem of impedance matching with drive compensation for gain levelling is difficult to solve analytical, CAD techniques were used to solve the problem. The initial low pass/high pass matching network for the input was first designed to have perfect match at the highest frequency of band V. With the component values found a computer optimization run was done to find the right values which provide the appropriate mismatch versus frequency while maintaining the best match at the highest frequency.

In order to get rid of the mismatch seen by the driver, two stages combined using 3 dB quadrature hybrids can be used which will result in minimum mismatch versus frequency. For evaluation of the single stage amplifier design a 3-port circulator was used to isolate the drive from the reflective input.

7 BIASING

The bias network were designed for spurious free operation. For stability in the low MHz region, basebias to collectorbias coil inductance ratio was chosen high. The minimum ratio strongly depending on Hfe, Cob and Ce of the device is approximately 1.5 for the BLV58. A transmission line stub is used for the collectorbias and a microchoke for the basebias. RF decoupling capacitors are added to provide low impedance to ground for all frequency components. Linearity is affected slightly by this in a positive way.

A bias circuit which achieves thermal stability through feedback techniques is used. The circuit applied is shown in Fig.6. The PNP(Q1) acts as a current source for the base of the BLV58. R1 controls the collector current drawn by the BLV58 and R2 sets the minimum of it. R3 establishes the operating bias point of the PNP. R4 sets the collector current drawn by the BLV58. R5 reduces the power dissipation in the PNP by taking a large part of the voltage drop across it. R6 reduces the effects of leakage current on the bias of the RF device. The diode (D1) thermally compensates the PNP's base-emitter voltage. A major part of the power consumption is concentrated in R4. The voltage drop across R4 should therefore be minimized (<1 V).

8 AMPLIFIER TUNING

Amplifiers with linearity requirements can be tuned in two ways. Although it will not always result in minimum distortion the first method optimizes for broadband gain using small signal techniques.

In the second method, loading for minimum distortion is emphasized. The tuning procedure adopted for this design consists of two phases. First the output network is tuned for the correct load impedance. Secondly the input network is tuned to obtain flat gain with the previously obtained load fixed. This off course will not necessarily results in the highest possible broadband gain obtainable from the device. The BLV58 requires a slightly different load impedance for minimum distortion than for maximum gain. The tuning procedure used is described below.

To obtain collector load tuning for minimum distortion a passive device(dummy) is used which represents the conjugate of the load as shown in Fig.4. Figure 5 shows the practical realization of the dummy device. An empty package of the BLV58 (SOT289) serves as carrier for the chip components R and C. Part of the printed line on the BeO die together with the collector leads form the required inductor L. The IMD performance of the BLV58 in a narrowband 860 MHz circuit, tuned with this dummy, was excellent. By inserting the dummy in place of the BLV58 without any voltages applied, the output network was tuned for minimum returnloss on small signal basis. After some practical optimization of the initial output network, the result obtained was as shown in Fig.4. Returnloss is better than –12 dB throughout the band and was considered the best obtainable with the applied matching technique. For the remaining part of the tuning procedure the output was not altered anymore. After replacing the dummy with a BLV58 biased into class-A, the complete amplifier was tuned for flat small signal gain by means of the input network only. Again some optimization of the input network was required too, to obtain the result as shown in Fig.9. The small signal gain is better than 11 dB throughout the band with a 0.6 dB ripple. Figure 10 contains the input response showing the mismatch versus frequency for gain levelling.

The output response is shown in Fig.7. A slightly increased bandwidth at the cost of inband returnloss is observed.

9 AMPLIFIER PERFORMANCE

The first class-A bias point for linearity evaluation was taken from the datasheet, i.e. V_{CE} = 25 V and I_{CQ} = 3.2 A. Based on the maximum published junction to case thermal resistance of 1.5 K/W, the maximum case temperature for zero RF drive is 80 °C. Improved linearity can be obtained at higher levels of collector voltage and current as long as the ratings (V_{CEmax} = 27 V and IC_{max} = 4 A) are not exceeded. As an example linearity has also been measured at V_{CE} = 26 V and I_{CQ} = 3.8 A. Maximum case temperature for zero drive at this bias point is 52 °C.

Linearity evaluation is done by comparing the intermodulation distortion products (IMD's) generated by a multi-tone test signal to a given reference level. Three tones are used to simulate television signals according two specifications for tone levels and spacings. The first is according the old German Post Office (GPO) specification, given in Fig.11, and the second according the new specification, given in Fig.12. The latter results in a somewhat lower Po-sync at same IMD level.

The test setup used for linearity evaluation is shown in Fig.13. To obtain good accuracy, the test signal must have a superior IMD to the levels to be measured. This has been achieved by amplifying each tone separately before combining them. Good isolation between the individual tones is obtained by using circulators as depicted in Fig.13. An additional circulator is added to isolate the drive from the reflective input of the amplifier.

Broadband measurement data are presented in the graphs of Figs 14 to 21. IMD and powergain are given at several output power levels to accommodate performance assessment for specific power levels. At an IMD level of –52 dB commonly specified for transposers, output power levels are as listed below (interpolated values):

1. 3-tones: –8/–16/–7 dB
   a) Po-sync ≥ 12 W @ 25 V/3.2 A
   b) Po-sync ≥ 16 W @ 26 V/3.8 A
2. 3-tones: –3/–20/–10 dB
   a) Po-sync ≥ 11 W @ 25 V/3.2 A
   b) Po-sync ≥ 15 W @ 26 V/3.8 A

So, Po-sync increases by 4 W typically or the second bias point and decreases by 1 W for the new tone specification. The power gain is approximately 11 dB for both cases with a ripple of 0.5 dB. Less gain compression is observed for the second bias point.

10 CONCLUSION

An amplifier design has been presented based on a single BLV58, capable of operating in full band IV/V with flat gain and good linearity. Design and tuning procedure described result in good and reproducible broadband behaviour. High gain (11 dB) and good linearity (Po-sync ≥ 12 W @ –52 dB) has been obtained at the published class-A bias point (25 V/3.2 A). At a higher bias point (26 V/3.8 A). Po-sync improves by 4 W.

A linear broadband 12 W amplifier for band IV/V TV transposers based on the BLV58

Application Note
AN98028

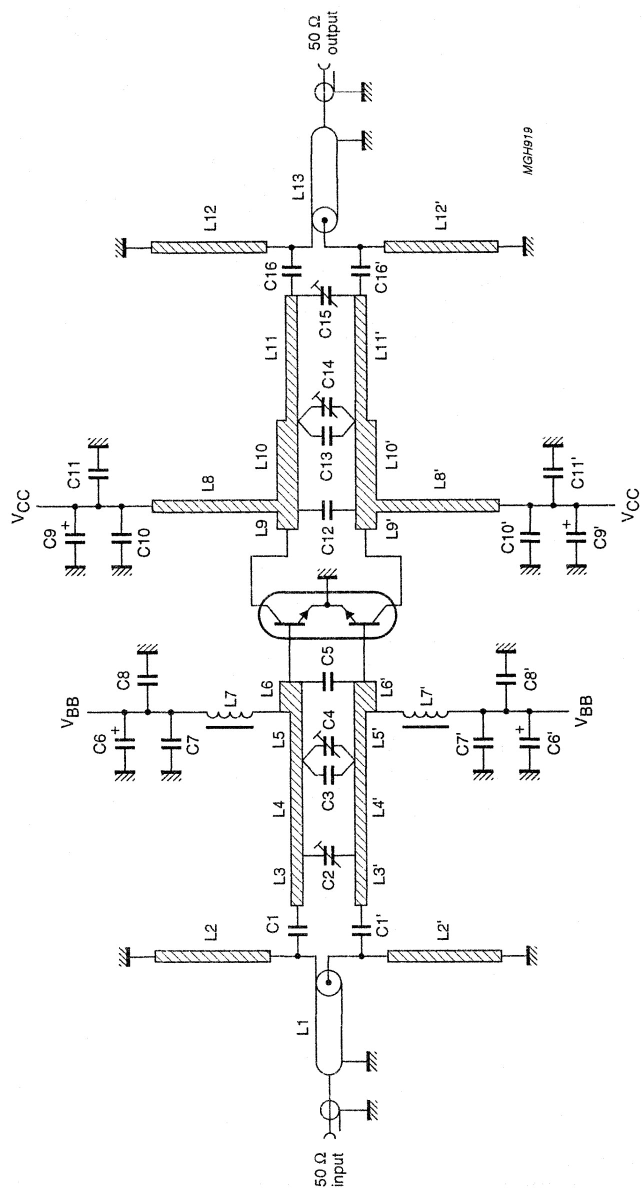


Fig.1 Circuit Diagram of Broadband Amplifier.

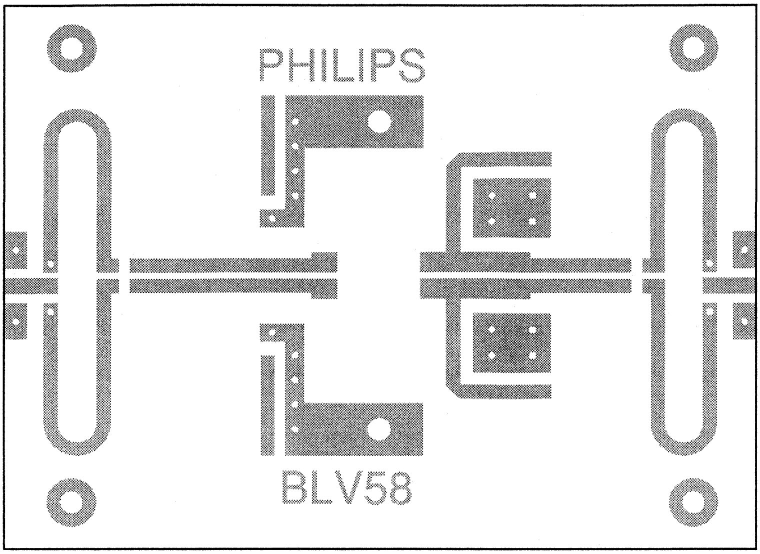


Fig.2 PC Board Layout (Not to Scale).

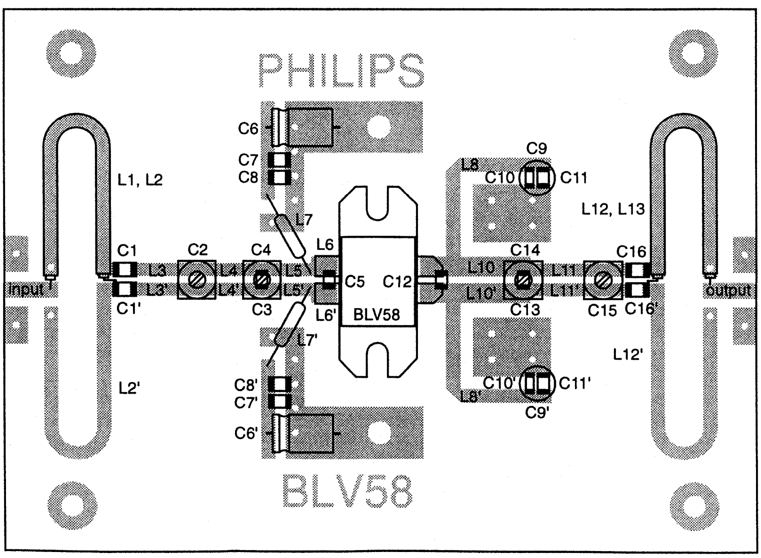


Fig.3 Component Layout Diagram.

11 LIST OF COMPONENTS BLV58 BROADBAND AMPLIFIER

Capacitors

C1 = C1'	11	pF	ATC 100B chip capacitor
C2 = C4 = C14 = C15	1.2 – 3.5	pF	Philips film dielectric trimmer
C3 = C13	6.8	pF	ATC 100A chip capacitor
C5	13	pF	ATC 100A chip capacitor
C6 = C6'	10	μF	63 V electrolytic capacitor
C7 = C7' = C10 = C10'	100	nF	Philips chip capacitor
C8 = C8' = C11 = C11'	100	pF	ATC 100B chip capacitor
C9 = C9'	2.2	μF	63 V electrolytic chip capacitor
C12	18	pF	ATC 100A chip capacitor
C16 = C16'	10	pF	ATC 100B chip capacitor

Transmission-lines/inductors

L1 = L13	50	Ω	Semi-Rigid Coax: L = 50 mm; OD = 2.2 m
L2 = L2' = L12 = L12'	53	Ω	Stripline: L = 50 mm; W = 1.9 mm
L3 = L3'	61	Ω	Stripline: L = 11.2 mm; W = 1.5 mm
L4 = L4'	61	Ω	Stripline: L = 10.5 mm; W = 1.5 mm
L5 = L5'	61	Ω	Stripline: L = 6.3 mm; W = 1.5 mm
L6 = L6'	41	Ω	Stripline: L = 3.7 mm; W = 2.8 mm

L7 = L7'	470	nH	RF micro-choke
L8 = L8'	53	Ω	Stripline: L = 28 mm; W = 1.9 mm
L9 = L9'	41	Ω	Stripline: L = 3.5 mm; W = 2.8 mm
L10 = L10'	41	Ω	Stripline: L = 12 mm; W = 2.8 mm
L11 = L11'	61	Ω	Stripline: L = 12.5 mm; W = 1.5 mm

Coaxal Lines L1 and L13 are soldered on striplines L2 and L12 respectively. The same lengths of coaxial lines (centre conductor unused) are soldered on L2' and L12' respectively. It results in a lower characteristic impedance of the striplines, due to the increased effective thickness. The initial value of 53 Ω decreases the approximately 44 Ω.

PCB: ULTRALAM 2000, thickness = 30 mils, ε_r = 2.55.

The back side of the board is fully metallized and serves as ground plane. Plated through holes are used for grounding areas on the top side.

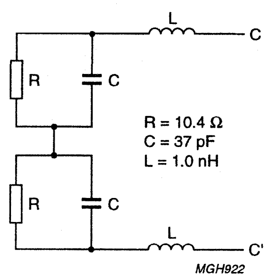


Fig.4 Equivalent Model for the Conjugate of the Load Impedance (Collector to Collector).

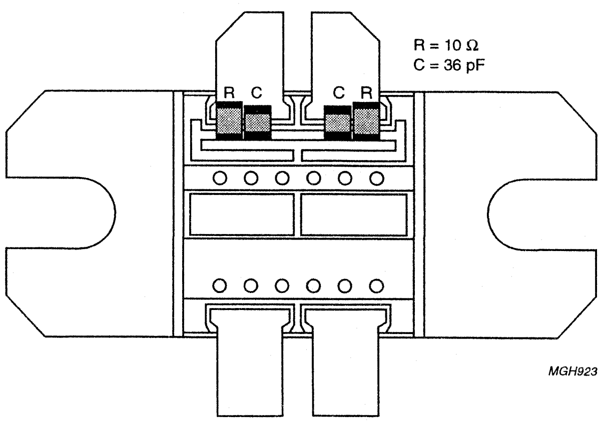


Fig.5 Passive Device (Dummy) for Load Tuning.

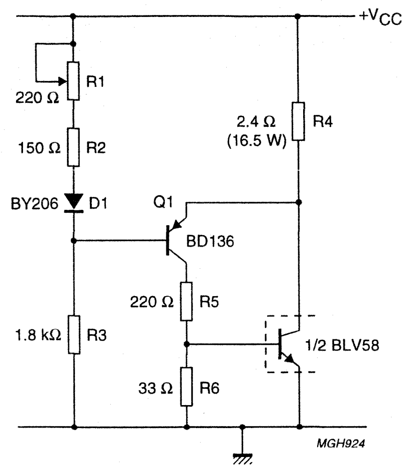
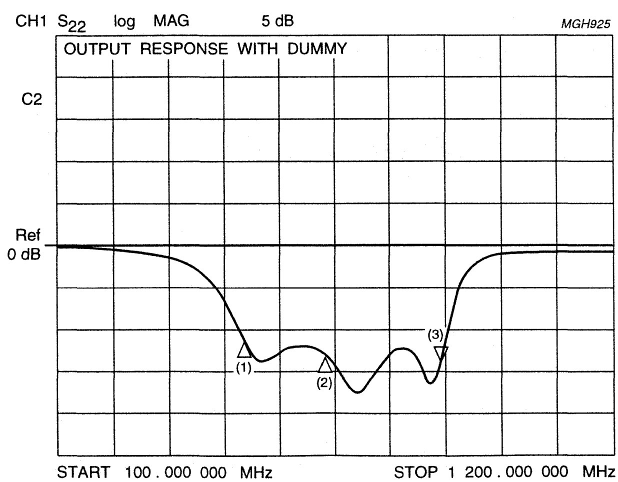
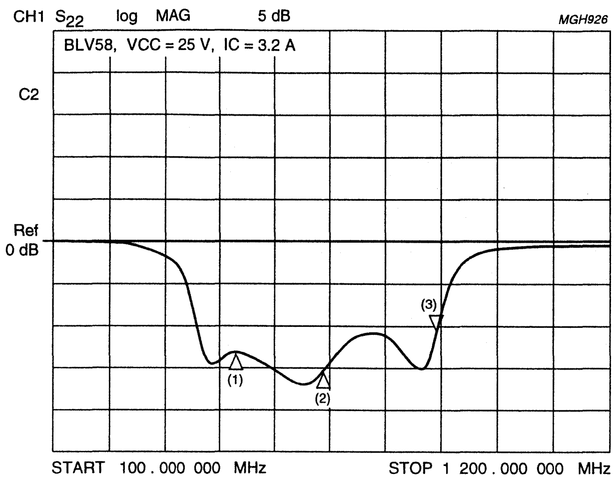


Fig.6 Class-A Bias Circuit for One Section.



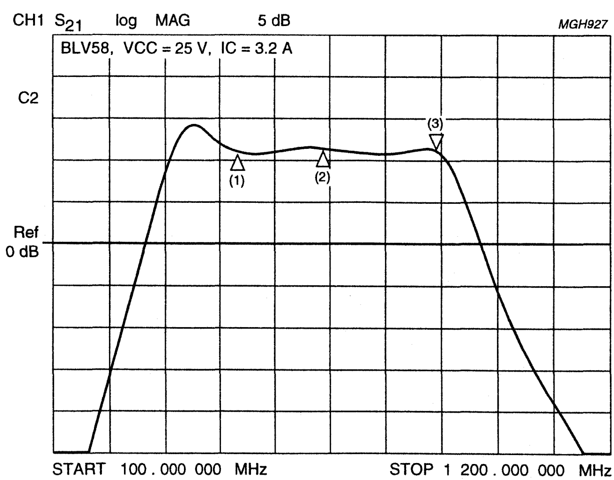
(1) −11.366 dB; 470 MHz.
(2) −13.365 dB; 636 MHz.
(3) −14.217 dB; 859 MHz.

Fig.7 Output Return Loss with Dummy Insert.



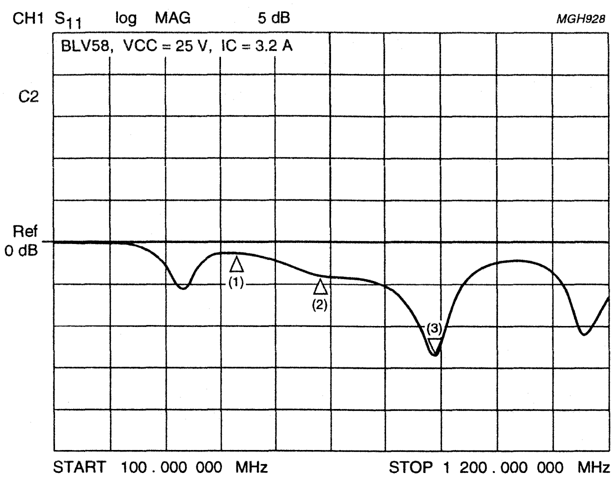
(1) −13.134 dB; 470 MHz.
(2) −15.409 dB; 636 MHz.
(3) −10.677 dB; 862 MHz.

Fig.8 Output Return Loss with BLV58.



(1) −10.959 dB; 470 MHz.
(2) −11.551 dB; 636 MHz.
(3) −10.979 dB; 862 MHz.

Fig.9 Small Signal Gain Response of Amplifier.



(1) −1.4169 dB; 470 MHz.
(2) −3.9376 dB; 636 MHz.
(3) −13.496 dB; 862 MHz.

Fig.10 Input Return Loss of Amplifier.

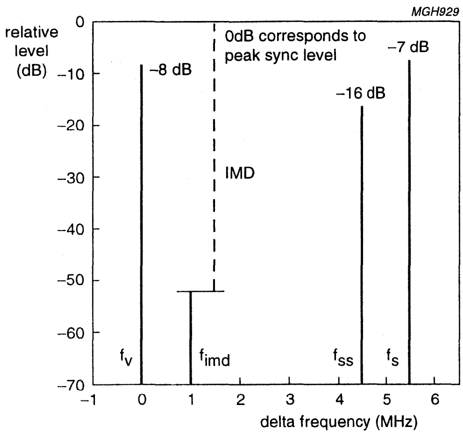


Fig.11 Three Tone Test used to Measure (IMD) According Old GPO Specification.

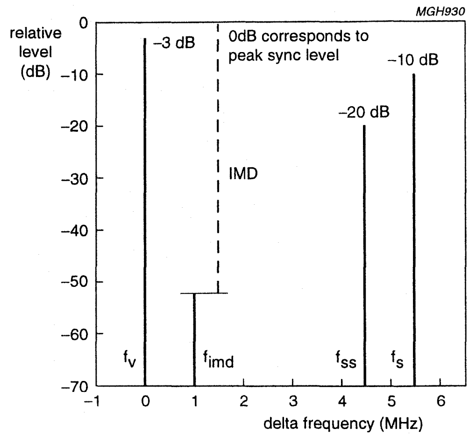


Fig.12 Three Tone Test used to Measure (IMD) According New GPO Specification.

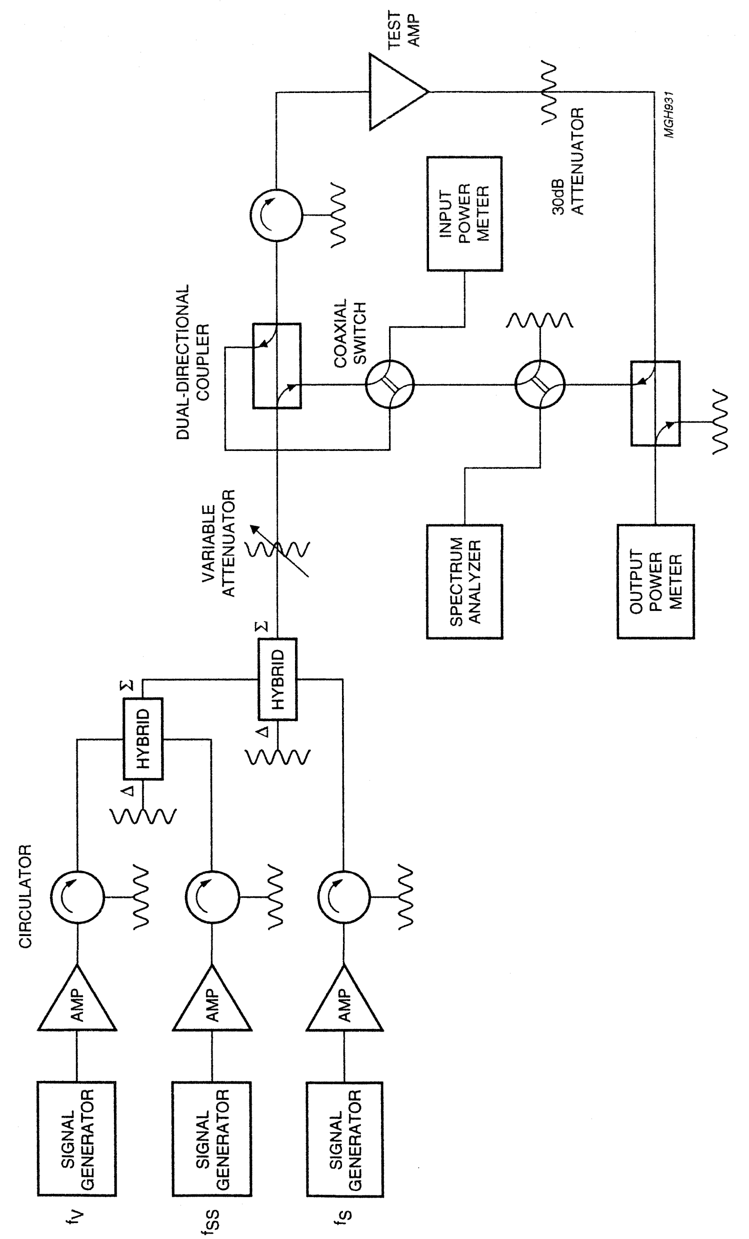
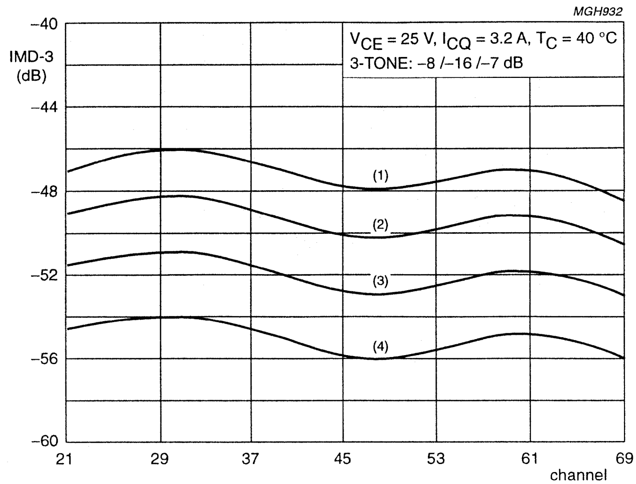
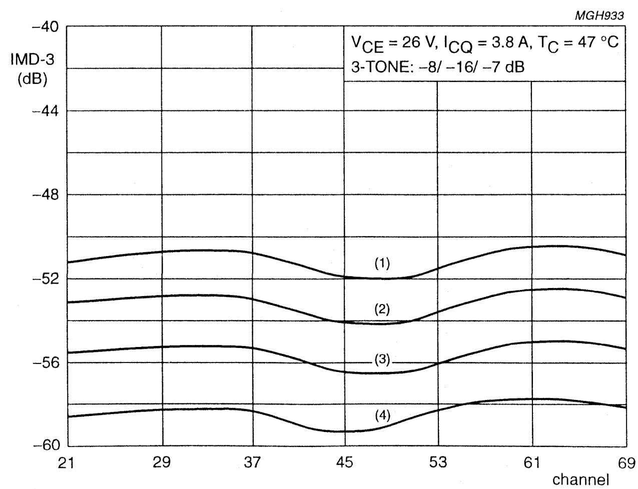


Fig.13 Three Tone Test Setup for Linearity Measurement.



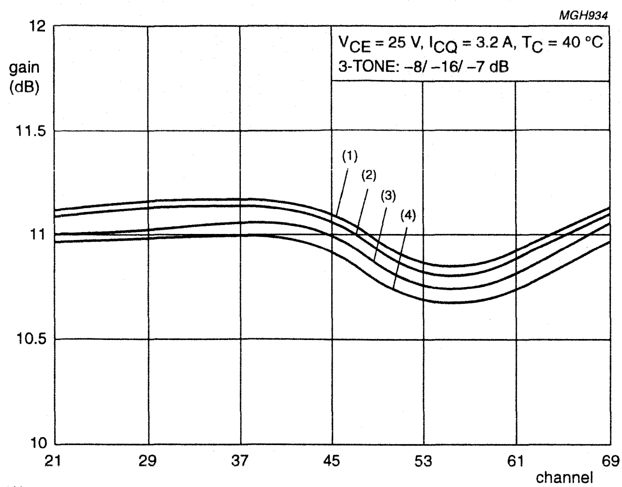
(1) Peak sync power = 18.3 W.
(2) Peak sync power = 15.7 W.
(3) Peak sync power = 13.1 W.
(4) Peak sync power = 10.4 W.

Fig.14 IMD versus Channel @ V_{CE} = 25 V and I_{CQ} = 3.2 A. According Old 3-Tone GPO Specification.



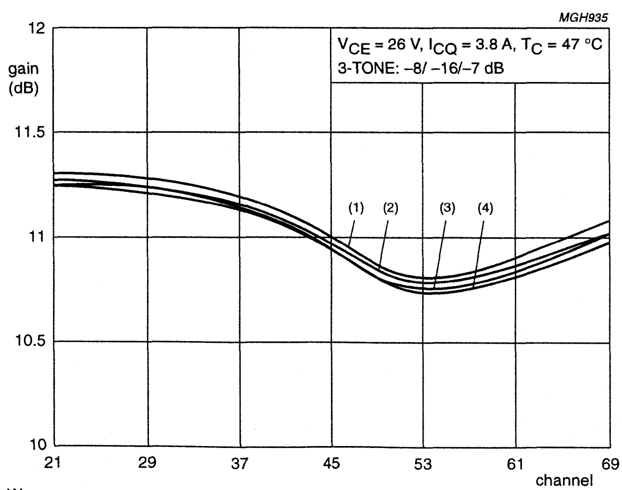
(1) Peak sync power = 18.3 W.
(2) Peak sync power = 15.7 W.
(3) Peak sync power = 13.1 W.
(4) Peak sync power = 10.4 W.

Fig.15 IMD versus Channel @ V_{CE} = 26 V and I_{CQ} = 3.8 A. According Old 3-Tone GPO Specification.



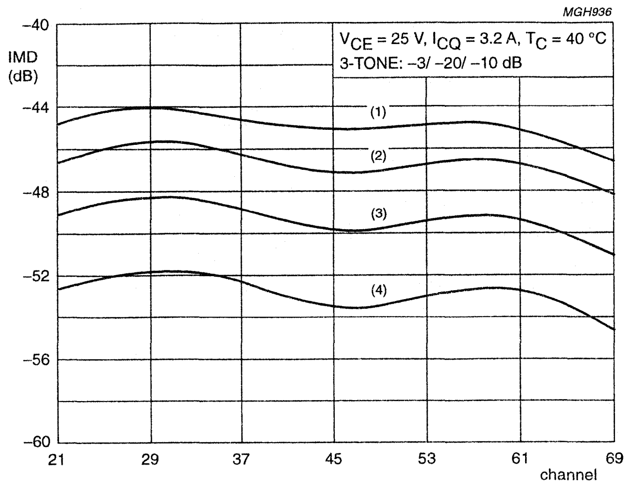
(1) Peak sync power = 10.4 W.
(2) Peak sync power = 13.1 W.
(3) Peak sync power = 15.7 W.
(4) Peak sync power = 18.3 W.

Fig.16 Gain versus Channel @ V_{CE} = 25 V and I_{CQ} = 3.2 A. According Old 3-Tone GPO Specification.



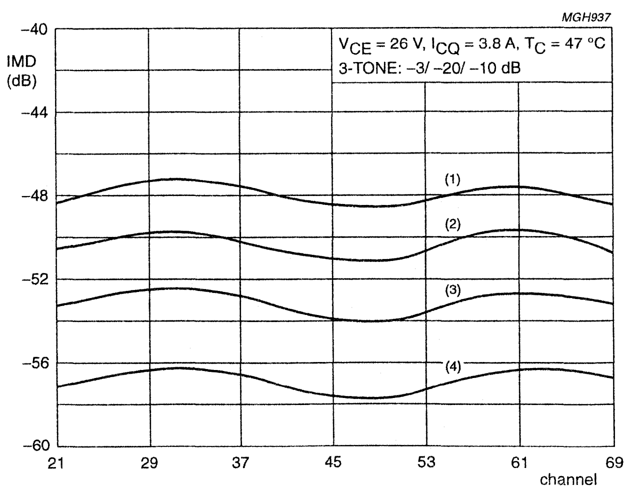
(1) Peak sync power = 10.4 W.
(2) Peak sync power = 13.1 W.
(3) Peak sync power = 15.7 W.
(4) Peak sync power = 18.3 W.

Fig.17 Gain versus Channel @ V_{CE} = 26 V and I_{CQ} = 3.8 A. According Old 3-Tone GPO Specification.



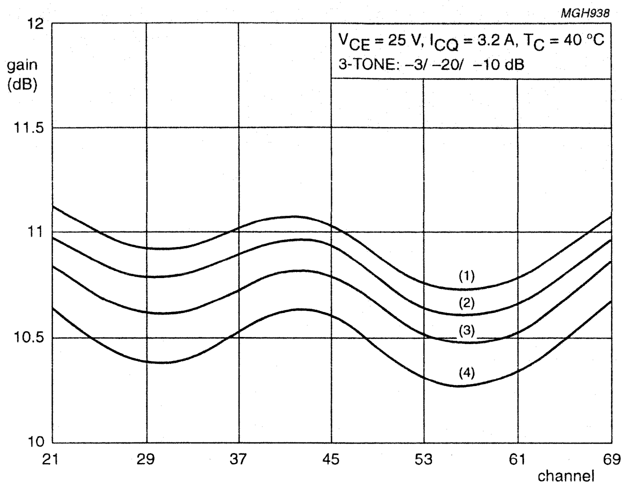
(1) Peak sync power = 21.3 W.
(2) Peak sync power = 18.0 W.
(3) Peak sync power = 14.7 W.
(4) Peak sync power = 11.5 W.

Fig.18 IMD versus Channel @ V_{CE} = 25 V and I_{CQ} = 3.2 A. According New 3-Tone GPO Specification.



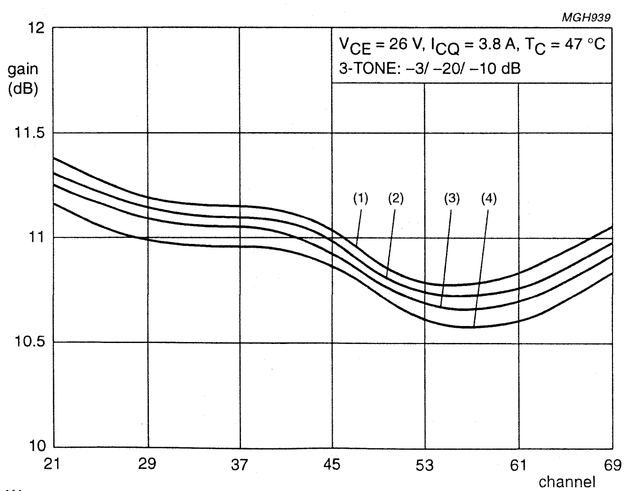
(1) Peak sync power = 21.3 W.
(2) Peak sync power = 18.0 W.
(3) Peak sync power = 14.7 W.
(4) Peak sync power = 11.5 W.

Fig.19 IMD versus Channel @ V_{CE} = 26 V and I_{CQ} = 3.8 A. According New 3-Tone GPO Specification.



(1) Peak sync power = 11.5 W.
(2) Peak sync power = 14.7 W.
(3) Peak sync power = 18.0 W.
(4) Peak sync power = 21.3 W.

Fig.20 Gain versus Channel @ V_{CE} = 25 V and I_{CQ} = 3.2 A. According New 3-Tone GPO Specification.



(1) Peak sync power = 11.5 W.
(2) Peak sync power = 14.7 W.
(3) Peak sync power = 18.0 W.
(4) Peak sync power = 21.3 W.

Fig.21 IMD versus Channel @ V_{CE} = 26 V and I_{CQ} = 3.8 A. According New 3-Tone GPO Specification.

A Broadband 100 W Push Pull Amplifier for Band IV & V TV Transmitters based on the BLV861

Application Note
AN98033

1 INTRODUCTION

Intended for applications in TV transmitter output stages a broadband high power amplifier has been described with a single BLV861 transistor. The design objectives are given in Table 1. In the following sections a background information of the BLV861 will be given, followed by a description and tuning of the application circuit. A broadband small signal and large signal performance of the BLV861 will be described. Finally several tests results will be shown measured in channel 69 (855/860 MHz). Additional AM-AM and AM-PM (ICPM) characteristics are presented which is a commonly measured parameter in analog vs. digital television transmitters. Because of the increasing interest for combined amplification of sound and vision also two and three-tone performance has been presented.

Table 1 Design objectives of the BLV861 amplifier

	SYMBOL	VALUE	UNIT
Frequency band	BW	470 to 860	MHz
Output power @ 1 –dB compression *	P_{out}	>100	W
Power gain	G_P	>8.5	dB
Gain ripple	$G_{P\text{-ripple}}$	±0.5	dB
Efficiency	η	>55	%
Input Return loss	IRL	–3 to –8	dB
Conditions: V_{ce} = 28 V; P_{LOAD} = 100 W; I_{CQ} = 100 mA; T_{HS} = 25 °C			

2 TRANSISTOR DESCRIPTION

2.1 BLV861 Internal Configuration

The BLV861 is a 100 W transistor encapsulated in a SOT289 package. A simplified outline of this package is shown in Fig.1. The emitter is connected to the flange and the collector leads are internally shorted for DC because of the applied postmatching. Due to this configuration its not possible to measure both collector currents separately.

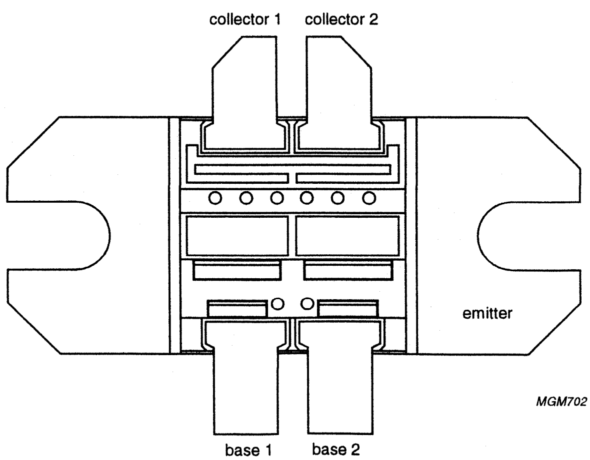


Fig.1 SOT289 package outline of the BLV861.

The active part of the BLV861 consists of two dies with a 6 μm emitter-pitch technology. It incorporates high value polysilicon emitter ballasting resistors for an optimum temperature profile in class-AB as well as in class-A operation (note 1). Combined with gold metallization it offers a high degree of reliability and ruggedness. The main transistor data is summarised in Table 2.

Table 2 Summary of main transistor data; note 1

MODE OF OPERATION	f [MHz]	V_{CE} [V]	P_L [W]	G_P [dB]	EFF. [%]	$G_{P\text{-}COMP.}$ [dB]	$R_{thj\text{-}hs}$ [K/W]
Class-AB	860	28	100	>8.5 dB	>55 %	<1dB	<1.0

Note

1. $P_{DISSIPATION} \leq 140$ W (DC) and $T_{junction,max} < 200$ °C.

2.2 BLV861 Internal Matching

The BLV861 is internally matched to increase the useable bandwidth and to elevate the device terminal impedance. Figure 2 shows the equivalent circuit of one section BLV861, with its matching circuitry. The input is pre-matched with two lowpass LC-sections to get low-Q transformation steps and high intermediate impedance level at the base terminals. The output is post-matched with a collector-to-collector shunt inductor which is designed to resonate with the transistor output capacitance at the low end of the band. This results in an increased broadband capability and increased impedance level at the transistor output.

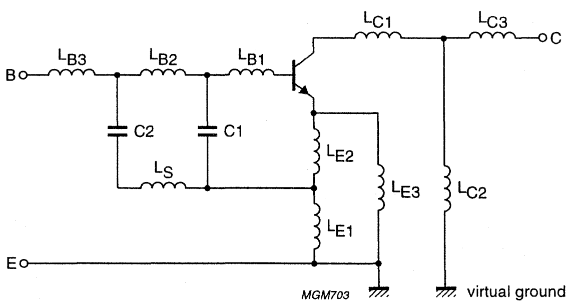


Fig.2 Internal circuit topology of one section BLV861.

2.3 Gain and Impedance Data

The gain and impedance data are listed in the Table 3 and curves are given in Figs 8 to 10. These data have been measured in a fixture tuned for maximum gain at rated output power for each frequency. The impedance data which is given has been measured from base-to-base and collector-to-collector terminals.

Table 3 Gain and impedance data (total device)

f MHz	G_P dB	η %	Z_{IN} (Ω)		Z_{LOAD} (Ω)	
			REAL{Z_{IN}}	IMAG{Z_{IN}}	REAL{Z_{LOAD}}	IMAG{Z_{LOAD}}
471	11.34	52.29	0.55	4.74	13.91	−10.13
519	10.97	52.99	1.23	5.17	13.40	−5.12
567	10.46	52.91	2.24	6.12	12.18	−3.71
615	10.12	53.54	3.26	6.82	10.10	−3.32
663	9.76	53.38	4.39	7.90	8.82	−3.65
711	9.99	54.28	5.44	8.42	6.94	−4.13
759	10.12	53.71	7.16	7.13	5.85	−4.45
807	9.96	54.03	8.04	4.14	5.28	−4.80
855	8.72	53.71	5.96	0.91	5.02	−5.81
Conditions: V_{CE} = 28 V; P_{LOAD} = 100 W; I_{CQ} = 100 mA; T_{HS} = 25 °C						

3 AMPLIFIER DESIGN

The total description of the amplifier is given in Figs 6 and 7 and Table 8. The amplifiers input and output matching networks contain mixed microstrip-lumped elements networks to transform the terminal impedance levels to approx. 25 Ω balanced. The remaining transformation to 50 Ω unbalanced is obtained by 1 : 2 balun transformers. The baluns B_1 and B_2 are 25 Ω semi-rigid coax cables with an electrical length of 45° at midband and a diameter of 1.8 mm, soldered over the whole length on top of microstrip lines. To keep the circuit in balance two stubs L_1 and L_8 with the same length have been added. For low frequency stability enhancement the input balun stubs are connected to the bias point by means of 1 Ω series resistors. Large capacitors (C_4 and C_{11}) are added at the biasing points to improve the amplifiers video response. The printed-circuit board laminate utilised is PTFE-glass with an ε_r = 2.55 and a thickness of 0.51 mm (20 mills). Specification of all components are given in Table 8.

3.1 Input Network

The input network is designed for high gain match and flat overall gain versus frequency. This is achieved by a three section lowpass filter with a series capacitor at 50 Ω input impedance level. Three variable capacitors are included for fine tuning of the gain. C_5 with an additional trimmer is utilised to tune the gain slope at low end of the frequency while C_7 is intended to tune the gain slope at 860 MHz. C_6 on the other hand is used to tune the gain ripple. See circuit diagram in Figs 6 and 7. The capacitor C_7 is placed close to the base of the BLV861 to maintain low Q transformation.

3.2 Output Network

The output network is designed for high output power and efficiency in full bandwidth. First two capacitors (C8 and C9) are placed close to each other. The physical distance between the capacitors is shown in Fig.7. RF dissipation in shunt capacitors, due to circulating currents, is a critical factor in the design of the output networks. The most critical component is the first shunt capacitor at the collector terminals. The current in this capacitor is at maximum level when operated at the upper end of the frequency band at max. power level. In practice this usually results in melting of the solder which on its turn degrades the power capability as experienced with ATC100B low Q capacitors. On the next page a comparison of ATC100B and ATC180R capacitors has been given. Calculations has been carried out in order to determine the heat development in this capacitors. The power transfer efficiency is given by:

$$\eta_{power\ transfer} = \left(1 - \frac{Q_L}{Q_U}\right)^2 \qquad (1)$$

Expressed in power losses we have:

$$P_{LOSS} = 10 \cdot \log\left(\frac{1}{\eta}\right)^2 \tag{2}$$

To get an impression of the body temperature of a capacitor, which can be strongly influenced by its own unloaded Q, we first have to define heat intensity of a body. The temperature of this body is proportional to the heat intensity. Generally the heat intensity of a body is defined as Joule per unit volume per second:

$$\text{Heat\_intensity} = \frac{\text{Absorbed power}}{\text{Volume}} = \frac{\text{Joule}}{m^3} \cdot \frac{1}{s}\left[\frac{W}{m^3}\right] \tag{3}$$

An example has been given in order to confirm the power capability of the ATC180R capacitors which has been used in BLV861 application circuit.

Table 4 Comparison of the electrical parameters of the ATC100B and ATC180R

TYPE OF CAPACITOR	ATC100B	ATC180R-1	ATC180R-2	UNIT
Value	13	10	2.7	pF
ESR	0.097	0.068	0.123	Ω
Unloaded Q (Q_U)	147	271	559	
Resonance frequency	1.79	3.33	5.73	GHz
Current	5.56	7.66	5.16	A
Dimensions	2.794 × 2.794 × 2.591	2.67 × 1.78 × 2.29	2.67 × 1.78 × 2.29	mm^3
Frequency of operation	860	860	860	MHz
Power to be transferred	100	100	100	W
Loaded Q (Q_L); note 1	3	3	3	

Note

1. Assumed high loaded Q is present at the upper end of the frequency (worst case).

Consider a single 13 pF ATC100B capacitor, see Table 4, then we get from [2]:

$$P_{LOSS} = 10 \cdot \log\left(\frac{1}{1-\frac{2}{147}}\right)^2 = 0.0595\ \text{dB}\ , \tag{4}$$

which means that 2.70% (2.7 W) of the through-put power is converted into heat.
The total heat intensity becomes:

$$\text{Heat\_intensity} = \frac{100\ [W] \cdot 0.027}{2.794\ [mm] \cdot 2.794\ [mm] \cdot 2.591\ [mm]} = 0.134 \frac{W}{mm^3} \tag{5}$$

In the same manner we can calculate the losses for the two paralleled ATC180R capacitors (10 pF//2.7 pF) which are used in the BLV861 output circuit. First we have to calculate the overall Q_U from the single component data as listed in table 4.

$$ESR_{TOT} = \frac{ESR_1 \cdot ESR_2}{ESR_1 + ESR_2} = 0.044\ \Omega \tag{6}$$

$$C_{TOT} = C_1 + C_2 = 12.7\ \text{pF} \tag{7}$$

$$Q_U = \frac{1}{2 \cdot \pi \cdot f \cdot ESR_{TOT} \cdot C_{TOT}} = 331 \tag{8}$$

$$P_{LOSS} = 10 \cdot \log\left(\frac{1}{1-\frac{2}{331}}\right)^2 = 0.0263\ \text{dB}\,, \tag{9}$$

which means that only 1.2% (1.2 W) of the through-put power is converted into heat.

The heat intensity is:

$$\text{Heat\_intensity} = \frac{100\,[\text{w}] \cdot 0.012}{2 \cdot 2.67\,[\text{mm}] \cdot 1.78\,[\text{mm}] \cdot 2.29\,[\text{mm}]} = 0.0554\frac{\text{W}}{\text{mm}^3} \tag{10}$$

As can be noticed, in case of two ATC180R capacitors the body temperature is more than factor 2 lower compared to an ATC100B capacitor. Taking into account the main parameters and power handling capability, it has been decided to utilise ATC180R as the first output matching capacitor. The capacitors need to be placed in full contact with the printed-circuit board in order to maintain better thermal resistance.

3.3 Bias Circuit

The class-AB bias circuit used is shown in Fig.3. This circuit has a very low power consumption allowing the use of low power SMD chip resistors. Two NPN transistors BD139 are used. T2 is chosen to operate in the reverse mode in order to have its lower collector to base diode voltage to track the base-emitter voltage of the BLV861. R3 mainly compensates for the difference between these two values. T2, T3 and BLV861 have been mounted on the same heatsink to have good temperature compensation. R4 is incorporated to improve video response and to protect T3 in case of short circuit in the BLV861 amplifier. Capacitor C15 bypass any RF leakage to T2. The bias circuit is fully integrated on the amplifier board, see Fig.7.

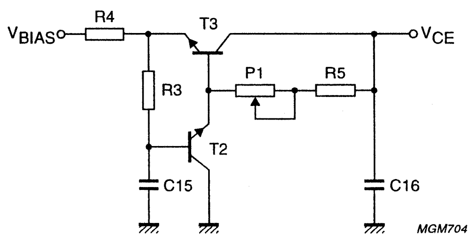


Fig.3 Class-AB bias circuit.

4 BROADBAND RF PERFORMANCE OF THE BLV861 AMPLIFIER

The amplifier has been tuned under class-A small-signal conditions and characterised under large signal class-AB conditions from 470 – 860 MHz. The conditions used shown in Table 5

Table 5 Conditions for class A and AB characterisation

	SMALL SIGNAL	LARGE SIGNAL
Class of operation	A	AB
Collector-emitter voltage	28 V	28 V
Quiescent current (I_{CQ})	1.0 A	0.1 A
Source/Load impedance	50 Ω	50 Ω
Heatsink temperature	25 °C	25 °C

4.1 Small Signal Response

Tuning high power amplifiers under small-signal class-A conditions to obtain optimum large signal performance was found to be a very suitable and save technique. The best small-signal response was determined experimentally.
The S_{11}, S_{22} and S_{21} response resulting in optimum large signal performance is given in Figs 11 to 14. The input is tuned for maximum gain and a flat response over the whole frequency band (470 – 860MHz). The output is tuned under both small signal and large signal to get an optimum power performance.

4.2 Large Signal Response

After the small-signal class-A tuning the amplifier was biased into class-AB operation. Gain, collector efficiency, input return loss and compression was determined versus frequency at a power level of 100 W (CW). The data are summarised in Figs 15 and 16 and Table 9. The power gain compression and collector efficiency are strongly sensitive to the location of capacitors C_8 and C_9, which have to be optimized experimentally. Shifting this capacitors from their initial location to the left will result in an improved power gain compression and a poor efficiency, while shifting to right will improve the efficiency. The average gain power level is about 9.0 dB with a ripple of less than ± 0.3 dB. Broadband collector efficiency is fluctuating around 56% and shows a dip at midband (663 MHz, i.e. channel 45). Power gain compression in the band of interest is below 0.8 dB. Highest compression of 0.79 dB occurs at 860 MHz which is referenced to 40 W output power level (CW). The broadband input return loss varies from –3.5 dB at the lower end to less than –10 dB at the upper end of the frequency range.

4.3 Amplifier Overdrive Capability Test

An 3 dB input overdrive test has been performed in order to force the amplifier beyond its saturation power and to check its overdrive capability. P_{OUT} vs. P_{IN} measurements have been done from zero to >3 dB above its nominal drive level at 860 MHz. The amplifier has proven to withstand a drive level of above 25 W many time for several minutes without degradation of the device. The power level associated with this level was 135 W (CW). Figs 17 and 18 presents the recorded data.

5 NON-LINEAR DISTORTIONS

Amplitude dependent waveform distortions are often referred to as non-linear distortions. This classification includes distortions which are dependent on average picture level (APL) changes and/or instantaneous signal level changes. Generally, amplifiers are linear over only a limited range, they may tend to compress or clip large signals. Non-linear distortions may also manifest themselves as crosstalk and intermodulation effects. The first three distortions measured and discussed in this section are:

- Intermodulation:
  - Two tone intermodulation, if sound and vision are amplified separately
  - Three tone intermodulation, in case of combined amplification.
- Incidental carrier phase modulation.

5.1 Intermodulation

Because of the increasing interest for combined carrier operation, the linear performance of the amplifier for two-tone and three-tone operation have been determined. Two tone and three tone IMD-measurement have been performed as defined in Fig.4. For two tone performance two carriers have been chosen which represents the vision and sideband carrier. Three tone measurement is done with an additional carrier which represents the sound carrier. The different tone systems used are listed in Table 6.

Table 6 Survey of used tone system for intermodulation measurements

CHANNEL 69	SYSTEM A	SYSTEM B	SYSTEM C
f_{visin} = 855.25 MHz **$f_{sideband}$ = 859.68 MHz** **f_{sound} = 860.75 MHz**		**dB**	
Vision amplitude	−8	−5	−3
Sideband amplitude	−16	−17	−20
Sound amplitude	−10	−10	−10

Two tone IMD-performance is depicted as a function of the output peak-sync power ($P_{O,SYNC}$) in Figs 19 to 21. Figure 22 shows three tone IMD performance of all three systems, shown in Table 6, measured in channel 69. As can be noticed $P_{O,SYNC}$ of each system is different. System A has a much higher output sync power related to system B and C, at the same average output power level. In all cases $P_{O,SYNC}$, is assumed to be at a certain reference level which is 0 dB. Based on this assumption conversion formulas are given to calculate different power levels regarding all systems, see "Appendix A".

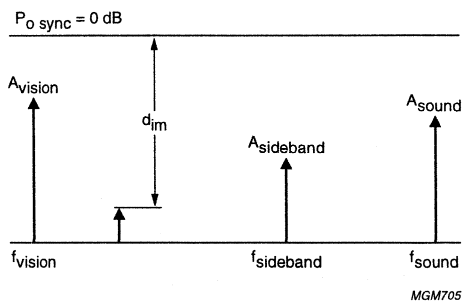


Fig.4 Definition of IMD measurement.

Finally a full band intermodulation performance has been given which is measured according to system A. As can be noticed a better linearity can be obtained around channel 45, see Table 7. A 3D graph which represents IMD = ($P_{O,SYNC}$, frequency channel) is given in Fig.23.

Table 7 Intermodulation vs. output power for 9 TV channels in Band IV and V (referred to $P_{O,SYNC}$ level)

SYSTEM A (–8/ –16/ –10)		TV CHANNELS								
$P_{O,AVG}$	$P_{O,SYNC}$	21	27	33	39	45	51	57	63	69
W		dB								
0.1	0.35	–42.3	–39.5	–38.6	–39.7	–41.4	–39.2	–37.8	–38.2	–37.8
1	3.53	–41.9	–39.8	–39.3	–39.5	–40.2	–38.9	–36.8	–37.8	–36.8
10	35.26	–49.0	–48.2	–47.9	–47.4	–46.5	–45.6	–41.5	–44.2	–41.5
20	70.52	–48.0	–50.6	–51.3	–49.6	–50.1	–51.0	–46.4	–50.5	–46.4
30	105.78	–44.6	–47.7	–48.7	–46.6	–55.8	–52.2	–50.6	–56.3	–50.6
40	141.04	–39.7	–43.3	–43.7	–42.1	–55.3	–45.9	–43.3	–45.3	–43.3
50	176.30	–35.4	–39.0	–39.2	–37.6	–45.0	–39.5	–37.6	–38.9	–37.6
60	211.56	–32.5	–35.3	–35.4	–34.0	–39.5	–35.3	–33.6	–34.4	–33.6

5.2 Incidental Carrier Phase Modulation

Incidental carrier phase modulation (ICPM) is a commonly measured parameter in analog television transmitters. This type of distortion is also commonly referred to as AM to PM distortion. The phase shift through an amplifier has the tendency to vary with output power. The capacitance of a reversed biased diode then varies with bias voltage. In an amplifier the trick is to avoid phase shift variations with output power level. Measurements have been carried out in order to determine the phase distortion of the amplifier using a network analyser. ICPM and also AM to AM distortion vs. input drive power is plotted in Figs 25 and 26 under several bias conditions.

The total setup for power sweep is reflected on Fig.24. The sweep range of the network analyser was set from –5 to +20 dBm corresponding with 0.05 to 15.6 W input drive power. Slight gain expansion at low output powers is obvious due to turn-on effects.

The phase is very linear up until the point where compression emerges. Important points for observation are the compression and phase deviation at 12.25 W drive power shown by marker 3 (valid for I_{CQ} = 100 mA). The phase shift is about ≈6.2° at 12.25 W input drive power (which corresponds to 100 W output load power) and the gain compression is around 1 dB referred to marker 2 (Figs 25 and 26).

6 TV CHARACTERISATION

Finally the amplifier is characterised with a PAL Composite Video Signal (CVS) (without soundcarrier) according CCIR standard G. The TV test setup used, is depicted in Fig.27. The following measurements have been performed under TV conditions:

- Differential gain
- Differential phase
- Transient sync compression vs. output peak sync power level
- Peak output power @ 1 dB compression.

TV measurements including differential gain and differential phase have been also characterised at V_{CE} = 32 V and I_{CQ} = 100 mA in order to attain higher output peak sync power.

6.1 Differential Gain

Differential gain is present if chrominance gain is dependent on luminance level. These amplitude errors are a result of the systems inability to uniformly process the high-frequency chrominance signal at all luminance levels. Differential gain is expressed in percentage of the chrominance gain at blanking level. The input video waveform used for differential gain evaluation is a modulated staircase with 10% rest carrier as given in Figs 28 and 29. Figures 33 to 40 reflects differential gain and differential phase in channel 69.

6.2 Differential Phase

Differential phase is present if a signals chrominance phase is affected by luminance level. This phase distortion is a result of a systems inability to uniformly process the high-frequency chrominance information at all luminance levels. The amount of differential phase distortion is expressed in degrees. See Figs 33 to 40.

6.3 Sync Compression vs. Peak-Sync Power

One effect produced by non-linearity above the blanking level is compression of the sync pulse. This effect is compensated in transmitters by making the sync pulses correspondingly greater before amplification. The degree of this so called sync-stretching required, depends on the sync compression due to the non-linearity in the amplifier. Evaluation of the sync compression is done using a input video waveform at black level, see Figs 28 and 5. The sync power is calculated by from the measured average output power and the sync-to-bar ratio after demodulation.
The sync-to-bar ratio is measured with the video waveform on line 18 containing a 100% white-bar. With this available ratio the sync amplitude can be calculated referenced to a 1 V sync-to-bar top level. The sync content is then normalised to a 1.11 V RF amplitude. An undistorted signal corresponds to 27% sync content. The sync power can then also be determined from the obtained sync level. The formula and definitions used for this calculation are given in formula 11 to 13 and in Fig.5. The output sync pulse content versus $P_{O,SYNC}$ power is presented in Fig.30.

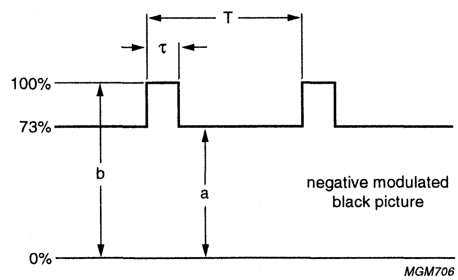


Fig.5 Composite video signal with black level for determining peak-sync power.

$$P_{RMS} = \frac{U_{RMS}^2}{R} = \frac{\left(\sqrt{\frac{1}{T}\int_o^\tau b^2 \cdot dt + \frac{1}{T}\int_\tau^T a^2 \cdot dt}\right)^2}{R} = \frac{\frac{\tau}{T} \cdot b^2 + \left(1 - \frac{\tau}{T}\right) \cdot a^2}{R} \tag{11}$$

$$P_{SYNC} = \frac{b^2}{R} \tag{12}$$

From [11] and [12] we have:

$$k = \frac{P_{SYNC}}{P_{RMS}} = \frac{1}{\frac{\tau}{T} + \left(1 - \frac{\tau}{T}\right) \cdot \left(\frac{a}{b}\right)^2} \text{(black picture)} \tag{13}$$

In case of no sync compression or expansion (a = 73% and b = 100%), then k = 0.567. In Fig.31 $P_{O,SYNC}$ versus $P_{IN,SYNC} = P_{IN,RMS}/k$ is depicted. In practice the allowable sync compression is bound to a maximum since sync-stretching is limited.

6.4 Output Sync Power Capability

Figure 32 shows gain versus $P_{O,SYNC}$ power for channel 69. The input video signal is at black level. The 1 dB compression point at I_{CQ} = 100 mA is above 120 W $P_{O,SYNC}$. At V_{CE} = 32 V on the other hand, 1 dB compression is above 150 W peak sync power.

7 CONCLUSIONS

A complete TV transmitter amplifier has been designed and characterised based on the BLV861, capable of operating in full band IV and V with flat gain and high output power in class-AB. BLV861 is able to generate 100 W CW power and a power gain compression below 1 dB in band IV and V. Overall gain of the amplifier is >8.5 dB and an efficiency of ± 55%. TV-measurements have been carried out showing a 1 dB compression point above 120 W $P_{O,SYNC}$ at V_{CE} = 28 V and 150 W at V_{CE} = 32 V.

- Amplifier shows an agreed linearity performance in class AB operation both under two tone and three tone conditions
- Biasing the amplifier at a V_{CE} = 32 V results in a higher output peak sync power and a better linearity response.

8 REFERENCES

Ref.1: Rohde & Schwarz Sound and Broadcasting:
"Rigs and Recipes how to measure and monitor...".

Ref.2: Philips Semiconductors Nijmegen, Prod. group Transistors and Diodes
BLV862 Application note: AN98014.

Ref.3: American Technical Ceramics:
The RF capacitor handbook, June 1970 / first edition.

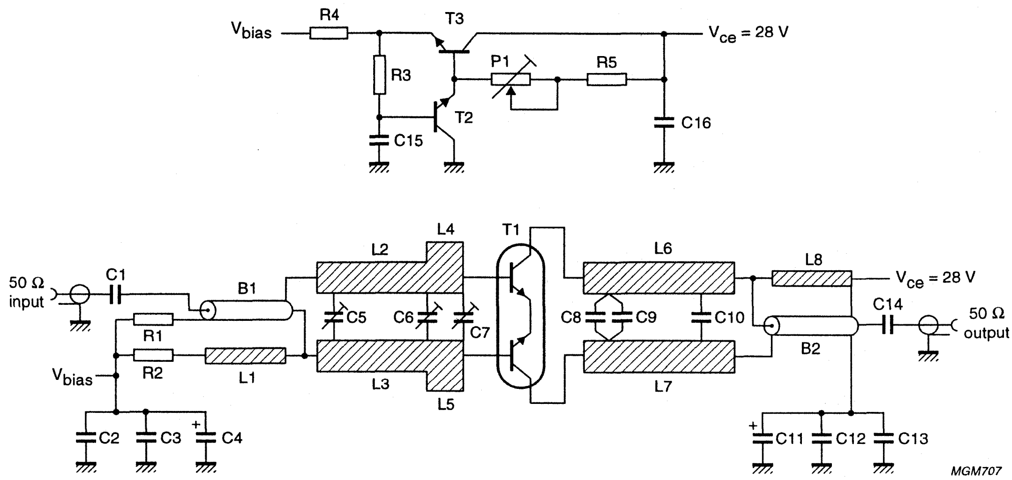
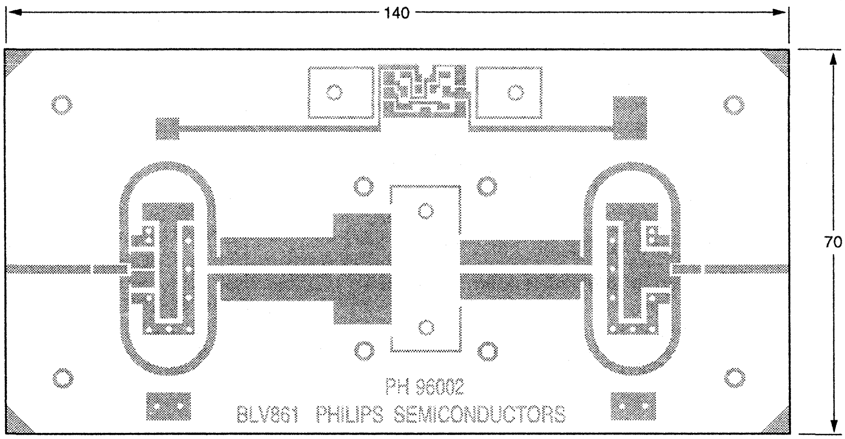


Fig.6 BLV861 amplifier circuit.



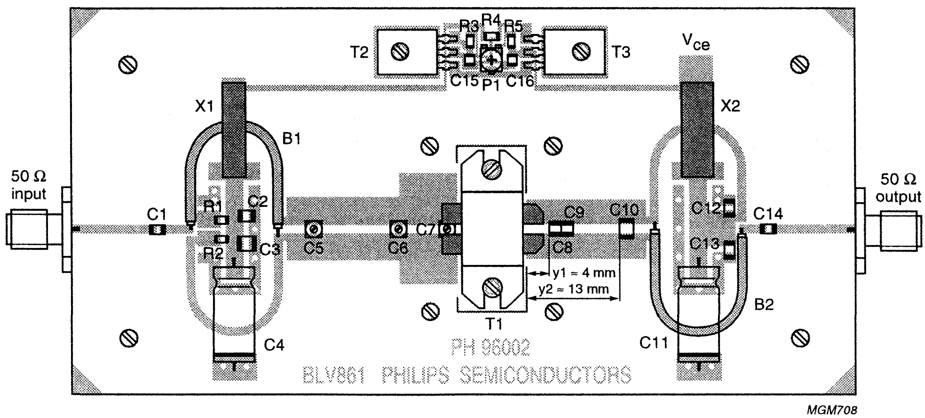


Fig.7 BLV861 Amplifier Circuit Board and layout.

Table 8 List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
C1	multilayer ceramic chip capacitor; note 1	15 pF	
C2 and C12	multilayer ceramic chip capacitor	15 nF	2222 590 16629
C3 and C13		100 nF	2222 581 16641
C4 and C11	solid aluminium capacitor	100 μF/40 V	2222 031 37101
C5	multilayer ceramic chip capacitor; note 2 + Tekelec trimmer	2.2 pF	
C6		10 pF	
C7		15 pF	
C8	multilayer ceramic chip capacitor; note 3	2.7 pF	
C9		10 pF	
C10	multilayer ceramic chip capacitor; note 2	3 pF	
C14	multilayer ceramic chip capacitor; note 1	30 pF	
C15		100 pF	
C16	multilayer ceramic chip capacitor	15 nF	
R1 and R2	SMD resistor	1 Ω	805
R3		47 Ω	
R4		1 Ω	
R5		1 k2 Ω	
P1	potentiometer	5 kΩ	
T1	NPN push-pull RF-transistor	BLV861	9340 542 40112
T2 and T3	NPN transistor	BD139	9330 912 20112
B1	semi rigid coax balun UT70-25	Z = 25 ±1.5 Ω	47.0 mm
B2			

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. American Technical Ceramics type 180R or capacitor of same quality.
4. The striplines are on a double copper-clad printed-circuit board: PTFE-glass material (TLX8) from Taconic (epsilon of 2.55).

Narrowband Gain and Impedance Data.

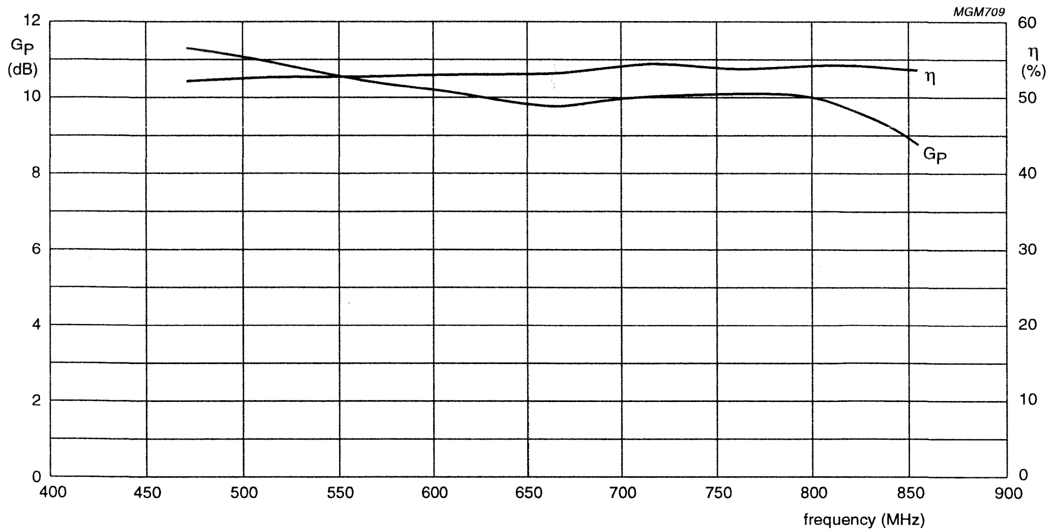


Fig.8 Maximum power gain and Collector efficiency.

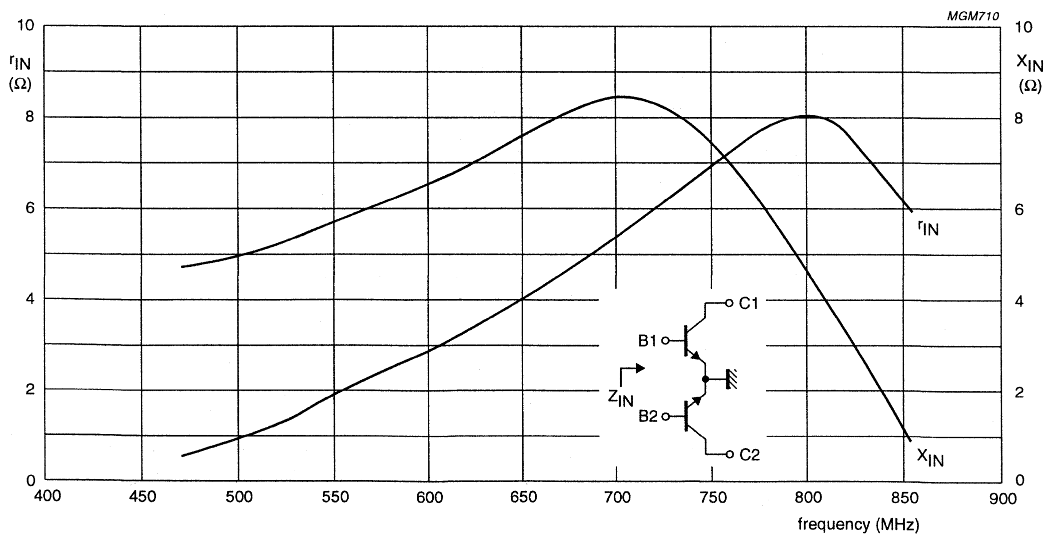


Fig.9 Input Impedance.

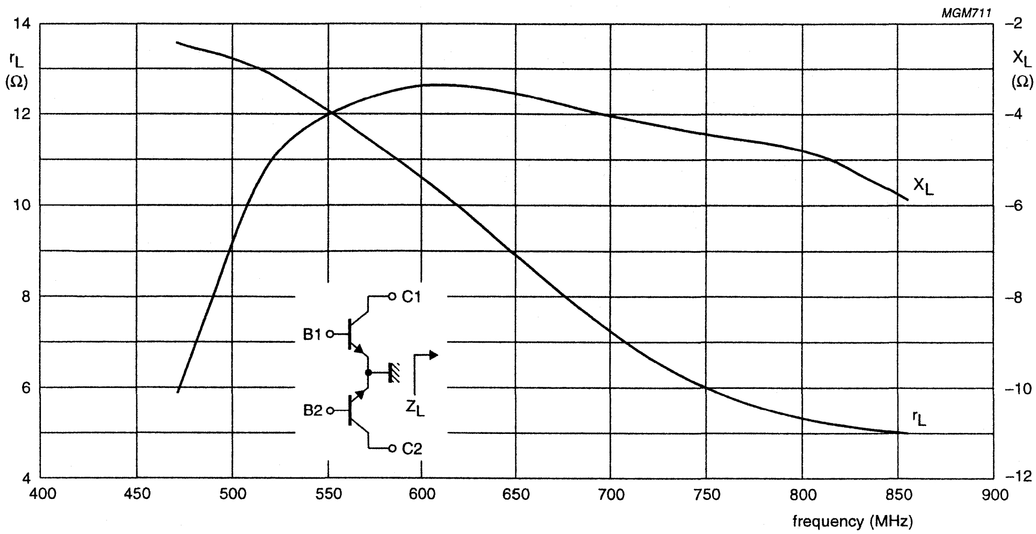
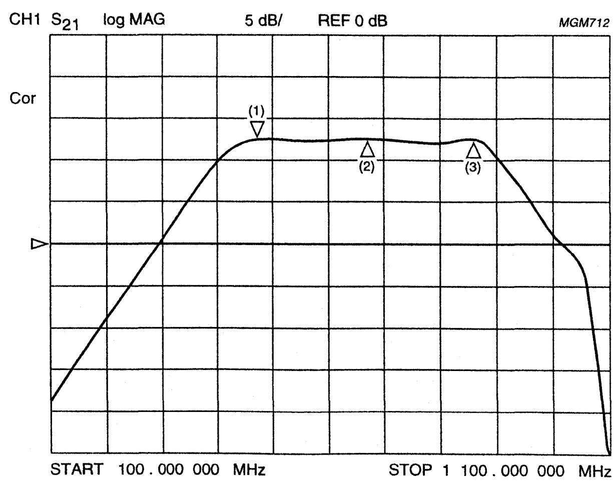
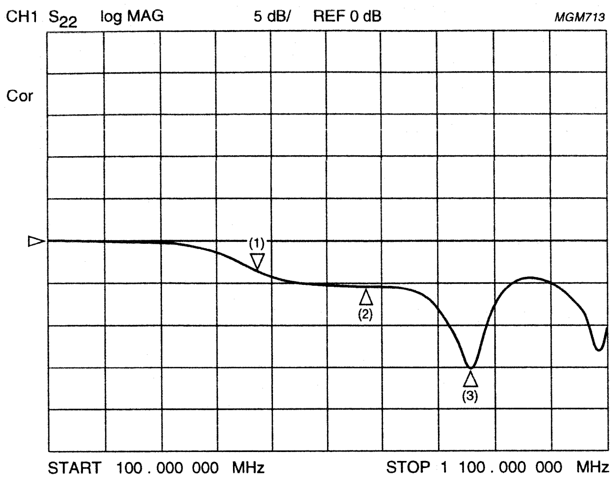


Fig.10 Output Impedance.



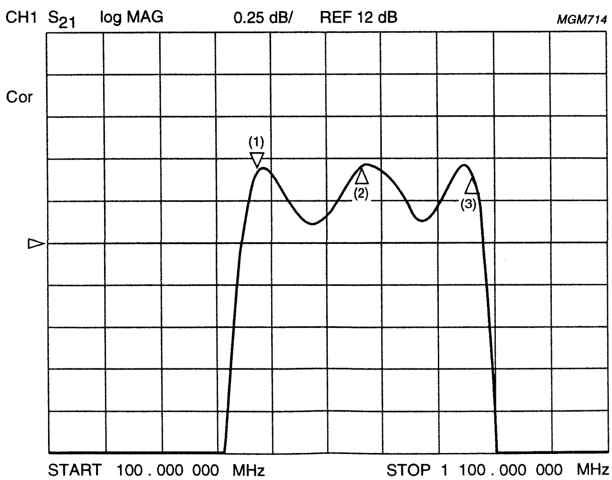
(1) 470 MHz: 12.38 dB.
(2) 665 MHz: 12.45 dB.
(3) 860 MHz: 12.38 dB.

Fig.11 Broadband Small Signal Respons S_{21}.



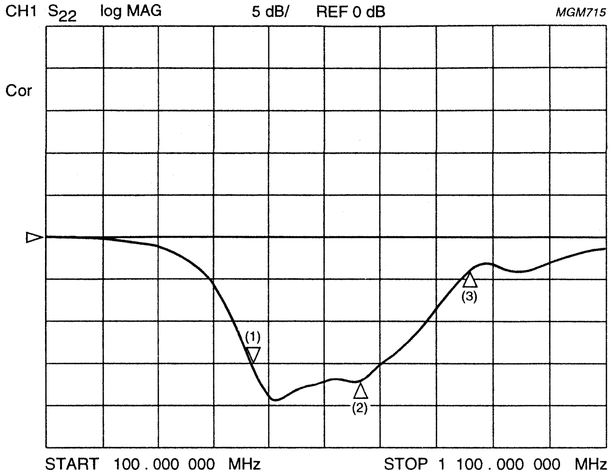
(1) 470 MHz: −3.50 dB.
(2) 665 MHz: −5.56 dB.
(3) 860 MHz: −15.09 dB.

Fig.12 Broadband Small Signal Respons S_{11}.



(1) 470 MHz: 12.38 dB.
(2) 665 MHz: 12.45 dB.
(3) 860 MHz: 12.38 dB.

Fig.13 Broadband Small Signal Respons S_{21}-ripple.



(1) 470 MHz: −15.34 dB.
(2) 665 MHz: −16.96 dB.
(3) 860 MHz: −4.14 dB.

Fig.14 Broadband Small Signal Respons S_{22}.

Table 9 Broadband Large Signal Performance

FREQUENCY MHz	**Gp dB**	**ΔGp dB**	**IRL dB**	η_c **%**
471	9.27	−0.67	−3.49	57.70
519	9.37	−0.47	−4.25	54.11
567	9.33	−0.46	−5.08	56.24
615	8.98	−0.74	−5.64	57.51
663	8.86	−0.67	−5.81	50.02
711	9.22	−0.55	−5.52	57.60
759	8.94	−0.59	−5.60	58.55
807	8.76	−0.69	−7.14	57.05
855	9.10	−0.79	−10.12	56.42

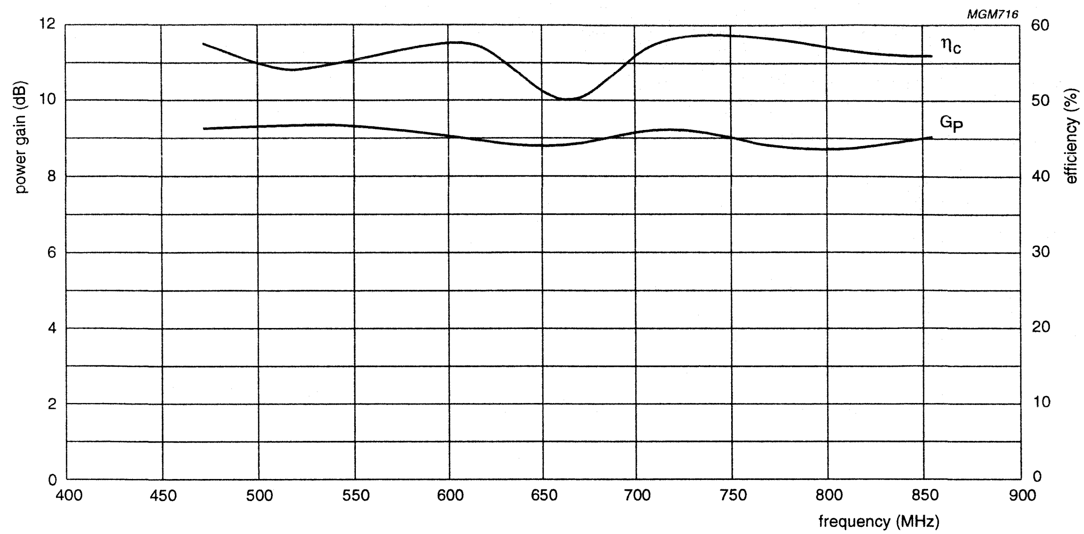


Fig.15 Broadband power gain and collector efficiency.

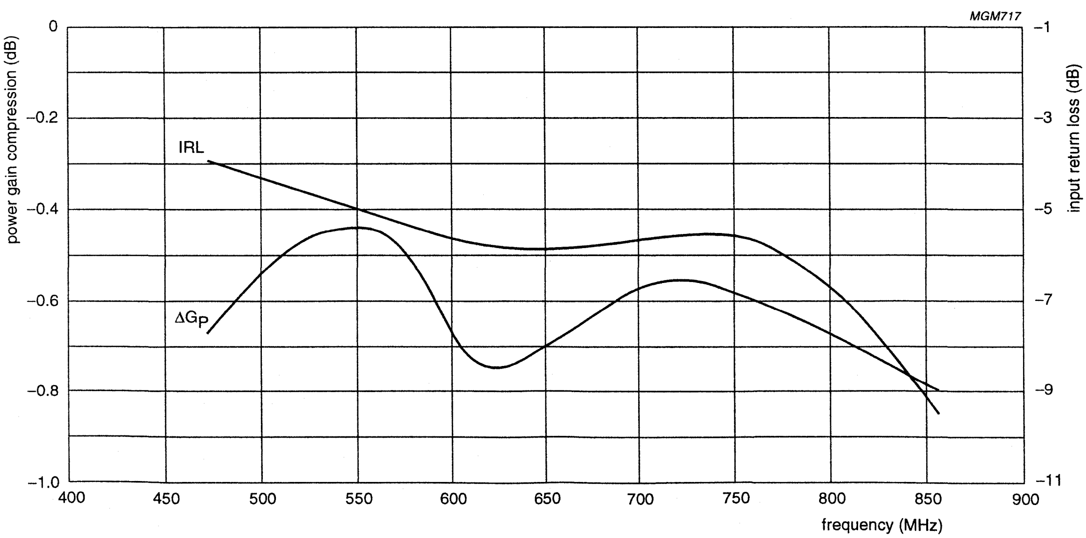


Fig.16 Input return loss and power gain compression vs. frequency.

Amplifier Overdrive Capability Test @ 860 MHz.

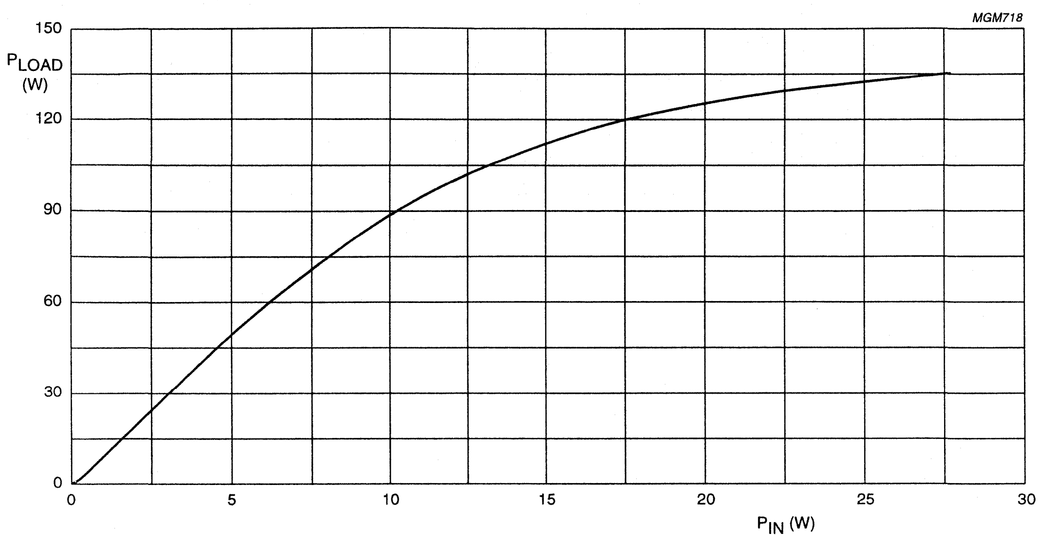


Fig.17 Load power vs. input drive power.

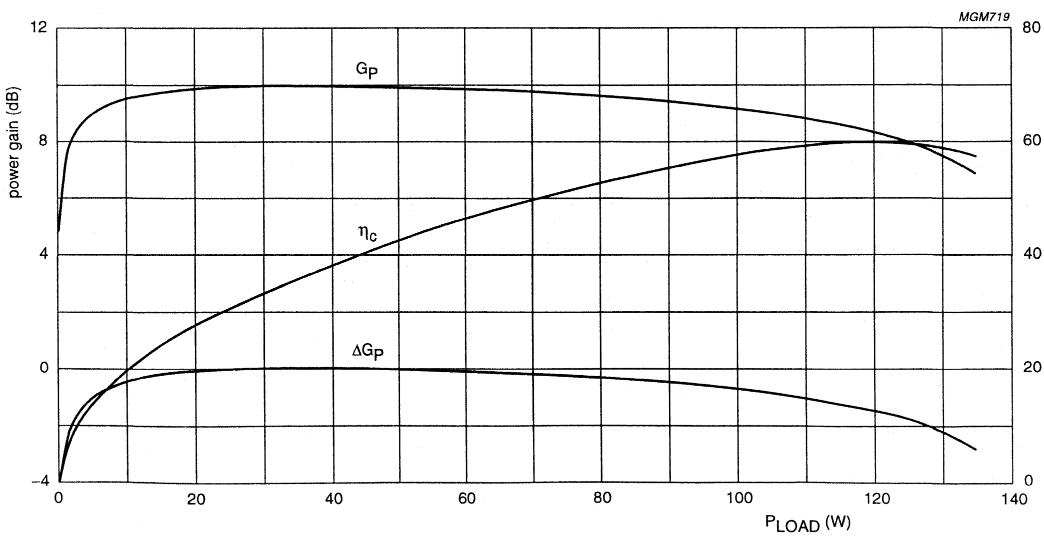


Fig.18 Power gain, power gain compression and collector efficiency vs. load power.

Two Tone Intermodulation Performance.

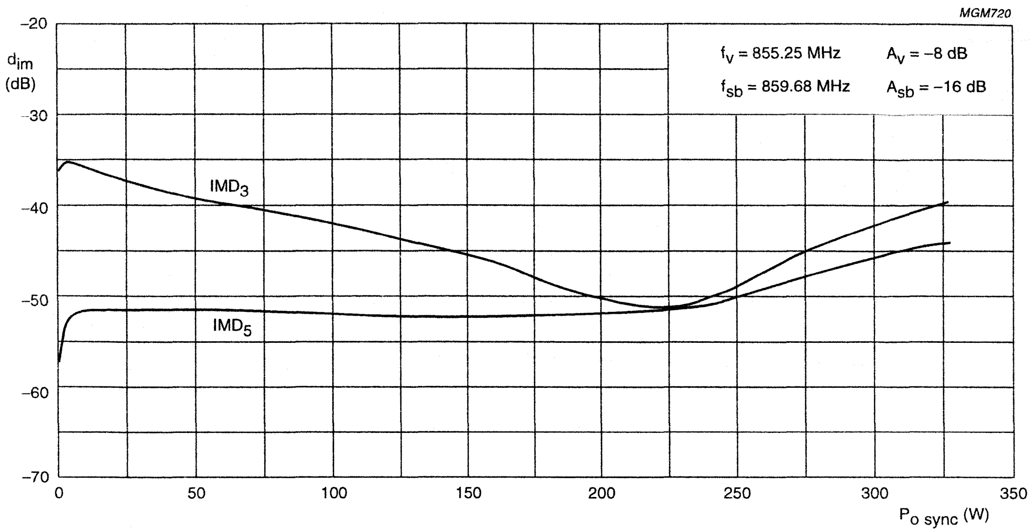


Fig.19 Two tone IMD according to System A.

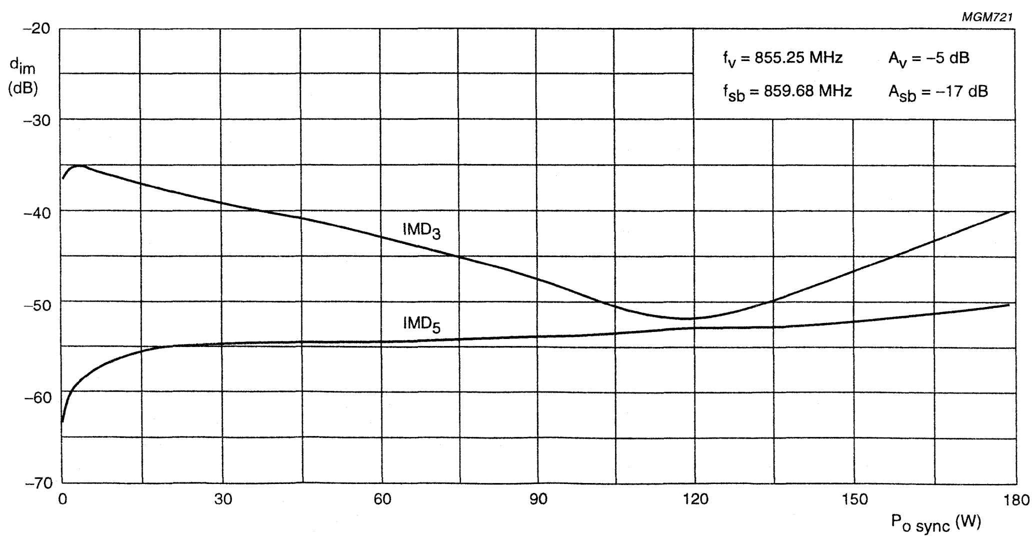


Fig.20 Two tone IMD according to System B.

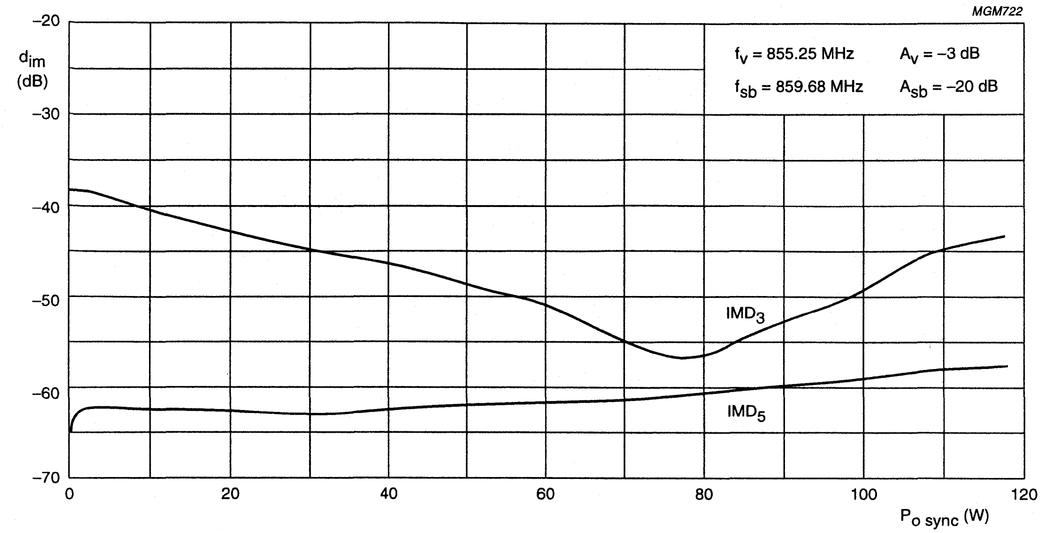


Fig.21 Two tone IMD according to System C.

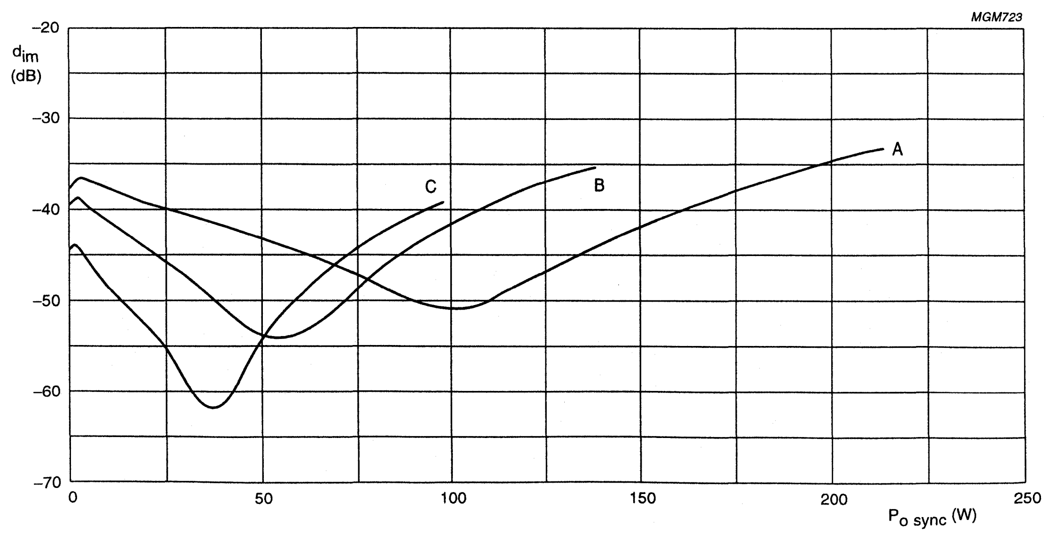


Fig.22 Tree Tone IMD at Channel 69 according to system A, B and C.

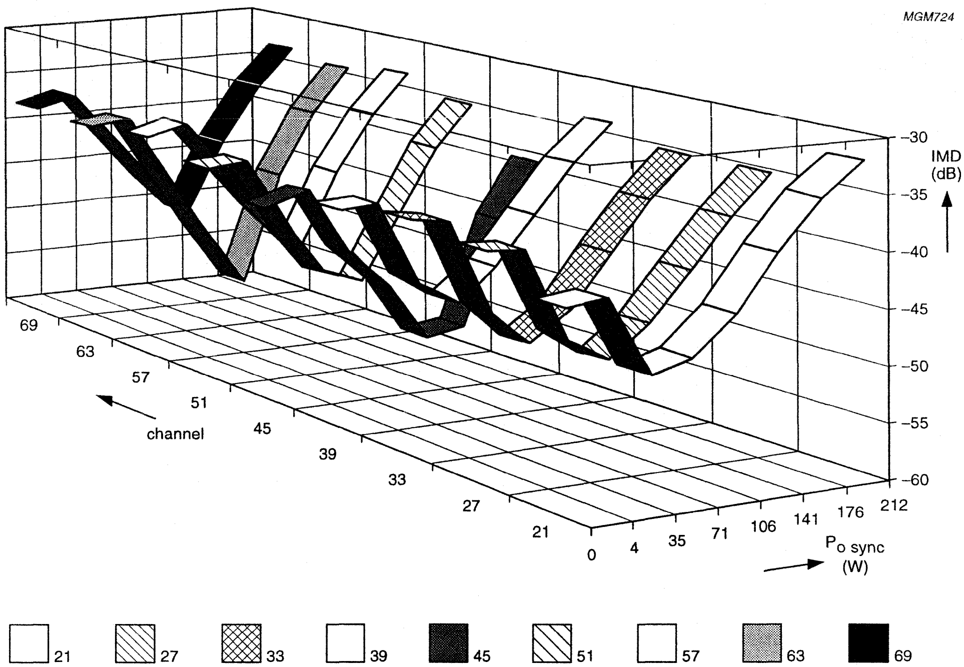


Fig.23 IMD vs. $P_{o,sync}$ level in band IV and V according to system A.

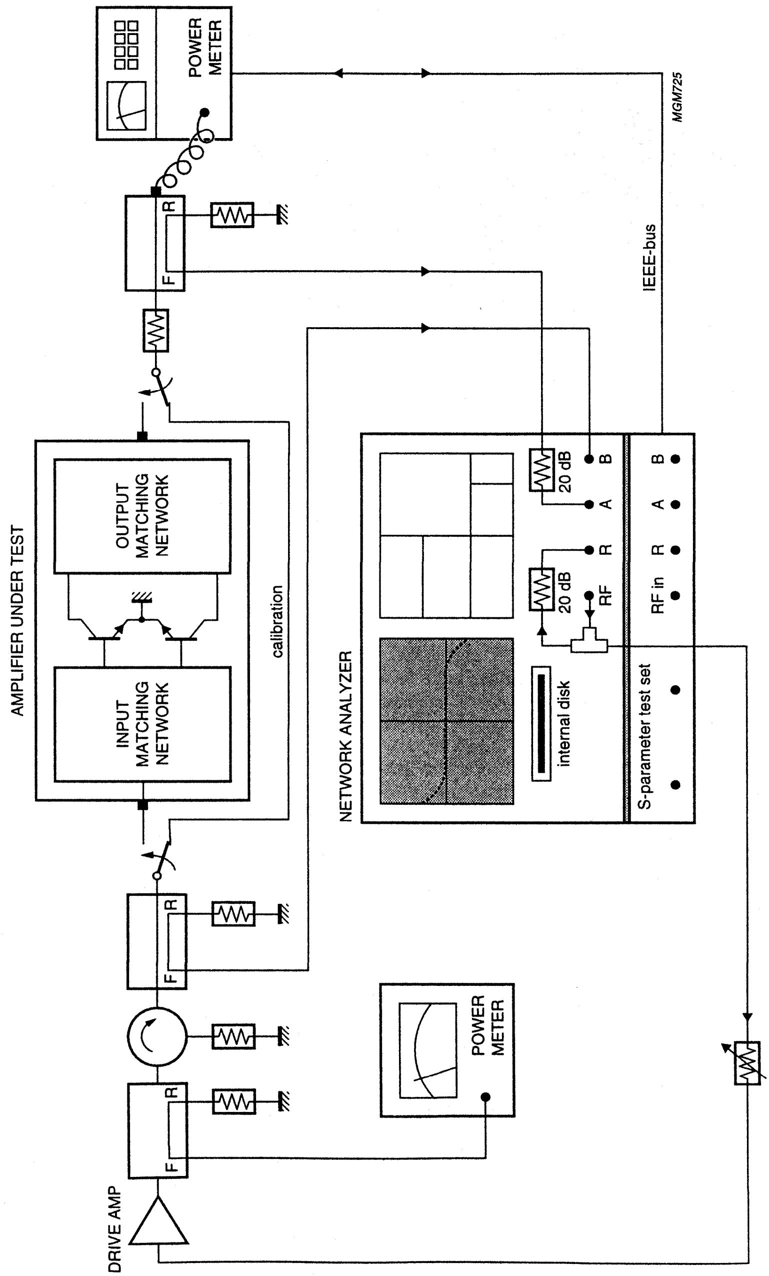
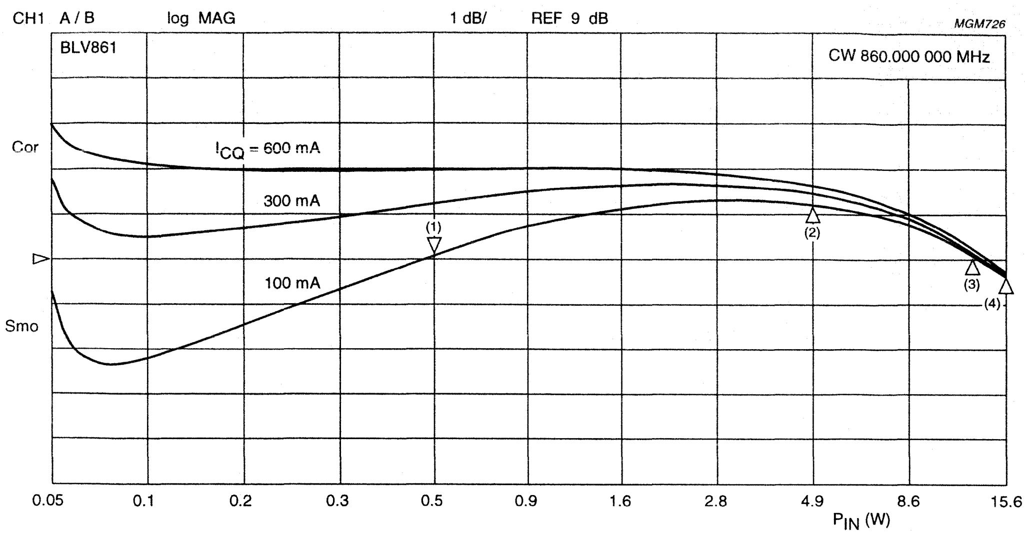
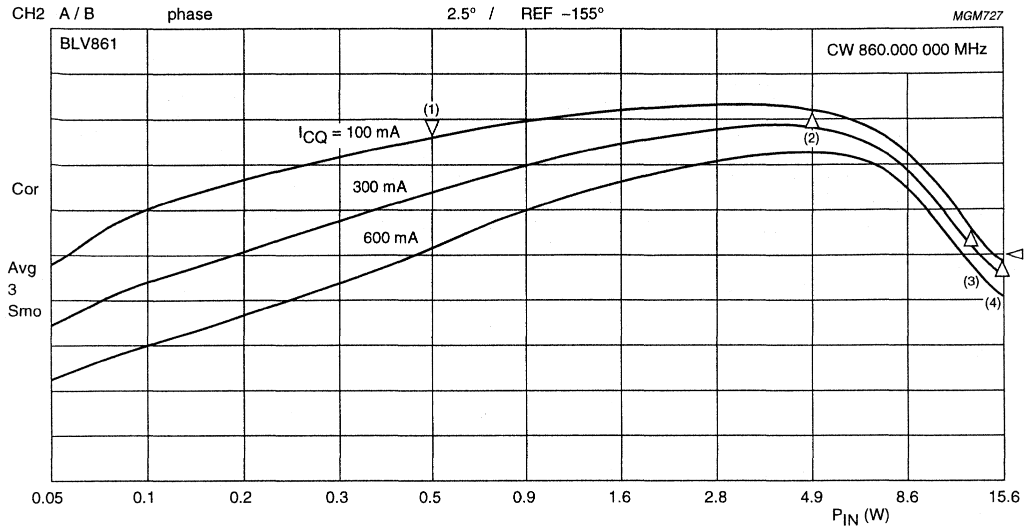


Fig.24 Setup for Power Sweep Measurement.



(1) I_{CQ} = 100 mA.
(2) I_{CQ} = 300 mA.
(3) I_{CQ} = 600 mA.

Fig.25 Amplifier Gain Distortion vs. Input Drive Power.



(1) I_{CQ} = 100 mA.
(2) I_{CQ} = 300 mA.
(3) I_{CQ} = 600 mA.

Fig.26 Amplifier Phase Distortion vs. Input Drive Power.

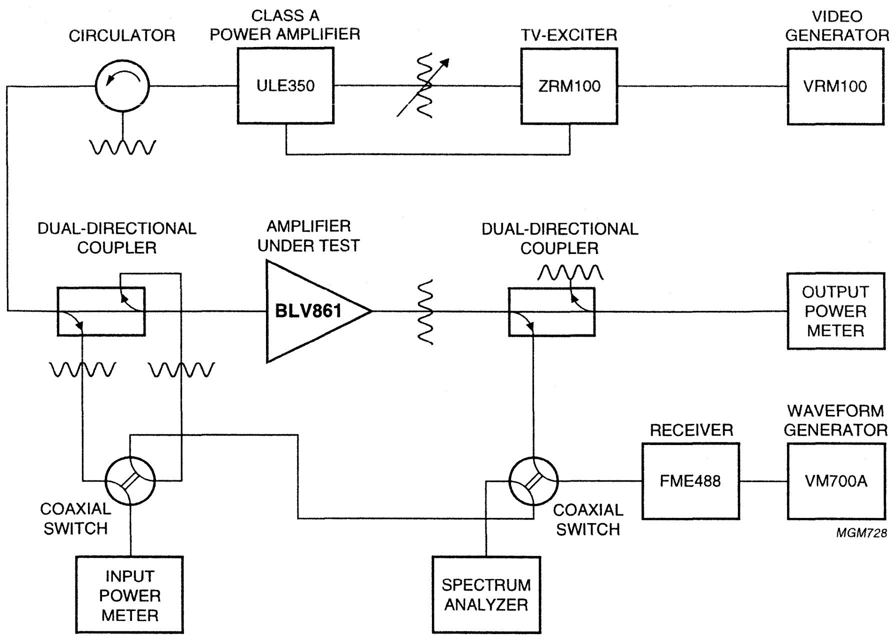


Fig.27 TV Measurement Setup.

Sync Pulse Compression vs. $P_{O,SYNC}$ @ Channel 69.

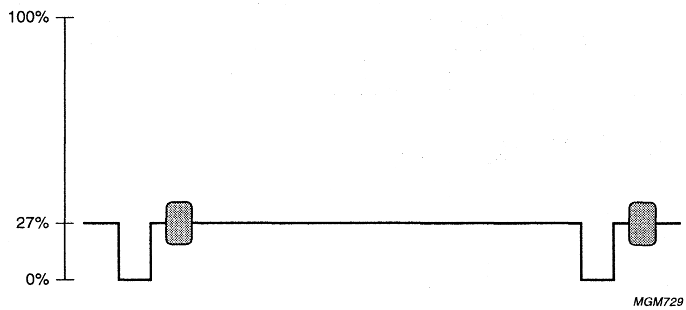


Fig.28 Black picture level (Line 18).

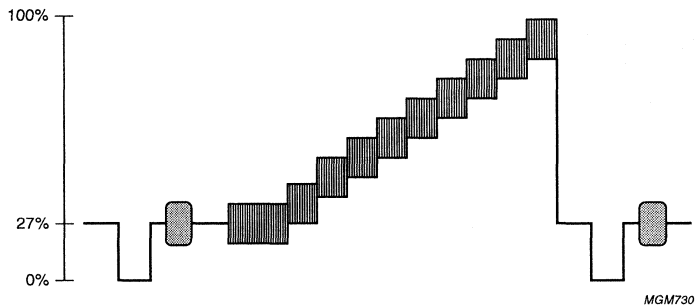


Fig.29 Compisite Video Signal, Modulated 10-steps staircase (Line 8).

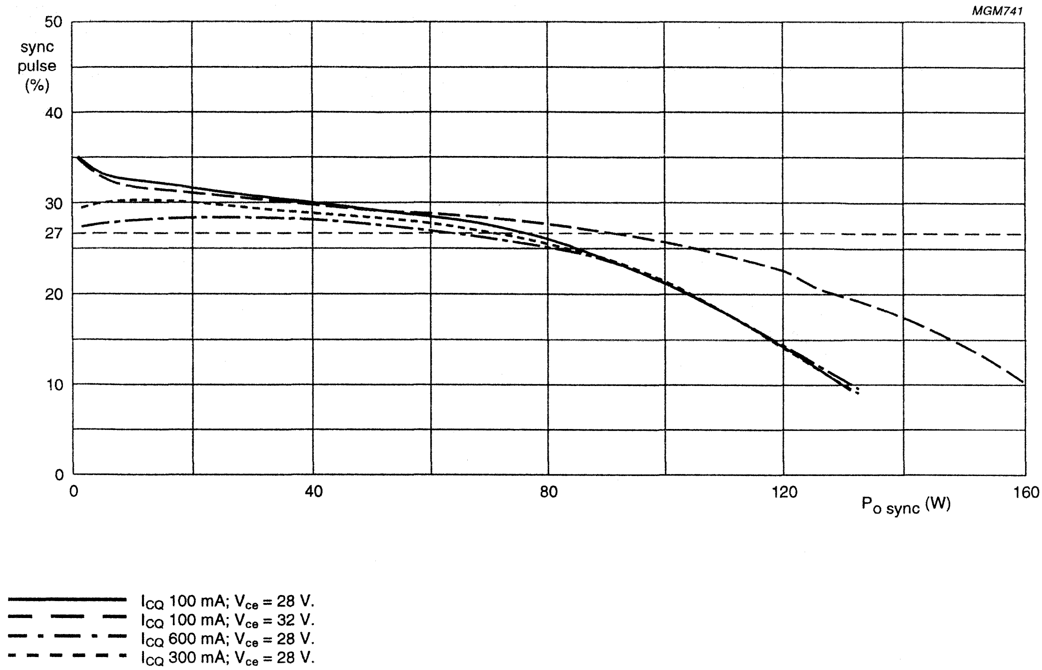


Fig.30 Sync Pulse Compression versus $P_{O,SYNC}$.

Output Sync Power Capability @ Channel 69.

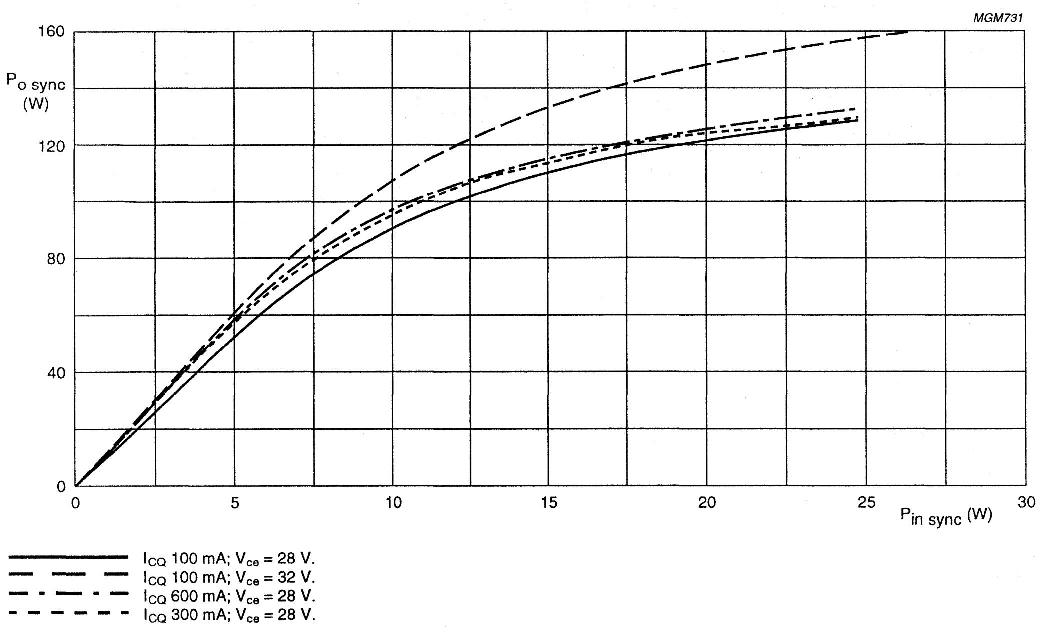


Fig.31 $P_{O,SYNC}$ versus $P_{IN,SYNC}$ @ Channel 69.

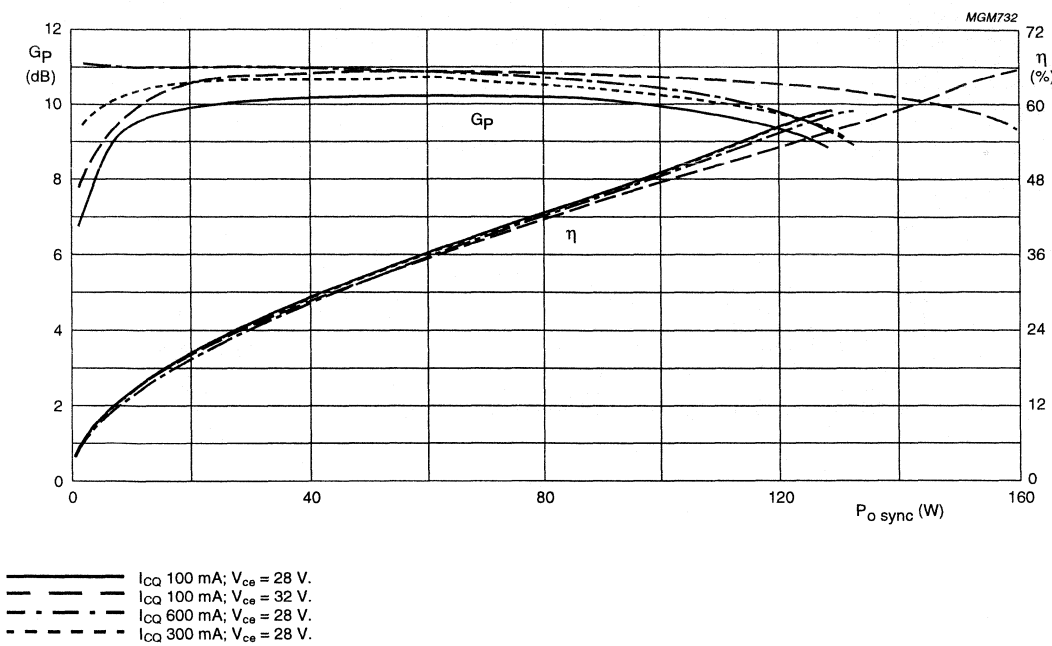
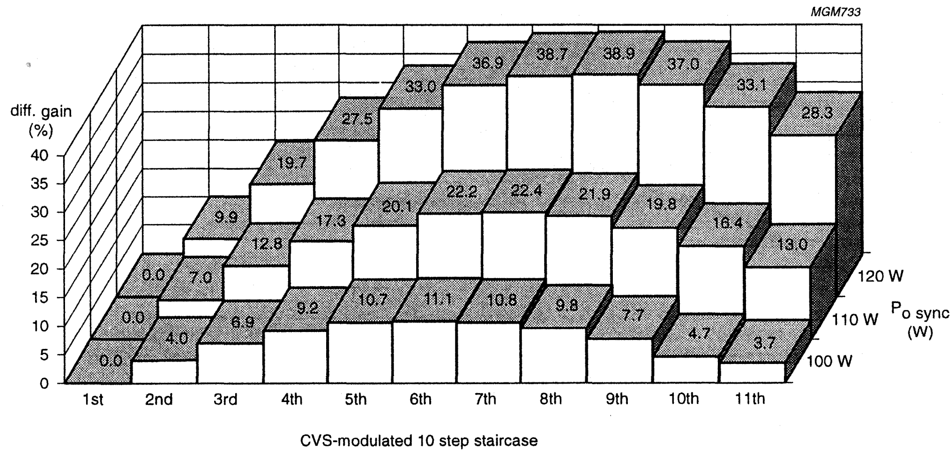


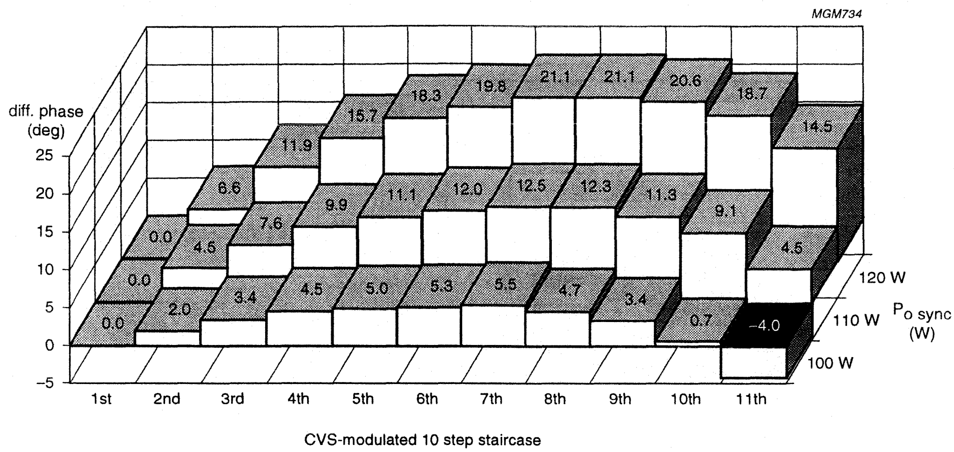
Fig.32 Power gain and collector efficiency versus $P_{O,SYNC}$ @ Channel 69.

Differential Gain and Differential Phase.



Conditions:
V_{CE} = 28 V.
I_{CQ} = 100 mA.
T_{HS} = 25 °C.
Channel = 69.

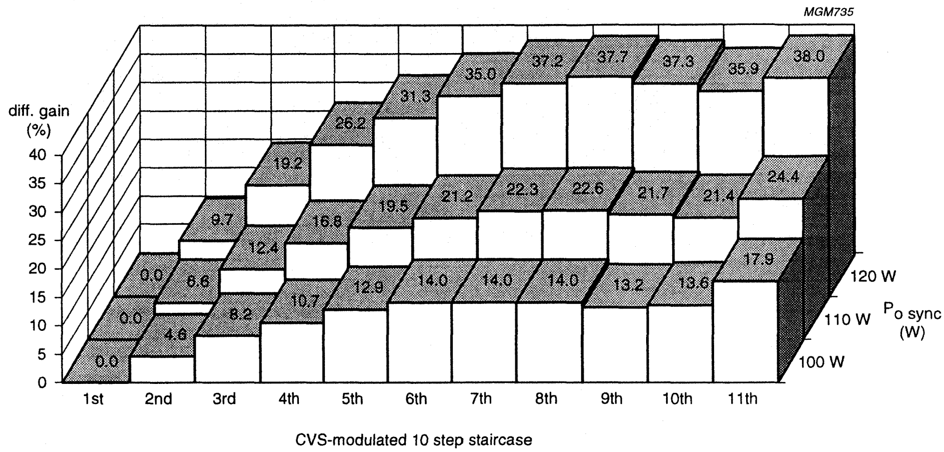
Fig.33 Differential Gain vs. Output Peak Sync Power.



Conditions:
V_{CE} = 28 V.
I_{CQ} = 100 mA.
T_{HS} = 25 °C.
Channel = 69.

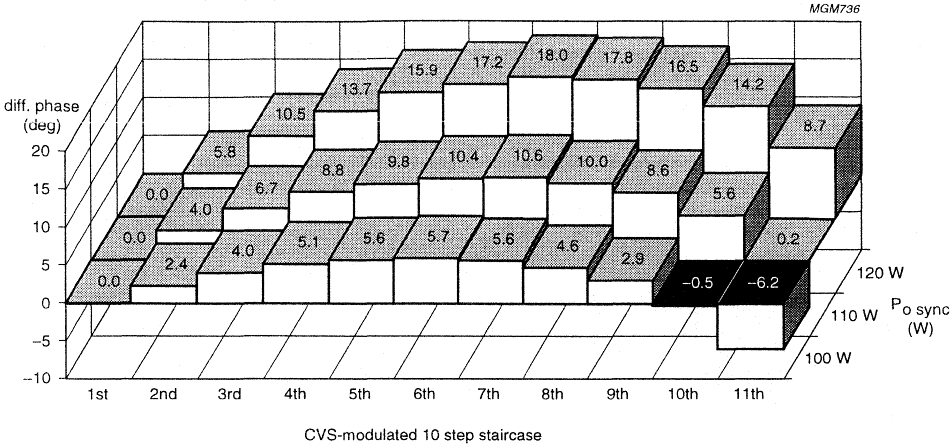
Fig.34 Differential Phase vs. Output Peak Sync Power.

Differential Gain and Differential Phase.



Conditions:
V_{CE} = 28 V.
I_{CQ} = 300 mA.
T_{HS} = 25 °C.
Channel = 69.

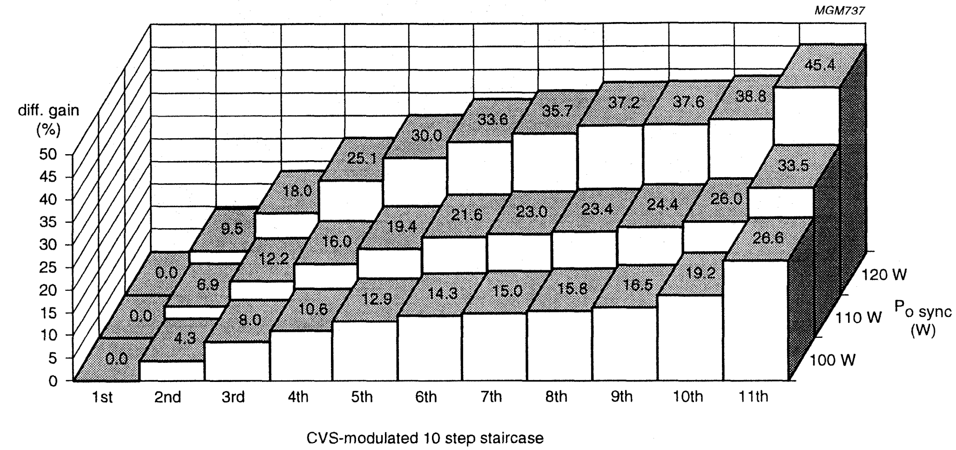
Fig.35 Differential Gain vs. Output Peak Sync Power.



Conditions:
V_{CE} = 28 V.
I_{CQ} = 300 mA.
T_{HS} = 25 °C.
Channel = 69.

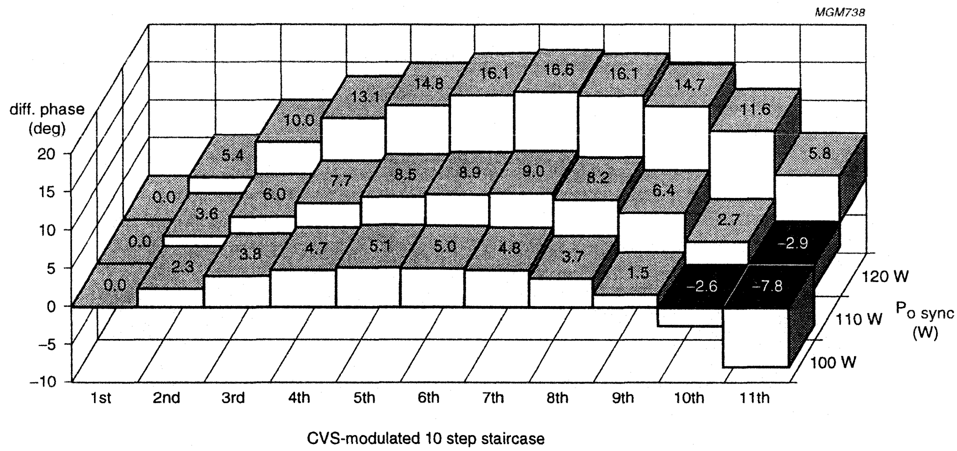
Fig.36 Differential Phase vs. Output Peak Sync Power.

Differential Gain and Differential Phase.



Conditions:
V_{CE} = 28 V.
I_{CQ} = 600 mA.
T_{HS} = 25 °C.
Channel = 69.

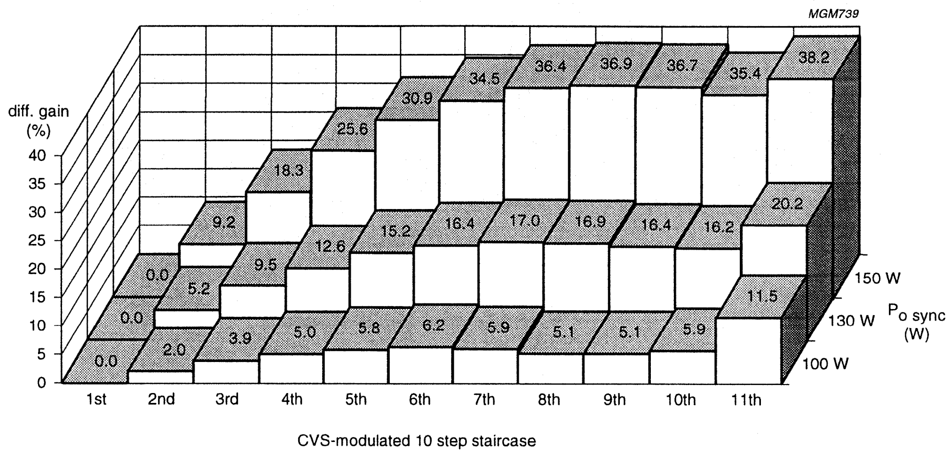
Fig.37 Differential Gain vs. Output Peak Sync Power.



Conditions:
V_{CE} = 28 V.
I_{CQ} = 600 mA.
T_{HS} = 25 °C.
Channel = 69.

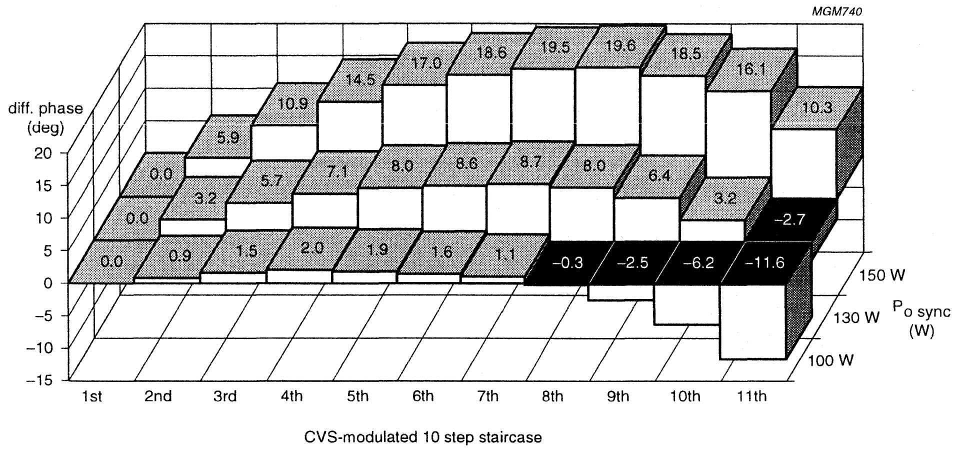
Fig.38 Differential Phase vs. Output Peak Sync Power.

Differential Gain and Differential Phase.



Conditions:
V_{CE} = 32 V.
I_{CQ} = 100 mA.
T_{HS} = 25 °C.
Channel = 69.

Fig.39 Differential Gain vs. Output Peak Sync Power.



Conditions:
V_{CE} = 32 V.
I_{CQ} = 100 mA.
T_{HS} = 25 °C.
Channel = 69.

Fig.40 Differential Phase vs. Output Peak Sync Power.

9 APPENDIX A

Tree Tone and Two Tone Power Levels

Relative power levels of a tree tone system:

$$V_{SYNC} = 1 \qquad V_{VISION} = 10^{\frac{Avision}{20}} \qquad V_{SIDEBAND} = 10^{\frac{Asideband}{20}} \qquad V_{SOUND} = 10^{\frac{Asound}{20}}$$

$$P_{SYNC} = \frac{(V_{SYNC})^2}{R}$$

$$P_{PEAK} = \frac{(V_{VISION} + V_{SIDEBAND} + V_{SOUND})^2}{R}$$

$$P_{AVG} = \frac{(V_{VISION})^2 + (V_{SIDEBAND})^2 + (V_{SOUND})^2}{R}$$

Table 10

SYSTEM	VISION	SIDEBAND	SOUND	$\frac{P_{SYNC}}{P_{AVG}}$	$\frac{P_{PEAK}}{P_{AVG}}$	$\frac{P_{SYNC}}{P_{PEAK}}$
A	0.398	0.158	0.316	3.526	2.686	1.313
B	0.562	0.141	0.316	2.293	2.384	0.962
C	0.708	0.100	0.316	1.636	2.068	0.791

Relative power levels of a two tone system:

$$V_{SYNC} = 1 \qquad V_{VISION} = 10^{\frac{Avision}{20}} \qquad V_{SIDEBAND} = 10^{\frac{Asideband}{20}}$$

$$P_{SYNC} = \frac{(V_{SYNC})^2}{R}$$

$$P_{PEAK} = \frac{(V_{VISION} + V_{SIDEBAND})^2}{R}$$

$$P_{AVG} = \frac{(V_{VISION})^2 + (V_{SIDEBAND})^2}{R}$$

Table 11

SYSTEM	VISION	SIDEBAND	$\frac{P_{SYNC}}{P_{AVG}}$	$\frac{P_{PEAK}}{P_{AVG}}$	$\frac{P_{SYNC}}{P_{PEAK}}$
A	0.398	0.158	5.446	1.687	3.228
B	0.562	0.141	2.975	1.473	2.020
C	0.708	0.100	1.956	1.277	1.532

1 ABSTRACT

For application in T.V. transposers for band IV/V (470 – 860 MHz) some wideband linear power amplifiers have been made with the BLW32 and BLW33. A single stage amplifier with BLW32 gave a minimum output power of 380 mW peak sync. at a 2-tone i.m.d. of –47 dB. The power gain was 11.4 ±0.55 dB. A similar amplifier with the BLW33 produced a minimum output of 790 mW peak sync. at the same i.m.d. and a power gain of 10.4 ±0.85 dB.
A 2-stage amplifier with the BLW32 as driver and BLW33 in the output showed a minimum output power of 750 mW peak sync. at –47 dB i.m.d. with an overall power gain of 22.5 ±2 dB.

2 INTRODUCTION

This report describes the theoretical aspects and practical realisation of some wide-band UHF power amplifiers for TV transposer service in bands IV and V (470 – 860 MHz).

The amplifiers are designed with the BLW32 and BLW33 transistors. These devices are intended for resp. 0.5 and 1 W peak sync output and are developed for ultra linear applications. For this purpose the transistors have to operate in class A.

The transistors are encapsulated in a ¼ inch capstan envelope with ceramic cap.

Because of their high gain they are excellently suited for the realisation of wide-band type amplifiers.

3 THEORETICAL CONSIDERATIONS

3.1 The equivalent circuit of the transistor input and output of the BLW32 and BLW33

For class A operation the BLW32 and BLW33 are specified as follows:

BLW32: V_{CE} = 25 V and I_C = 150 mA

BLW33: V_{CE} = 25 V and I_C = 300 mA.

Although the power gain, the input impedance and the optimum narrow band load impedance versus frequency are given in the Data sheets for the above operating points, the actual class A operation points chosen differ somewhat for the circuits described in this report.

Namely, from earlier investigations it is known that the wide-band properties are more favourable for lower load impedances. So, we have chosen for the following class A operation points:

BLW32: V_{CE} = 22.5 V and I_C = 165 mA

BLW33: V_{CE} = 22.5 V and I_C = 330 mA.

The corresponding typical gain, input and load impedances have been calculated. The values thus obtained for three frequencies are given in Tables 1 and 2.

Table 1 BLW32

f (MHz)	gain (dB)	R_i (SERIES) (Ω)	X_i (SERIES) (Ω)	R_L (SERIES) (Ω)	X_L (SERIES) (Ω)
470	16.5	4.59	1.67	41.5	39.4
636	14.0	4.42	3.61	28.9	38.0
860	11.4	4.12	5.86	17.7	33.0

Table 2 BLW33

f (MHz)	gain (dB)	R_i (SERIES) (Ω)	X_i (SERIES) (Ω)	R_L (SERIES) (Ω)	X_L (SERIES) (Ω)
470	15.0	3.60	1.90	27.1	17.4
636	12.5	3.45	3.26	21.0	18.4
860	10.1	3.19	4.90	14.5	17.3

To facilitate calculations approximate equivalent circuits for the transistor input and output impedances can be given. They are shown in Figs 1 and 2.

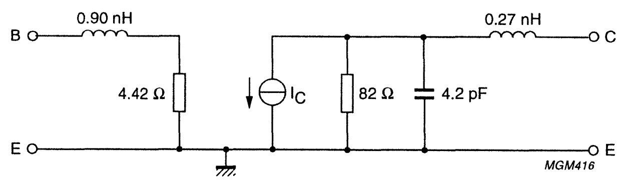


Fig.1 BLW32.

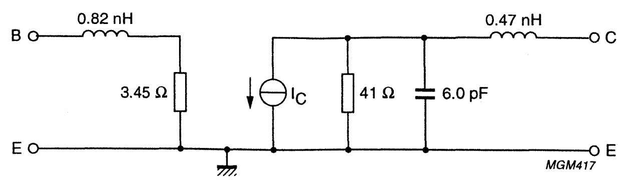


Fig.2 BLW33.

3.2 The output networks

The circuits will be designed on printed circuit boards with P.T.F.E.-fibre-glass as a dielectric with an $\varepsilon_r = 2.74$ and a thickness of 1/16 inch.

The input and output network start with a piece of stripline having a width of 6 mm, being the width of the base and collector leads. For a dielectric of 1/16 inch the characteristic impedance Z_C is 37.6 Ω. The length for the collector leads amounts to 3 mm. The base leads are different in length.

As the output impedance of both transistors is rather high a Chebyshev bandpass-filter configuration will be chosen to match it to the 50 Ω load. As will be shown later 6 elements are sufficient to obtain an acceptable VSWR through the band.

The bandpass filter is derived from a low-pass prototype having a cut-off frequency equal to the bandwidth of the final filter, i.e. 860 – 470 = 390 MHz and a characteristic resistance of 50 Ω (see Ref.1). The transformation procedure is depicted in Figs 3 to 7. These figures are for the BLW32.

To determine $C_1 = C_3$ in Fig.3 we have to keep in mind that the input (and output) RC-product remains constant with impedance transformation, so: $C_1 = C_3 = 82 \times 4.2/50 = 6.9$ pF.

Next, we determine the quantity γ being equal to: $\gamma = \frac{1}{\omega_c \times C_1 \times R}$

In which ω_c is the cut-off frequency of the low-pass prototype and $C_1 \times R$ is the already mentioned time constant, so:

$$\gamma = \frac{1}{2 \times \pi \times 390 \times 10^{6} \times 6{,}9 \times 10^{-12} \times 50} = 1{,}183$$

Then L_2 can be calculated according to: $L_2 = \{\frac{R}{\omega_c}\}\{\frac{2\gamma}{\gamma^2 + 0{,}75}\}$

in which R is the characteristic resistance of the filter being 50 Ω, so:

$$L_2 = \{\frac{50}{2 \times \pi \times 390 \times 10^{6}}\}\{\frac{2 \times 1{,}183}{1{,}399 + 0{,}75}\} = 22{,}46\ \text{nH}$$

The transformation from low-pass to bandpass is made by:

1. Shunting each capacitor by an inductor and
2. Putting the capacitor in series with each inductor, such that resonance is obtained at the geometric mean frequency of the band: $f_O = \sqrt{860.470} = 635.8$ MHz

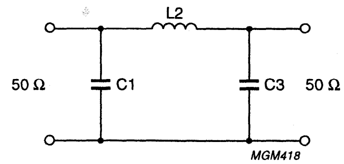


Fig.3

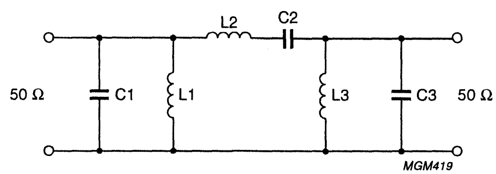


Fig.4

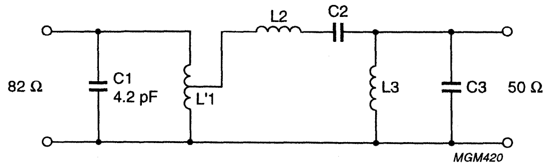


Fig.5

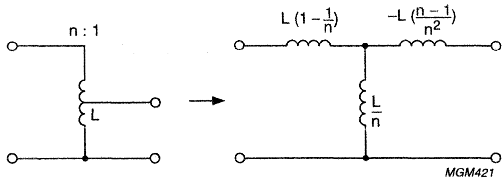


Fig.6

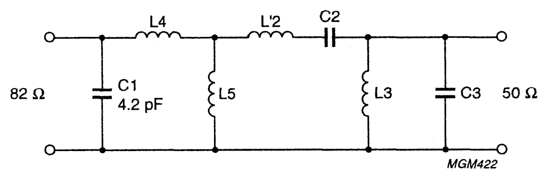


Fig.7

This means in Fig.4 that:

$L_1 = L_3 = 9.081$ nH

$C_2 = 2.79$ pF

Now we transform the input part of the filter to the actual output impedance of the transistor (see Fig.5). This is done with an ideal transformer having a primary inductance, $L'_1 = 82/50.9.081 = 14.89$ nH and a transformation ratio n : 1 in which

which $n = \sqrt{82/50} = 1.281$

This ideal transformer is subjected to a Norton transformation (see Fig.6) in which the inductances become 3.27 nH, 11.62 nH and –2.55 nH resp. The final situation is then depicted in Fig.7 with $L_4 = 3.27$ nH, $L_5 = 11.62$ nH and $L'_2 = L_2 - 2.55$ nH $= 22.46 - 2.55 = 19.91$ nH.

The resulting maximum VSWR is equal to:

$S = \{(x^3 + 1)/(x^3 - 1)\}^2$ in which:

$$X = \gamma + \sqrt{\gamma^2 + 1}$$

For our filter this becomes: S = 1.22, which is a very acceptable value justifying the conclusion that the number of filter elements is sufficient.
The next step is the transformation of this filter to a stripline circuit. If a transmission line is shorter than 1/8 of a wavelength the following equivalence is reasonably accurate (see Fig.8):

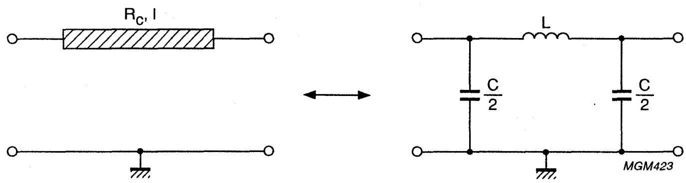


Fig.8

$$L = \frac{R_C \times l}{v} \text{ and } C = \frac{l}{R_C \times v}$$

in which v is the propagation speed being 3.10^8 m/s for air-line. Starting from Fig.7 we must keep in mind that C_1 and part of L_4 (viz. 0.27 nH) are inside the transistor.
The inductors are then replaced by striplines. The consequence of this transformation is that at some points in the circuit parasitic capacitances are introduced.
This can be corrected by adjusting the values of L_5 and C_3. A second reason for correcting the latter is its parasitic series inductance. The remaining part of L_4 is composed of 2 pieces of stripline with different characteristics impedances. The part with the lower R_C serves to accomodate the collector lead of the transistor. C_2 has a parasitic series inductance of appr. 1 nH which must be subtracted from L_2'.
The remaining part is split up in 2 equal pieces on both sides of C_2. The result of the transformation described above is shown in Fig.9 and Table 3.

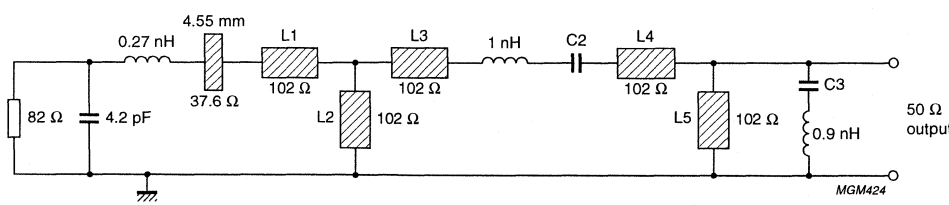


Fig.9 See also Table 3.

An exact analysis of this circuit results in a maximum output VSWR of 1.66 which is rather high. Therefore the complete circuit is subjected to a computer optimization procedure with the object to reduce the maximum output VSWR to the lowest possible value. The results are given in Table 3.

Table 3

ELEMENT	BEFORE OPTIM.	AFTER OPTIM.	UNIT
l_1	7.15	6.84	mm
l_2	28.4	27.7	mm
l_3	27.8	29.8	mm
C_2	2.79	2.76	pF
l_4	27.8	29.8	mm
l_5	26.7	33.4	mm
C_3	5.14	4.01	pF
S_{max}	1.66	1.35	–

As a final step the practical dimensions of the striplines must be determined. the printed-circuit board material is P.T.F.E. fibre-glass with a thickness of 1/16 inch and a dielectric constant ε_r of 2.74. The lines with R_C = 102 Ω must have a width of 1 mm. The length reduction factor is 1.43. The collector pad (R_C = 37.6 Ω) must have a width of 6 mm and its length reduction factor is 1.52. The results of the latter transformation can be found in the final circuit diagram and parts list.

3.3 The input networks

The approach followed for these networks is rather similar to those described in Refs 2 and 3. However, there is one exception:

Because of the higher input impedance of the BLW32, as compared to the BLW98, a smaller amount of transformation is required. As a consequence of this a single section matching network is sufficient. Generally speaking it can be said that this section must have a loaded Q-factor of appr. 4 to produce the required gain compensation.

This means that the total inductive reactance (of transistor and matching network) must be 4 times the input resistance of the transistor (see Fig.10).

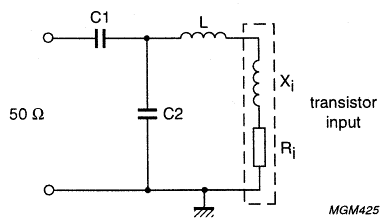


Fig.10

The tuning of this circuit is then at appr. 860 MHz.

The single section transforms the transistor impedance to a value above 50 Ω, so that some ‘back-transformation’ is required. This is done by reducing the value of the blocking capacitor C_1 (8.2 pF instead of 100 pF).

In case of the BLW33 the input impedance is somewhat lower, so a 2 section network is advisable. Here, the blocking capacitor is 100 pF.

The final steps are the same as in the previous section, viz. transformation to stripline and computer optimization. The results can again be found in the circuit diagrams.

4 THE SINGLE AMPLIFIERS WITH BLW32 AND BLW33

4.1 Practical considerations

On previous pages the theoretical approach has been discussed. In practice it was the intention to realize small compact amplifiers on a printed-circuit board with the input and output terminals (R_C = 50 Ω) in-line for easy cascading of several amplifiers.

The printed-circuit board needs to be double copper clad and has a P.T.F.E. fibre-glass dielectric for low losses at UHF. With a typical ε_r of 2.74 we had the choice between a thickness of 1/16 and 1/32 inch.

In principle 1/32 inch is possible but especially the 102 Ω lines in this design become so narrow, that the risk of under etching is too high.
So, we have decided to use a dielectric of 1/16 inch, what means that these 102 Ω lines are 1 mm wide.

Another problem being met with the application of 1/32 inch is the very small surface for soldering of the multi-layer chips and also an unusual ratio between the width of chip and track.

Figure 11 shows the circuit diagram of the BLW32 class A amplifier with biasing, whilst in Fig.12 the circuit is drawn for the BLW33. Both circuits contain a bias network with a PNP transistor type BD136. The lists of components are given in Tables 7 and 8.

The printed-circuit boards are in Figs 13 and 14.
For a correct earthing the upper earth sheet parts are directly connected to the lower sheet by soldering copper straps at the edges of the printed-circuit board.

The emitters were grounded as short as possible by applying copper straps under the emitter leads. For that reason the holes in the board were square instead of round.

All components are situated on one side of the board viz. the side of the tracks.

The transistors were screwed to an extruded aluminium heatsink, resulting in an average stud temperature of appr. 50 °C.
In both circuits tuning capacitors are applied. They are of the film dielectric type with three tags. Both earth terminals are fed through holes and soldered to the upper and lower earth plane.

In the experimental phase, the coupling capacitors in the collector bandpass sections are of the ‘Micro thin-trim’ type 1.0 – 4.0 pF. Later, they can probably be replaced by fixed multilayer chip capacitors.

The coaxial connectors are of the SMA 50 Ω type. They are soldered to the upper and lower earth plane.

In general, earth connections have to be made as short as possible.

4.2 Practical optimization method

Both prototypes were built according to the result of the theoretical part. It proved that such a theoretical approach was very valuable. It led, via some relatively small modifications to the ultimate design.

Optimization on a small signal basis has been done with the circuits inserted in a network analyzer chain, having swept S (scattering)-parameter facilities. From this set-up one can examine under dynamical conditions the effect on the power gain (represented by S_{21}), input- and output impedances (resp. S_{11} and S_{22}) and feedback (S_{12}) by tuning and modifications on the circuit of the amplifier.

The correction of power gain over the whole 470 – 860 MHz range is arranged by applying appropriate mismatch. The resulting high VSWR, especially at low frequency, is not reduced in an equalizer.

So, tuning on an S-parameter set-up means that the S_{21} has to be optimized for flat gain, and at the same time the input reflection damping S_{11} tuned for minimum at the highest frequency of 860 MHz.

4.3 Measured results

Figures 16 to 21 show the practical results for resp. the BLW32 and BLW33 amplifiers.
The results for two units are both given. They are numbered (1) and (2).

For a clear interpretation of the S_{11} and S_{22} readings the expression for the reflection damping and some figures are given in Table 4:

Table 4 Refl. damping = 20 log (S + 1)/(S – 1) dB in which S is the voltage standing wave ratio (VSWR)

REFL. DAMPING (dB)	REFL. COEFF.	S
0	1	∞
4	0.631	4.42
8	0.398	2.32
12	0.251	1.67
16	0.158	1.38
20	0.1	1.22
24	0.063	1.13
28	0.04	1.08

Examining Figs 16 and 19 one will see that in both cases, the reflection damping is about 20 dB so the input VSWR is about 1.2 near 860 MHz, whilst the output VSWR, with respect to 50 Ω, varies between 3 and 1.06 over the band.

After optimization at small signals, the i.m.d. has been measured in a 2-tone set-up. Although it is advised to apply the 3-tone test method for determining the i.m.d. in case of TV systems, the 2-tone test shows a good correlation with the former (see Ref.3).

In practice this means that for a 3-tone test with the tones at –7, –8 and –16 dB below the 0 dB peak sync. level, the in-band i.m. product has to be at least –60 dB down, whilst the same amplifier has to show a distance of two i.m. products d_3 of at least –47 dB with respect to one of the equal tones in case of the 2-tone test with equal peak output power.

The results are given in the curves of Figs 22 to 25.

For these amplifiers, of which two each have been constructed and measured, the results are according to the expected ones for wide-band operation. At three channels the peak sync power for a 3-tone i.m.d. of –60, –56 and –52 dB has been measured too. Table 5 gives an impression of the average –60 dB results of the BLW32 and BLW33.

Table 5

CHANNEL NO.	BLW32	BLW33
21 (471.25 MHz)	445 mW	1286 mW
39 (615.25 MHz)	671 mW	1308 mW
70 (863.25 MHz)	500 mW	941 mW
P_O sync. for –60 dB i.m.d. (average of two amplifiers)		

Tables 10 and 11 show the more complete test results.

Comparing the afore mentioned 3-tone (–60 dB) results with the 2-tone (–47 dB) figures it appears that: As for the single amplifiers the typical low frequency decoupling elements are divided over the bias circuit and the amplifier circuit. This was done because in case of concentrating all low-frequency decoupling elements on the bias board, parasitic oscillations occurred.

To get some idea of the reproducibility of practical amplifiers, two equivalent units have been built. They are screwed to heatsinks having a thermal resistance of appr. 2 °C/W. So for an average ambient temperature of 25 °C the stud temperature rises to about 48 °C for a power dissipation of about 11.5 W.

For the single amplifiers described, the straight forward method of small signal tuning at the S-parameter equipment and afterwards the 2-tones test was followed. Via this method reliable results could be obtained.
However in case of the double amplifier it appeared to be rather difficult to find the optimum between an acceptable flat gain curve and sufficient output power with low i.m.d.

Because there is a correlation between the single tone 1 dB compression point and the i.m.d. of a linear amplifier, the following dynamic way of tuning was applied: For the BLW33 compression starts around 2 W output. The gain of the complete amplifier is appr. 20 dB so appr. 20 mW (+13 dBm) drive power should be sufficient. This amount of swept power is available from the sweep oscillator HP8620C in combination with RF plug-in unit HP86222A. Because of internal ALC the swept output power level is very stable and almost unaffectable by the strong input VSWR variation of the BLW32 amplifier.

- For the BLW32, the channel 21 and 39 results are somewhat better (3 – 18%) when measured under 3-tone conditions, whilst the channel 70 figures are about 6% lower.
- In case of the BLW33, the 3-tone results are somewhat different for both tested units. As an average they are in between those of the 2-tone test.
- The gain figures are about the same. For a description of the 2-tone and 3-tone test chain and the way of testing one is referred to Ref.3.

5 COMBINED AMPLIFIER WITH BLW32 AND BLW33

5.1 Practical considerations

As an experiment both amplifiers, being tuned for optimum performance, were cascaded. In that case the output of the BLW32 has to accept the mismatch, specially at lower frequencies, caused by the BLW33 amplifier.

The gain (S_{21}) becomes appr. 20 dB, whilst the input and output reflection damping of the combination show somewhat different values. However, the trend is the same.

From this experiment the idea came to integrate both amplifiers on one printed-circuit board. The easiest solution was the direct connection of the two 50 Ω striplines, maintaining the blocking capacitor C_1 (see Fig.12) and concentrating the elements C_{11} (see Fig.11) and C_2 (see Fig.12) in a new single tuning element.

Figure 26 shows the total circuit diagram, Fig.15 the printed-circuit board of the amplifier part and Table 9 the list of components.

To create an amplitude variation the sweep generator is amplitude modulated (AM input) with a square wave pulse generated with a PM5715 pulse generator.

The output of the amplifier under test is now again attenuated (about 20 dB), detected and supplied to an oscilloscope being horizontally driven by means of the available sweep output of the HP8620C.

Figure 27 shows the block diagram of the measuring set-up, and Figs 28 to 30 screen pictures of the swept output power for different input levels (+7, +10 and +13 dBm) in which compression is clearly shown. From above mentioned experiments it appeared that the blocking capacitor, C_{12} in Fig.26, better could be decreased to 8.2 pF.

5.2 Measured results

Being tuned for a good large signal behaviour the i.m.d. results of both amplifiers constructed are given in Figs 31 and 32. Figures 33 and 34 resp. show the gain curves for an input power of 5 mW (+7 dBm) and Figs 35 to 37 the S-parameter results.

The peak sync. power for a 3-tone i.m.d. of –60, –56 and –52 dB has been measured at three channels. Table 6 shows the –60 dB results for the combination no. (2).

Table 6

CHANNEL NO.	BLW32 – BLW33
21 (471.25 MHz)	1045 mW
39 (615.25 MHz)	895 mW
70 (863.25 MHz)	587 mW
P_O sync for –60 dB i.m.d. (amplifier no. 2)	

Table 12 shows the more complete test results.

Comparing the 2-tone (–47 dB) and 3-tone (–60 dB) results it appears that:

- The combination BLW32/33 shows appr. equal results for channels 21 and 39. However the channel 70 results are somewhat lower.
- The gain figures are about the same.

6 CONCLUSIONS

On preceding pages the theoretical and practical designs have been described of some wide-band (470 – 860 MHz) high quality linear amplifiers, utilizing the BLW32 and BLW33 transistors operating in class A.

The class A operation points, in these wide-band applications, differ somewhat from those being published in the data sheets for narrow band applications. This led to a better wide-band loading, what again resulted in a better i.m.d. performance.

The flatness of the power gain versus frequency is obtained by applying an increasing amount of mismatch when the frequency becomes lower.

This can be seen as a disadvantage of the system, because the preceding driver stage has to accept that mismatch. In the present combination, however, the driver is so large that no difficulties are experienced.

7 RECOMMENDATIONS

A flat power gain characteristic combined with a low input VSWR may be obtained by:

1. Applying an equalizing network at the input.
2. A coaxial isolator or circulator at the input.
   However, these devices have restricted bandwidths.
3. Applying the method in which two equal amplifiers have been connected in parallel with the aid of two wide-band 3 dB –90 °C coaxial hybrids on a 50 Ω basis. In that configuration the output power will be nearly doubled, whilst the input VSWR of the system becomes max. 1, 2 a value mainly given by the properties of these devices. The reflected power will be absorbed in the resistor matching the isolated port.

   A suitable type of hybrid is the ultra-miniature 3 dB –90 °C coupler, model 10264-3 (range 0.5 – 1.0 GHz) or 1H 0264-3 (range 0.44 – 0.88 GHz) from Anaren Microwave Inc.

   Compared with the rest of the components such an arrangement is rather expensive.

   If one wishes to construct the couplers oneself it can be done with 'wire-line' type BH 10 of Sage. The assembling, however, asks for special tools.

In this report a number of measuring methods are given. It could be considered to apply the swept compression test method with an external wide-band amplifier (no need for linearity) and the external ALC possibility for testing amplifiers asking for more drive power.

8 REFERENCES

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Ref.2:
O. Pitzalis, Jr. and R.A. Gilson – Tables of impedance matching networks with approximate prescribed attenuation versus frequency slopes.
IEEE Transactions on microwave theory and techniques, Vol. MTT-19, no. 4, April 1971, pp. 381-386.

Ref.3:
M.J. Köppen – Wide-band linear power amplifier (470 – 860 MHz) with two transistors BLW98; appl. report no. ECO7905.

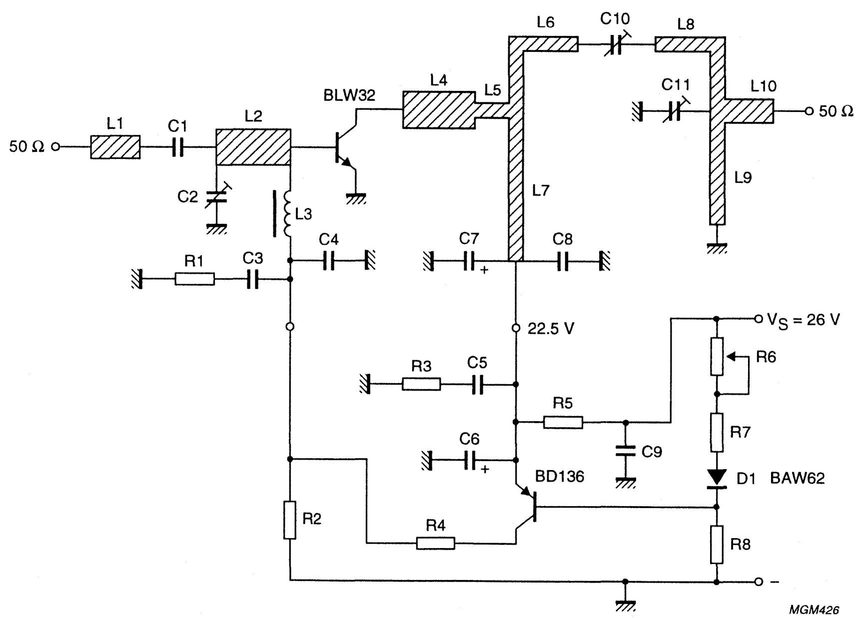


Fig.11 BLW32 circuit.

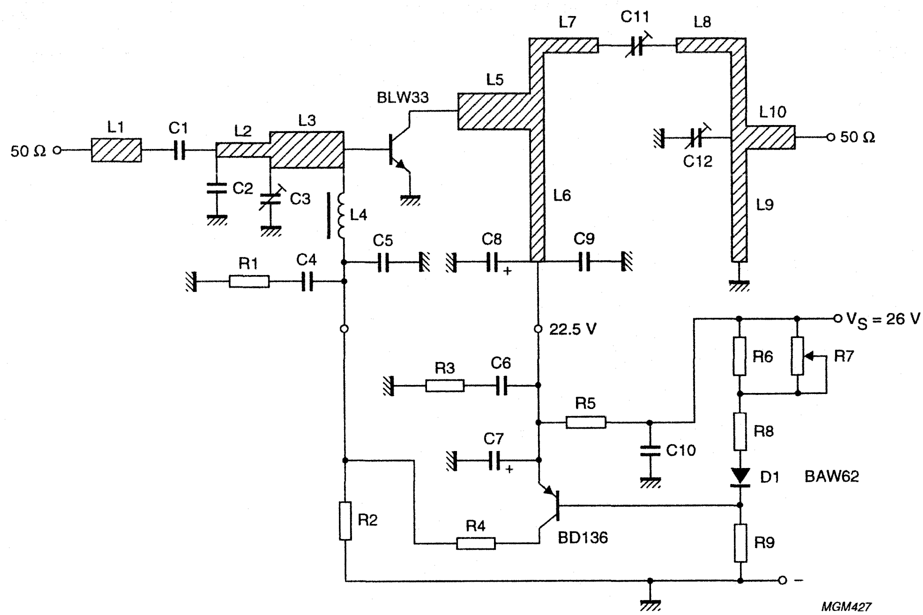


Fig.12 BLW33 circuit.

Table 7 List of components of the BLW32 amplifier (Figs 11 and 13)

C_1	8.2 pF	multilayer ceramic chip capacitor, ATC (Amercian Technical Ceramics) type 100A-8R2-J-Px-50
$C_2 = C_{11}$	1 to 3.5 pF	film dielectric trimmer (cat. no. 2222 809 05001)
$C_3 = C_9$	100 nF	polyester capacitor
$C_4 = C_8$	100 pF	multilayer ceramic chip capacitor (cat. no. 2222 852 13101)
C_5	470 nF	polyester capacitor
$C_6 = C_7$	6.8 µF; 63 V	electrolytic capacitor
C_{10}	1 to 4 pF	micro thin-trim, Tekelec Airtronic part no. AT9401-4-SL1
$L_1 = L_{10}$	stripline (Z_C = 50 Ω)	width 4.0 mm
L_2	stripline (Z_C = 37.6 Ω)	11.5 × 6.0 mm^2
L_3	470 nH	microchoke
L_4	stripline (Z_C = 37.6 Ω)	3.0 × 6.0 mm^2
L_5	stripline (Z_C = 102 Ω)	4.8 × 1.0 mm^2
$L_6 = L_8$	stripline (Z_C = 102 Ω)	20.8 × 1.0 mm^2
L_7	stripline (Z_C = 102 Ω)	19.3 × 1.0 mm^2
L_9	stripline (Z_C = 102 Ω)	23.4 × 1.0 mm^2
$R_1 = R_3$	10 Ω (±5%)	carbon resistor CR25 type
R_2	33 Ω (±5%)	carbon resistor CR25 type
R_4	220 Ω	power metal film resistor PR37 type
R_5	18 Ω (±5%)	power metal film resistor PR52 type
R_6	220 Ω	cermet preset potentiometer
R_7	150 Ω (±5%)	carbon resistor CR25 type
R_8	1.8 kΩ (±5%)	carbon resistor CR25 type
D_1		BAW62

Table 8 List of components of the BLW33 amplifier (Figs 12 and 14)

$C_1 = C_5 = C_9$	100 pF	multilayer ceramic chip capacitor (cat. no. 2222 852 13101)
C_2	2.7 pF	multilayer ceramic chip capacitor, ATC type 100A-2R7-B-Px-50
$C_3 = C_{12}$	1 to 3.5 pF	film dielectric trimmer (cat. no. 2222 809 05001)
$C_4 = C_{10}$	100 nF	polyester capacitor
C_6	470 nF	polyester capacitor
$C_7 = C_8$	6.8 µF; 63 V	electrolytic capacitor
C_{11}	1 to 4 pF	micro thin-trim, Tekelec Airtronic part no. AT 9401-4-SL1
$L_1 = L_{10}$	stripline (Z_C = 50 Ω)	width 4.0 mm
L_2	stripline (Z_C = 102 Ω)	9.6 × 1.0 m^2
L_3	stripline (Z_C = 37.6 Ω)	5.3 × 6.0 m^2
L_4	470 nH	microchoke
L_5	stripline (Z_C = 37.6 Ω)	3.0 × 6.0 m^2
L_6	stripline (Z_C = 102 Ω)	16.2 × 1.0 m^2
$L_7 = L_8$	stripline (Z_C = 102 Ω)	21.7 × 1.0 m^2
L_9	stripline (Z_C = 102 Ω)	20.4 × 1.0 m^2

$R_1 = R_3$	10 Ω (±5%)	carbon resistor CR25 type
R_2	33 Ω (±5%)	carbon resistor CR25 type
R_4	220 Ω (±5%)	power metal film resistor PR37 type
R_5	10 Ω (±5%)	enamelled wire-wound resistor WR0617E style
R_6	1 kΩ (±5%)	carbon resistor CR25 style
R_7	220 Ω	cermet preset potentiometer
R_8	150 Ω (±5%)	carbon resistor CR25 style
R_9	1.8 kΩ (±5%)	carbon resistor CR25 style
D_1		BAW62

Printed-circuit boards 1/16 inch PFTE double CU clad

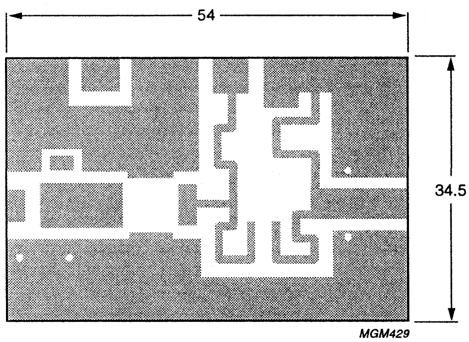


Fig.13 Printed-circuit board BLW32.

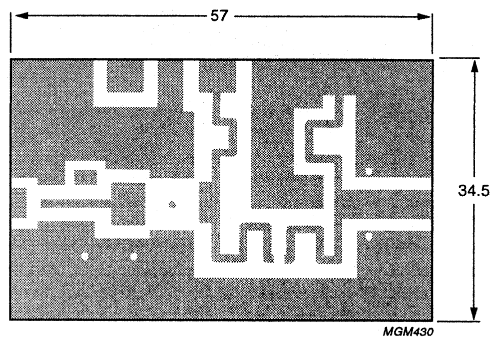


Fig.14 Printed-circuit board BLW33.

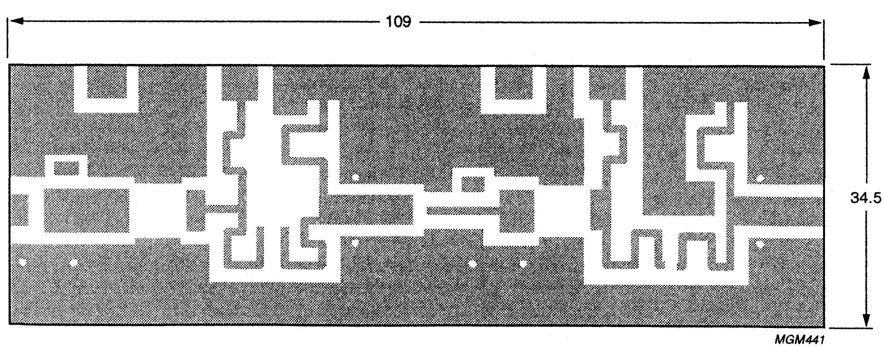


Fig.15 Printed-circuit board BLW32-33.

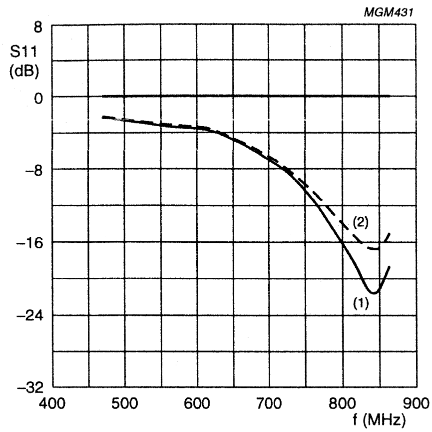


Fig.16 BLW32.

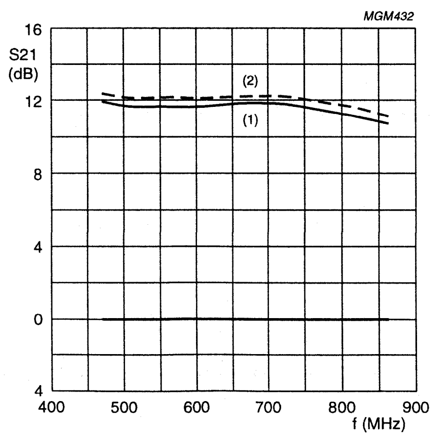


Fig.17 BLW32.

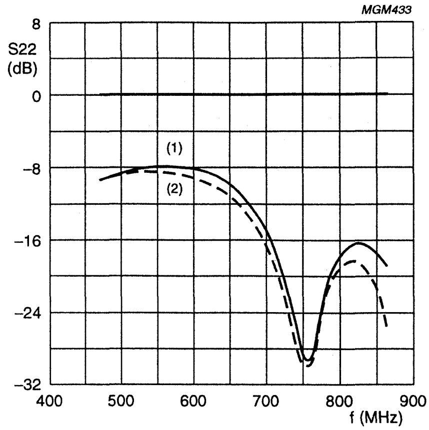


Fig.18 BLW32.

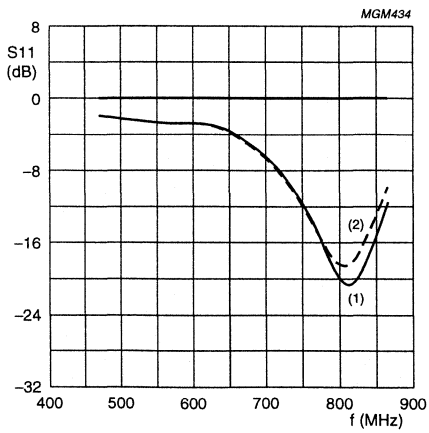


Fig.19 BLW33.

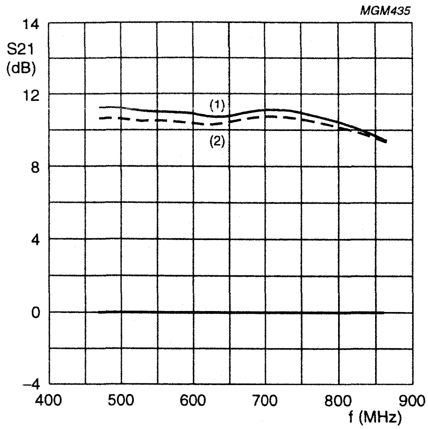


Fig.20 BLW33.

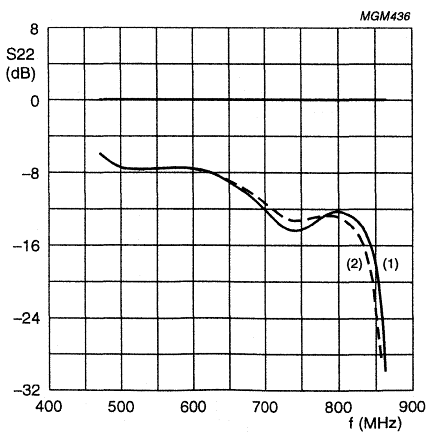


Fig.21 BLW33.

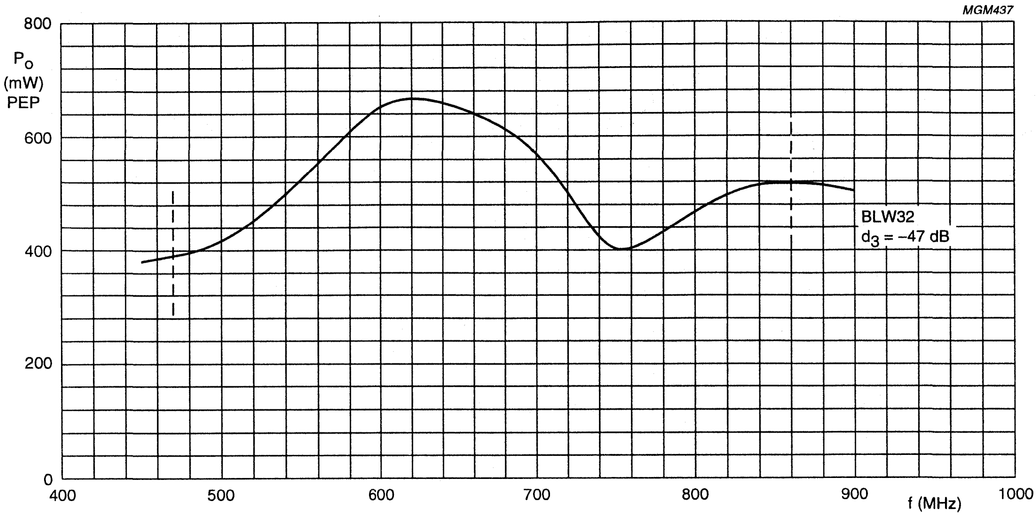


Fig.22 Ampl. no.1.

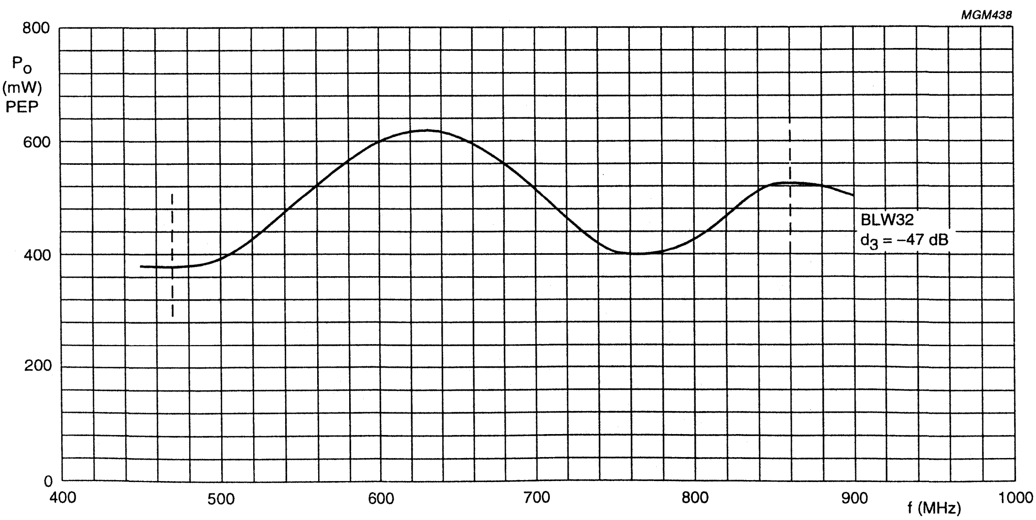


Fig.23 Ampl. no.2.

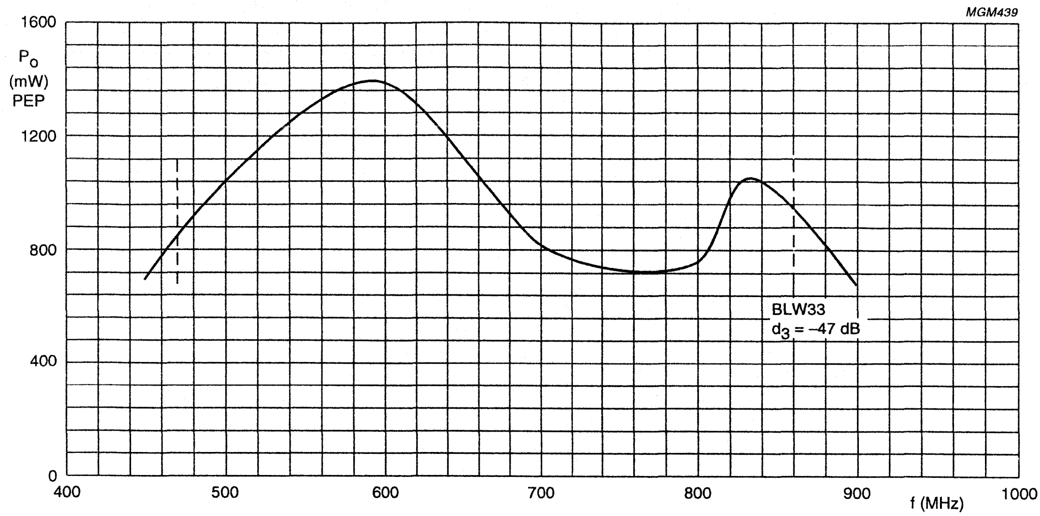


Fig.24 Ampl. no.1.

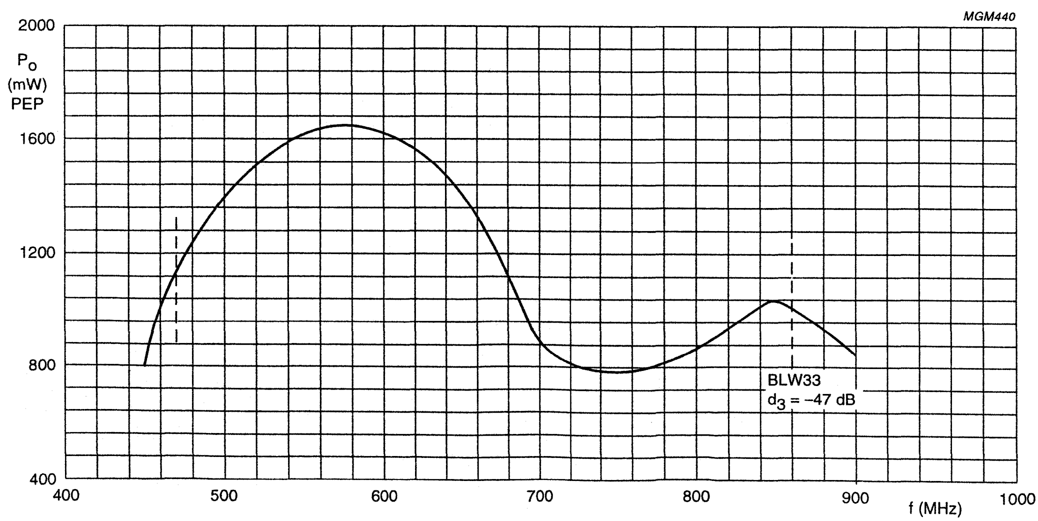


Fig.25 Ampl. no.2.

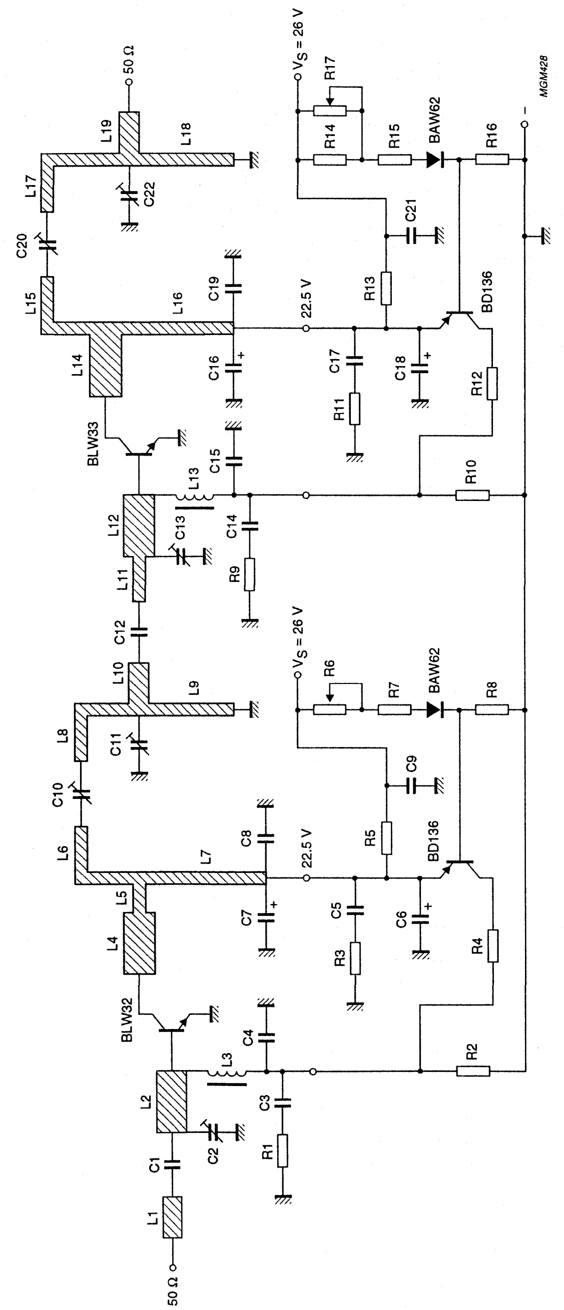


Fig.26 BLW32 and BLW33 circuit.

Table 9 List of components of the BLW32 and BLW33 amplifier (Figs 15 and 26)

$C_1 = C_{12}$	8.2 pF	multilayer ceramic chip capacitor, ATC type 100A-8R2-J-Px-50
$C_2 = C_{11} = C_{13} = C_{22}$	1 to 3.5 pF	film dielectric trimmer (cat.no. 2222 809 05001)
$C_3 = C_9 = C_{14} = C_{21}$	100 nF	polyester capacitor
$C_4 = C_8 = C_{15} = C_{19}$	100 pF	multilayer ceramic chip capacitor (cat.no. 2222 852 13101)
$C_5 = C_{17}$	470 nF	polyester capacitor
$C_6 = C_7 = C_{16} = C_{18}$	6.8 µF	63 V, electrolytic capacitor
$C_{10} = C_{20}$	1 to 4 pF	micro thin-trim, Tekelec Airtronic part no. AT 9401-4-SL1
$L_1 = L_{10} = L_{19}$	stripline (Z_C = 50 Ω)	width 4.0 mm
L_2	stripline (Z_C = 37.6 Ω)	11.5 × 6.0 mm^2
$L_3 = L_{13}$	470 nH	microshoke
$L_4 = L_{14}$	stripline (Z_C = 37.6 Ω)	3.0 × 6.0 mm^2
L_5	stripline (Z_C = 102 Ω)	4.8 × 1.0 mm^2
$L_6 = L_8$	stripline (Z_C = 102 Ω)	20.8 × 1.0 mm^2
L_7	stripline (Z_C = 102 Ω)	19.3 × 1.0 mm^2
L_9	stripline (Z_C = 102 Ω)	23.4 × 1.0 mm^2
L_{11}	stripline (Z_C = 102 Ω)	9.6 × 1.0 mm^2
L_{12}	stripline (Z_C = 37.6 Ω)	5.3 × 6.0 mm^2
$L_{15} = L_{17}$	stripline (Z_C = 102 Ω)	21.7 × 1.0 mm^2
L_{16}	stripline (Z_C = 102 Ω)	16.2 × 1.0 mm^2
L_{18}	stripline (Z_C = 102 Ω)	20.4 × 1.0 mm^2
$R_1 = R_3 = R_9 = R_{11}$	10 Ω (±5%)	carbon resistor CR25 type
$R_2 = R_{10}$	33 Ω (±5%)	carbon resistor CR25 type
$R_4 = R_{12}$	220 Ω (±5%)	power metal film resistor PR37 type
R_5	18 Ω (±5%)	power metal film resistor PR52 type
$R_6 = R_{17}$	220 Ω	cermet preset potentiometer
$R_7 = R_{15}$	150 Ω (±5%)	carbon resistor CR25 style
$R_8 = R_{16}$	1.8 kΩ (±5%)	carbon resistor CR25 style
R_{13}	10 Ω (±5%)	enamelled wire-wound resistor WR 0617E style
R_{14}	1 kΩ (±10%)	carbon resistor CR25 type
$D_1 = D_2$		BAW62

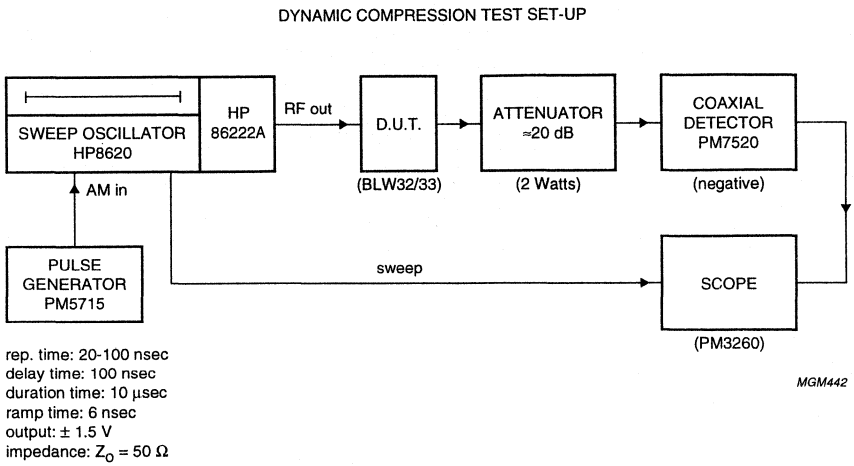


Fig.27 Dynamic compression test set-up.

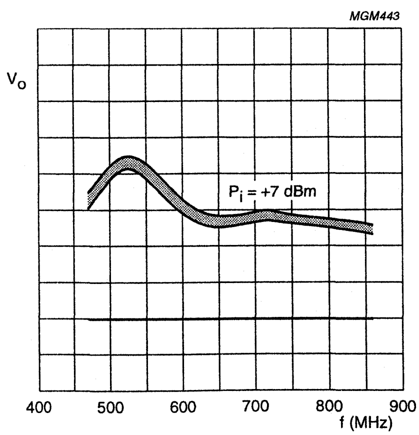


Fig.28 Compression.

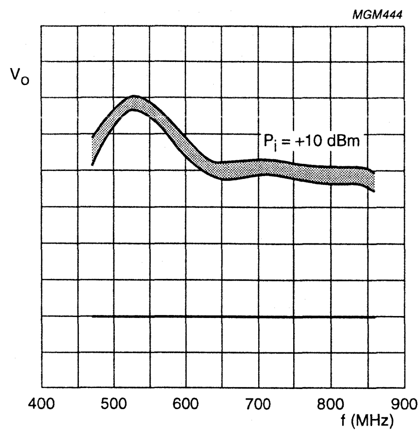


Fig.29 Compression.

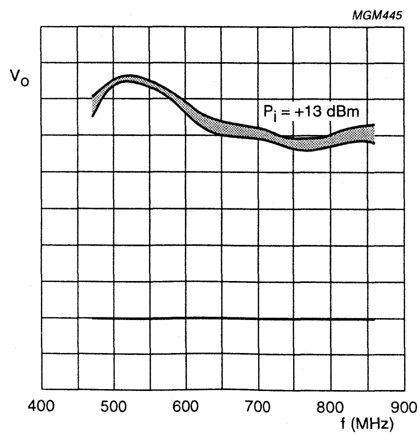


Fig.30 Compression.

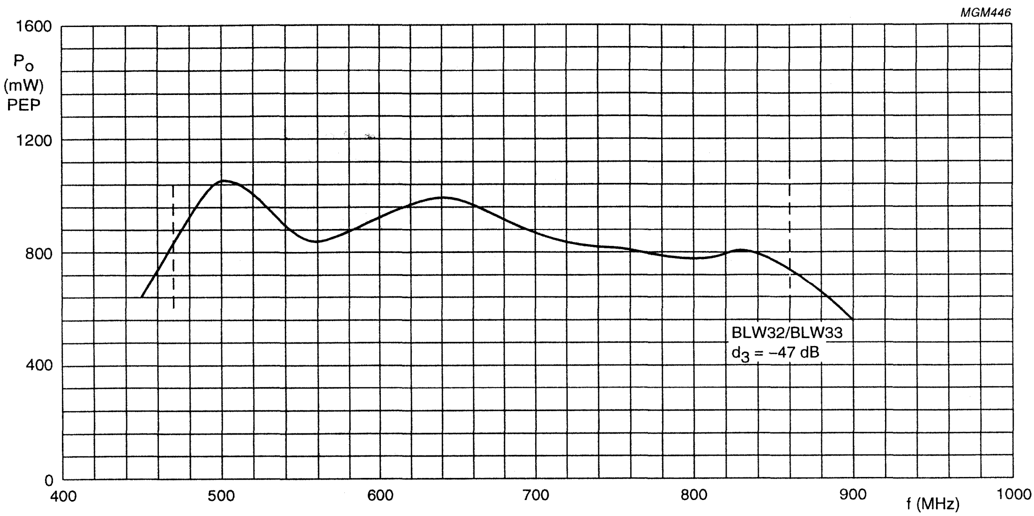


Fig.31 Ampl. no.1.

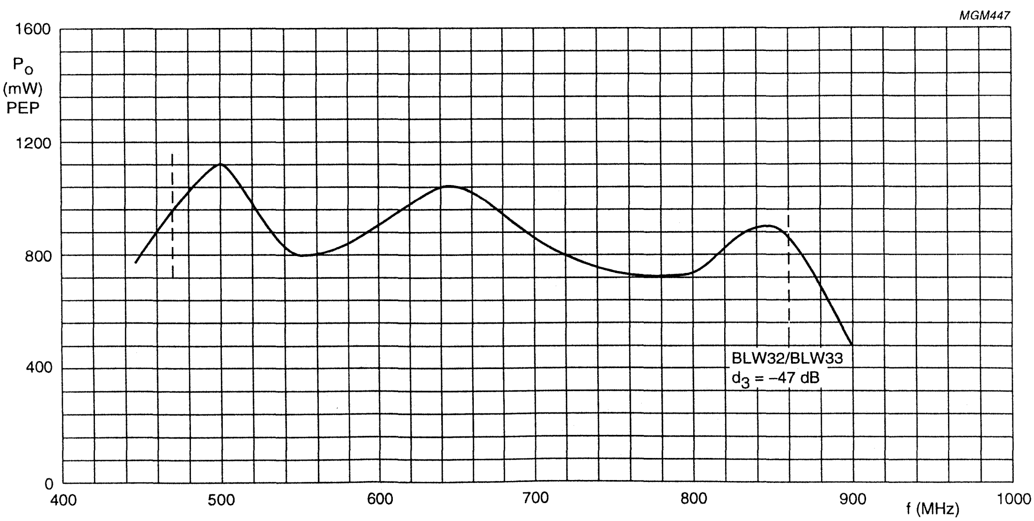


Fig.32 Ampl. no.2.

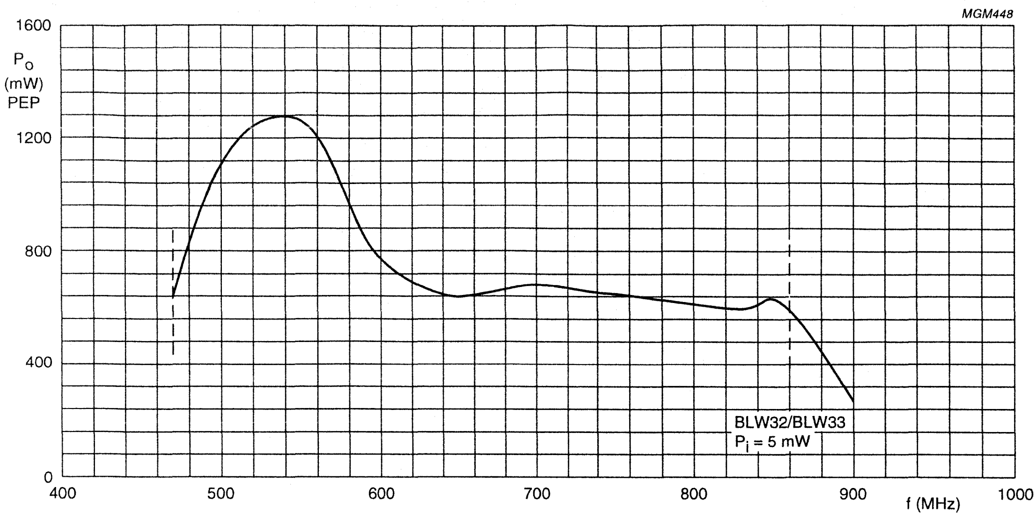


Fig.33 Ampl. no.1.

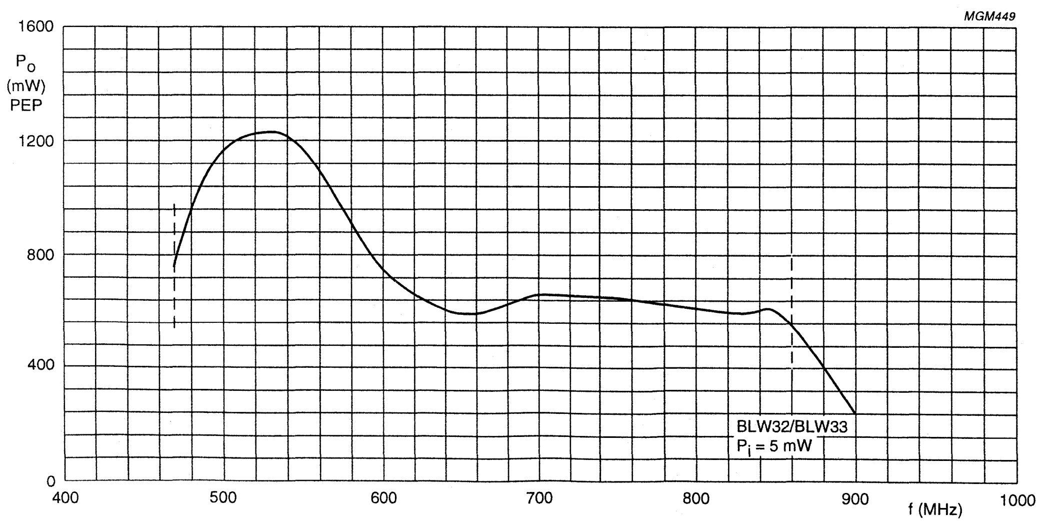


Fig.34 Ampl. no.2.

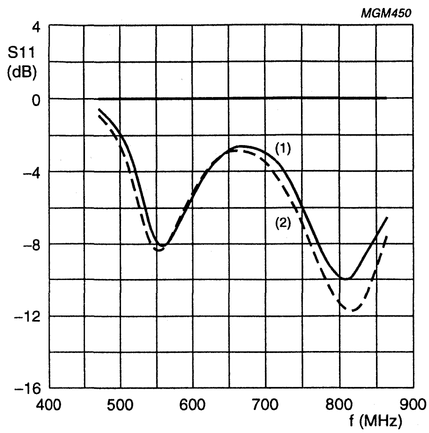


Fig.35 BLW32 and BLW33.

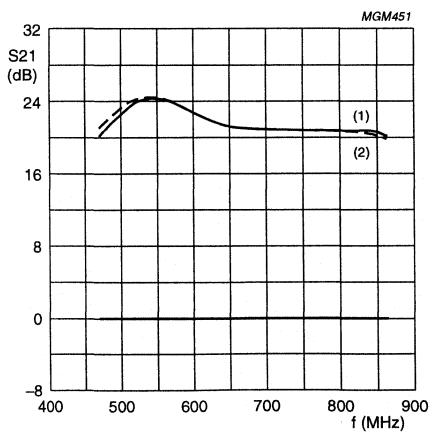


Fig.36 BLW32 and BLW33.

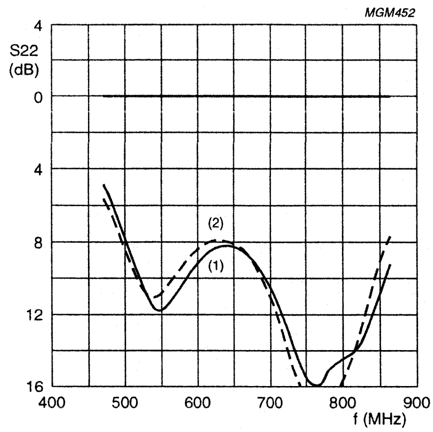


Fig.37 BLW32 and BLW33.

Table 10 BLW32

CHANNEL NO.	I.M.D. (dB)	P_O SYNC. (mW)		GAIN (dB)	
		1[(1)]	2	1	2
21	−60	462	427	12.0	12.3
21	−56	605	561		
21	−52	771	716		
39	−60	699	643	11.7	11.15
39	−56	965	937		
39	−52	1245	1189		
70	−60	487	512	10.8	11.3
70	−56	713	769		
70	−52	1007	1021		

Note

1. Corresponding amplifier number.

Table 11 BLW33

CHANNEL NO.	I.M.D. (dB)	P_O SYNC. (mW)		GAIN (dB)	
		1	2	1	2
21	−60	1132	1440	10.7	10.3
21	−56	1775	1916		
21	−52	2263	2246		
39	−60	1161	1454	10.6	10.25
39	−56	1762	1902		
39	−52	2293	2321		
70	−60	819	1063	9.5	9.3
70	−56	1342	1580		
70	−52	2014	2265		

Table 12 BLW32 and BLW33

CHANNEL NO.	I.M.D. (dB)	P_O SYNC. (mW)	GAIN (dB)
		2	2
21	−60	1045	21.65
21	−56	1706	–
21	−52	2311	–
39	−60	895	21.40
39	−56	1440	–
39	−52	2014	–
70	−60	587	19.75
70	−56	923	–
70	−52	1384	–

A wide-band linear power amplifier (470 – 860 MHz) with two transistors BLW34

Application Note ECO7901

1 ABSTRACT

For application in driver or final stages of TV-transposers in band IV/V (470-860 MHz) a linear wideband power amplifier has been designed with 2 transistors BLW34 coupled by means of 3 dB –90° hybrids. Each transistor is adjusted in class-A at V_{CE} = 25 V and I_c = 0.6 A. The peak sync output power for a 3-tone I.M. distortion of –60dB varies between 3.6 and 5.4 W. The power gain is 9.1 ± 0.3 dB. Input and output VSWR are below 1.3.

2 INTRODUCTION

This report describes the realisation of a wide-band UHF power amplifier for TV transposer service in band IV and V (470 – 860 MHz).

The amplifier is designed with the BLW34 transistor being developed for ultra linear applications operating in class A.

Each device is able to deliver at least 1.8 W peak sync output. The BLW34 forms a series with the smaller devices BLW33 (1.0 W) and BLW32 (0.5 W).

The power gain at 860 MHz is at least 9 dB.

The BLW34 is encapsulated in a 1/4 inch capstan envelope with ceramic cap.

3 THEORETICAL CONSIDERATIONS

3.1 The equivalent circuit of the BLW34

For class A operation the BLW34 is specified at V_{CE} = 25 V; I_c = 600 mA.

The corresponding typical gain, input and load impedance according to the Data sheets are given in Table 1.

Table 1

f (MHz)	GAIN (dB)	R_i (SERIES) (Ω)	X_i (SERIES) (Ω)	R_L (SERIES) (Ω)	X_L (SERIES) (Ω)
470	15.2	1.46	1.93	12.8	11.0
636	12.6	1.39	2.84	8.85	9.97
860	10.1	1.27	4.00	5.36	7.67

To facilitate calculations an approximate equivalent circuit for the transistor input and output impedance can be given. It is shown in Fig.1.

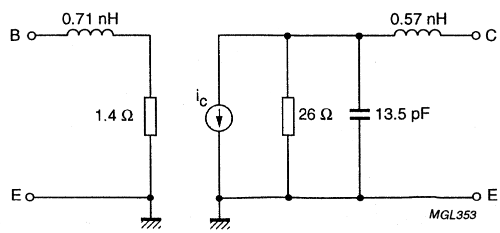


Fig.1

3.1.1 THE OUTPUT NETWORK

The circuit will be designed on printed circuit board with PTFE fibre glass as a dielectric having an $\varepsilon_r = 2.74$ and thickness of 1/32 inch.

The input and output network start with a piece of stripline having a width of 6 mm, being the width of the base and collector leads. For a dielectric of 1/32 inch the characteristic resistance is 21 Ω. The length for the collector lead amounts to 3 mm, but the base lead is different in length.

The first step in the matching is to tune out the output capacitance of the transistor by means of the collector R.F. choke.

This choke is executed as a stripline with a width of 1 mm corresponding with a characteristic resistance of 72 Ω to keep the parallel capacitance at this point as low as possible.

For practical reasons the choke is connected to the main transmission line at a distance of 3 mm from the transistor edge. For the design procedure one is referred to Part 1 of this handbook (SC19B).

The results of the calculations before and after computer optimization are given in Fig.2 and Table 2.

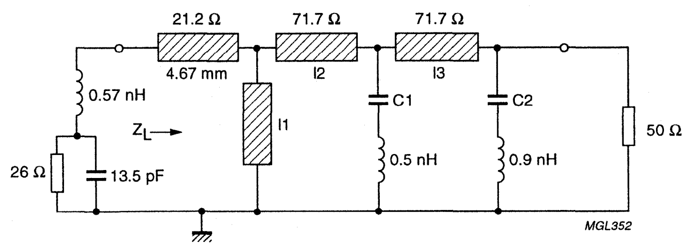


Fig.2

Table 2

ELEMENT	BEFORE OPTIM.	AFTER OPTIM.	UNIT
l_1	16.8	22.1	mm
l_2	18.2	20.8	mm
C_1	8.58	9.76	pF
l_3	38.2	43.5	mm
C_2	3.91	3.09	pF
$S_{max.}$	2.48	1.23	–

S_{max} is the maximum VSWR of the network.

The lenghts given hold for air lines. The actual lengths on the printed-circuit board are shorter; the reduction factors are: 1.445 for the 72 Ω lines and 1.556 for the 21 Ω line.

The predicted minimum output power of the complete amplifier with two transistors BLW34 is:

$$Po_2 = \frac{2Po_1}{S_{max}} \cdot 0.95 = \frac{2 \cdot 1.8}{1.23} \cdot 0.95 \cong 2.8W$$

Po_1 is the minimum output power of one transistor in a narrow band circuit, S_{max} is as specified above and the factor 0.95 represents the power loss of the hybrid coupler at the output.

3.1.2 THE INPUT NETWORK

The design procedure can be found in Part 1 of this handbook (SC19B).

The results of the calculations are summarized in Fig.3 and Table 3.

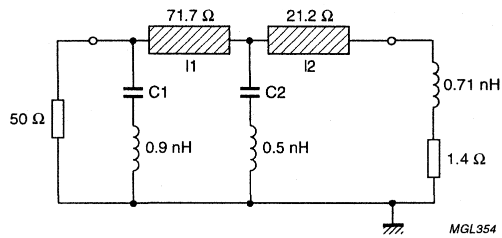


Fig.3

Table 3

ELEMENT	BEFORE OPTIM.	AFTER OPTIM.	UNIT
C1	4.78	4.41	pF
l1	25.9	32.1	mm
C2	21.9	19.9	pF
l2	13.3	10.5	mm
ΔG	±1.93	±0.12	dB

ΔG is the resulting power gain variation caused by the transistor and the input network over the frequency band. The lengths of the lines hold for air as a dielectric. Transformation to striplines on a printed-circuit board is done in the same way as in the previous section.

The minimum power gain of the complete amplifier with two transistors BLW34 is expected to be:

$$G_o = G_t - 2A_H - A_1 - A_2$$

in which: G_t = minimum power gain of BLW34 in a narrow band circuit.

A_H = power loss of one hybrid coupler

A_1 = reflection loss of input network

A_2 = reflection loss of output network.

In practical figures this means:

$G_o = 9.0 - 2 \times 0.2 - 0.15 - 0.05 = 8.4$ dB.

The input VSWR of a single amplifier was calculated to vary from 11 at 470 MHz down to 1.45 at 860 MHz.

4 THE HYBRID COUPLED AMPLIFIER

4.1 Practical considerations

On previous pages the theoretical approach of a single amplifier has been discussed.

In practice, it was the intention to realize a small compact amplifier on a printed-circuit board with the input and output terminal (Rc = 50 Ω) in line for easy cascading of several amplifiers.

Besides the wide-band properties it is the intention to obtain a higher output power, so two BLW34 branches are connected in parallel.

At the same time it is of course rather unacceptable that the amplifier loads a driver stage with a mismatch causing a VSWR of 11 at 470 MHz.

Both problems may be solved sufficiently by applying two BLW34 branches in parallel with the aid of two wide-band 3 dB –90 °C. coaxial hybrids on a 50 Ω basis.

In this configuration the output power will be nearly doubled; reduction of the input VSWR of the complete system to a value of around 1.2 may be explained from the properties of the coupler applied. The reflected power will be absorbed in the resistor matching the isolated port. This resistor is 50 Ω and consists of two 100 Ω power metal film resistor in parallel. The same has been done on the output side.

The printed-circuit board needs to be double copper clad with a PTFE fibre glass dielectric ($\varepsilon_r = 2.74$) for low losses at UHF.
A thickness of 1/32 inch has been chosen; so the 72 Ω lines are 1 mm wide.

Figure 4 shows the circuit diagram of the complete 2× BLW34 class A amplifier. The biasing circuit is drawn in Fig.5.

The printed-circuit board and the amplifier lay-out in Fig.6.

For a correct earthing the upper earth sheet parts are connected to the lower sheet by soldering copper straps at the edges of the printed-circuit board. The black parts in Fig.6 are the soldered copper straps.

The emitters are grounded as short as possible by applying copper straps under the emitter leads. For that reason the holes in the board are square instead of round.

Both transistors are screwed to a water-cooled brass heatsink. So, several heatsink temperatures can be applied by means of a TAMSON unit supplying water with a thermostatically controlled temperature.

The tuning capacitors in the circuit are of the film dielectric type with three tags of which both earth terminals are fed through small holes and soldered to the upper as well as the lower plane. Fixed capacitors in the r.f. path are of the multi-layer ceramic chip type.

The coaxial connectors are of the SMA 50 Ω type, being soldered to upper and lower sheet.

4.2 Practical optimization

We started with optimization on a small signal basis with the circuit inserted in a network analyzer chain, having swept S-parameter facilities.

So far, similar tuning methods have been applied as described in Ref. 2.

Because it is rather complicated to find the best compromise between an acceptable flat gain curve (S_{21}) and sufficient output power with low i.m.d. a dynamic large signal optimization method has been realized. Figure 7 shows the block diagram.

This tuning method is based on the correlation between the single tone 1dB compression point and the i.m.d figure of a linear amplifier.

In this set-up the swept output power level of the amplifier under test is kept constant and the required (detected) drive power monitored on an oscilloscope screen (PM3260).

The swept drive power is available from the sweep generator HP8620C in combination with RF plug-in unit HP86222A. Because the output power of this system is too low viz. appr. 20 mW (+13 dBm) a combined amplifier with BLW32 and BLW33 (Ref. 2) has been added. The latter combination shows an overall gain of approx. 20 db in the range 470 – 860 MHz. When the circuit under test is inserted in the chain of Fig.7, the input power measured on port C of hybrid 1 corresponds in principle with the gain curve (S_{21}) being measured with the network analyzer; in fact one is the inverse of the other.

When the drive level is slowly increased, the shape of the gain curve changes somewhat when compression starts. By careful retuning of the amplifier the shape of the gain curve can be corrected again in the direction of the original smaller signal curve.

The actual single tone output power has been measured with the aid of the calorimetric watt meter HP435A when the action of the sweep is stopped. Also it is possible to examine the output signal itself by means of a spectrum analyzer being loosely coupled via a 50 Ω pick-off device.

Resuming it can be said that the advantage of applying this high level tuning system is characterized by the fact that the output power is leveled and so compression does not start earlier due to gain fluctuations of the amplifier. This makes the judgement of the compression level easier.

4.3 Intermodulation, VSWR and gain measurements

For i.m.d. measurements on television systems the post offices advice and apply the 3-tone test method (vision carrier –8 dB, sound carrier –7 dB, sideband signal –16 dB; zero dB corresponds to peak sync level).

For this reason a wideband test set-up has been realized. The block diagram is in Fig.8. In this set-up first the sound and vision carriers are joined in the wide-band coaxial hybrid H_1.Then the sideband signal from the (smaller) generator SMLU is added in hybrid H_2.

The complete 3-tone signal passes a low-pass filter (700 or 1 000 MHz cut-off depending on input frequency) a continuously variable attenuator and a circulator (three different types needed to cover at least the range 470 – 860 MHz).

The output power is measured with a HP435A calorimetric watt meter and the i.m.d. observed with a spectrum analyzer (HP8558B).

Figure 9 shows the 3-tone i.m.d. results measured on the complete hybrid coupled 2 × BLW34 amplifier. To get an idea of the $P_{o\ sync}$ drop for different heatsink temperatures, measurements have been done for T_{HS} = 23 °C and T_{HS} = 70 °C. The maximum drop in $P_{o\ sync}$ amounts to 1.1 dB.

Besides the 3-tone test the peak envelope power has been measured in a two-tone way for a third order i.m.d of d_3 = –47 dB.

It can be proved that there is a correlation between the afore described –60 dB 3-tone and the –47 dB two-tone test method.

It is known that the advantage of video precorrection on i.m.d. amounts to values up to 10 dB. Calculating with an average of 8 dB, the two-tone i.m.d. for d_3 = 39 dB is interesting. From Fig.10 it may be seen that the output power is more than doubled. Both tests have been done for heatsink temperatures of resp. 23 and 70 °C.

Finally input and output VSWR and gain figures were measured only under small signal conditions. The results of amplifier branches 1 and 2 for a heatsink temperature of 70 °C are shown in Figs 11 to 13. The VSWR figures of the input and output are expressed in reflection damping (resp. S_{11} and S_{22}) on a 50 Ω basis.

According to Fig.11 the minimum reflection damping of the input amounts to $S_{11} = -1$ dB (VSWR = 17.4) at 470 MHz and to $S_{11} = -10$ dB (VSWR = 1.93) at 860 MHZ.

On the output side the worst reflection damping amounts to $S_{22} = -5.5$ dB (VSWR = 3.26) in the middle of the passband (Fig.13).

The power gain, represented by S_{21}, is appr. 9.5 dB (Fig.12).

Resuming it can be said that, as Figs 11 to 13 show, the differences in gain, input and output VSWR between both branches are rather small.

Figs 14 to 16 show the final results of the complete hybrid coupled amplifier. Examining the S_{11} and S_{22} figures it appears that the minimum input reflection damping (S_{11}) amounts to appr. 18 dB, what corresponds with a maximum VSWR of 1.29.

The latter value may be mainly explained from the specified maximum VSWR = 1.25 of the applied Anaren hybrids. If more attention is paid to matching of the isolated ports the results may be improved. The matching consists of two metal film power transistors of 100 Ω in parallel. They have low-frequency tolerances of 5%.

The small signal gain of the complete amplifier amounts to 9.1 ±0.3 dB for $T_{HS} = 23$ °C, whilst the dashed line shows the results for $T_{HS} = 70$ °C being 8.9 ± 0.3 dB.

The temperature influence on the S_{11} and S_{22} figures is almost negligible.

5 CONCLUSIONS

On preceding pages the theoretical and practical design has been described of the wide-band (470 – 860 MHz) high quality linear amplifier being equipped with two BLW34 transistors operating in class A.

There are some small differences between the theoretical design and the practical circuit.

- The calculated value for the chip capacitors $C_{11} = C_{12} = C_{13} = C_{14}$ in Fig.4 was 10 pF. In practice 8.2 pF appeared to be a better choice.
- Also the values of $C_{19} = C_{20} = C_{21} = C_{22}$, being calculated as 4.7 pF are changed. The new value is 3.9 pF.
- In the first instance a chip capacitor of 1.5 pF in parallel with C_{23} and C_{26} was planned. However this capacitor could be omitted in the operational circuit.

The excepted results for a single amplifier: $G_{p\ min.} = 8.8$ dB; and $P_{o\ sync} = 1.5$ W at a 3-tone i.m.d. of –60 dB and $G_{p\ min} = 8.4$ dB and $P_{o\ sync} = 2.8$ W for $T_{HS} \leq 70$ °C are realized in this design.

Here, we have calculated with a total insertion loss of 0.4 dB for the applied hybrids. They are specified for a maximum of 0.25 dB per device (1.06 × power).

6 REFERENCES

Ref. 1: O. Pitzalis Jr. and R.A. Gilson - Tables of impedance matching networks which approximate prescribed attenuation versus frequency slopes. IEEE Transactions on microwave theory and techniques, Vol. MTT-19, no. 4, April 1971, pp. 381-386.

Ref. 2: A.H. Hilbers and M.J. Köppen - Wide-band linear power amplifier (470 – 860 MHz) with the transistors BLW32 and BLW33. C.A.B. report ECO7806.

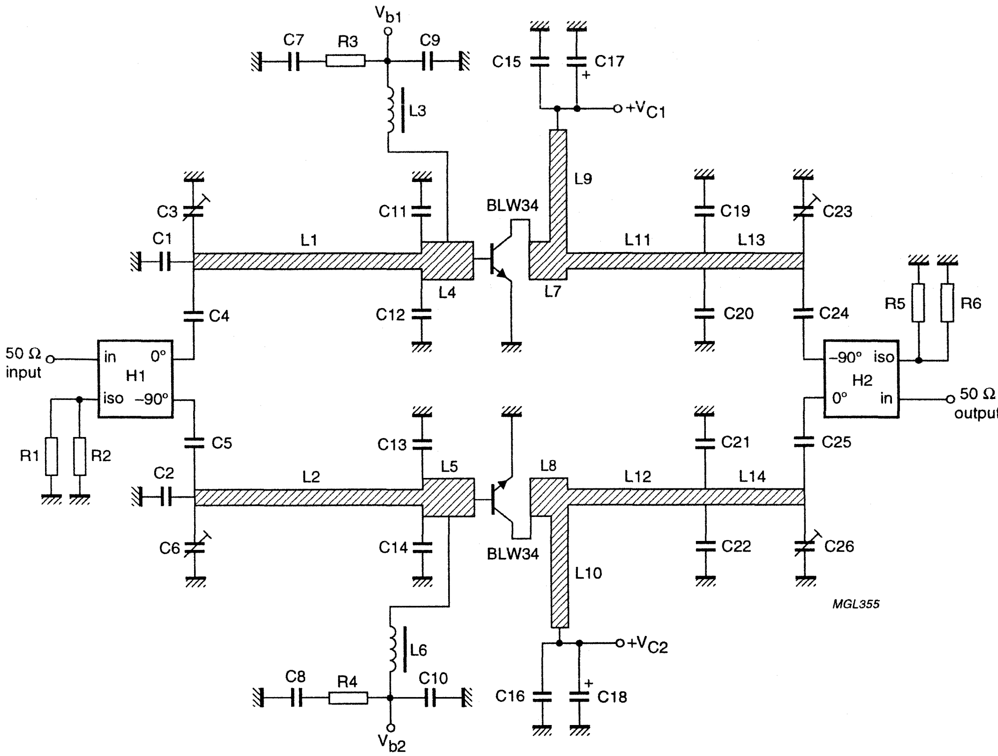

Vb1
C7
R3
C9
C15
C17
+VC1
L3
L9
BLW34
C3
C11
C19
C23
C1
L1
L11
L13
L4
L7
C4
C12
C20
C24
R5
R6
50 Ω
input
in
0°
H1
iso
–90°
–90°
iso
H2
0°
in
50 Ω
output
R1
R2
C5
C13
C21
C25
C2
L5
L8
L2
L12
L14
C6
C14
BLW34
C22
C26
L10
MGL355
+VC2
L6
C8
R4
C10
C16
C18
Vb2

Fig.4

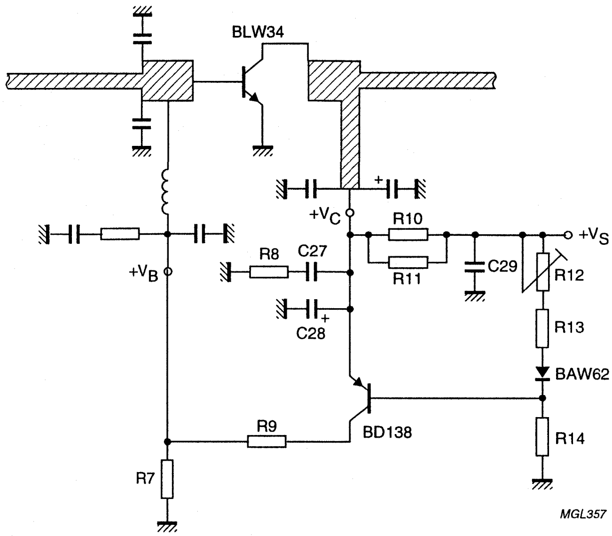

BLW34
+VC
R10
+VS
R8
C27
R11
C29
R12
+VB
C28
R13
BAW62
R9
BD138
R14
R7
MGL357

Fig.5

Table 4

LIST OF COMPONENTS	
$C_1 = C_2 = 2.2$ pF	multilayer ceramic chip capacitor Tekelec-Airtronic part no. 500 R15 N2R2 BA
$C_3 = C_6 = C_{23} = C_{26} = 1.4$ to 5.5 pF	film dielectric trimmer (cat. no. 2222 809 09001)
$C_4 = C_5 = C_{24} = C_{25} = 100$ pF	multilayer ceramic chip capacitor (cat. no. 2222 851 13101)
$C_7 = C_8 = C_{29} = 100$ nF	polyester capacitor
$C_9 = C_{10} = C_{15} = C_{16} = 100$ pF	multilayer ceramic chip capacitor (cat. no. 2222 852 13101)
$C_{11} = C_{12} = C_{13} = C_{14} = 8.2$ pF	multilayer ceramic chip capacitor, ATC (American Technical Ceramics) type 100A-8R2-J-Px-50
$C_{17} = C_{18} = C_{28} = 6.8$ µF, 63 V	electrolytic capacitor
$C_{19} = C_{20} = C_{21} = C_{22} = 3.9$ pF	multilayer ceramic chip capacitor, Tekelec-Airtronic part no. 500 R15 N3R9 CA
$C_{27} = 470$ nF	polyester capacitor
$R_1 = R_2 = R_5 = R_6 = 100\ \Omega$ (±5%)	power metal film resistor PR37 type (cat. no. 2322 191 31001)
$R_3 = R_4 = R_8 = 10\ \Omega$ (±5%)	carbon resistor; CR25 type
$R_7 = 33\ \Omega$ (±5%)	carbon resistor; CR25 type
$R_9 = 220\ \Omega$ (±5%)	power metal film resistor PR52 type (cat. no. 2322 192 32201)
$R_{10} = 5.6\ \Omega$ (±5%)	enamelled wire-wound resistor WR0617E style
$R_{11} = 8.2\ \Omega$ (±5%)	enamelled wire-wound resistor WR0617E style
$R_{12} = 100\ \Omega$	cermet preset potentiometer
$R_{13} = 120\ \Omega$ (±5%)	carbon resistor; CR25 type
$R_{14} = 1.8$ kΩ (±5%)	carbon resistor; CR25 type
$H_1 = H_2$ = ultra-miniature 3 dB –90° coupler model no. 10264-3, range 0.5 – 1,0 GHz; Anaren Microwave Inc.	
$L_1 = L_2$	stripline (Zc = 72 Ω), 22.1 × 1.0 mm^2; note 1
$L_3 = L_6 = 1$ µH	microchoke
$L_4 = L_5$	stripline (Zc = 21 Ω), 6.7 × 6.0 mm^2; note 1
$L_7 = L_8$ = stripline	(Zc = 21 Ω), 3.0 × 6.0 mm^2; note 1
$L_9 = L_{10}$ = stripline	(Zc = 72 Ω), 15.2 × 1.0 mm^2; note 1
$L_{11} = L_{12}$ = stripline	(Zc = 72 Ω), 14.3 × 1.0 mm^2; note 1
$L_{13} = L_{14}$ = stripline	(Zc = 72 Ω), 29.9 × 1.0 mm^2; note 1

Note

1. These striplines are printed on double Cu-clad printed-circuit board with PTFE fibre-glass dielectric ($\varepsilon_r = 2.74$); thickness 1/32".

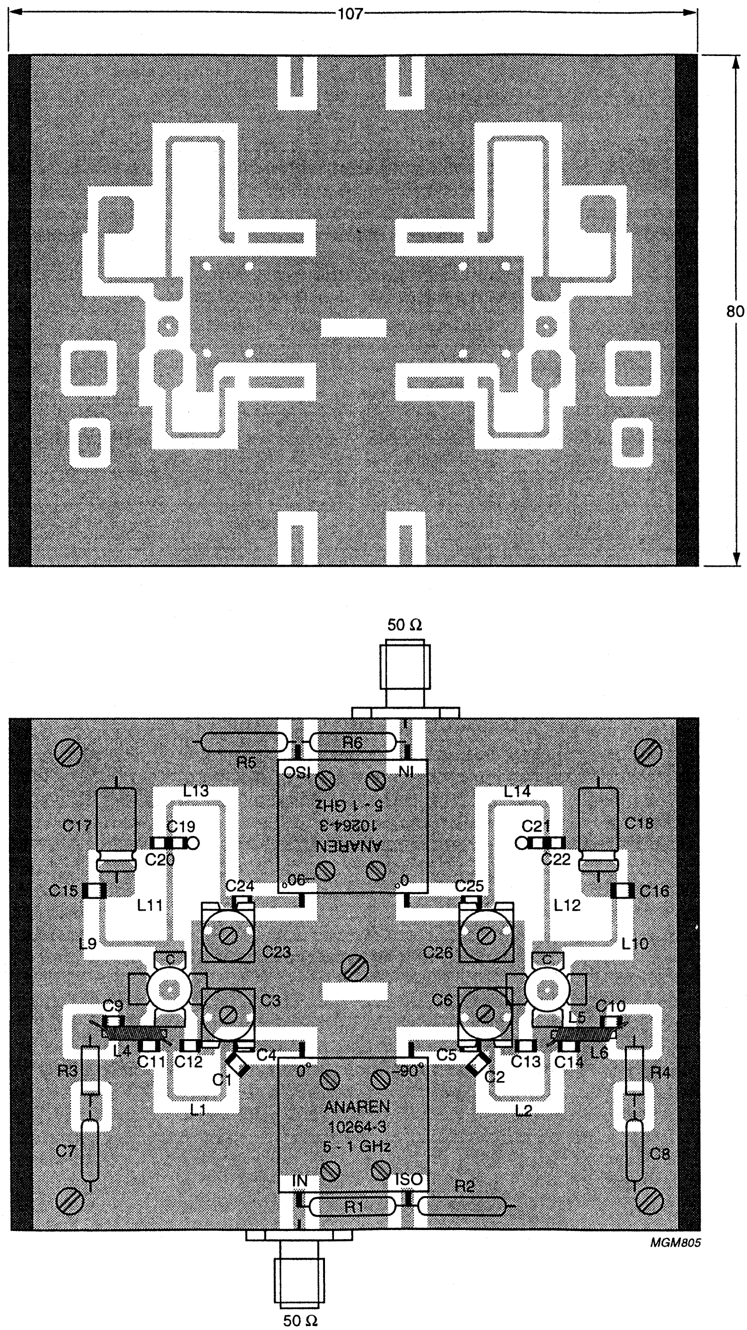


Fig.6 Printed-circuit board and amplifier lay-out.

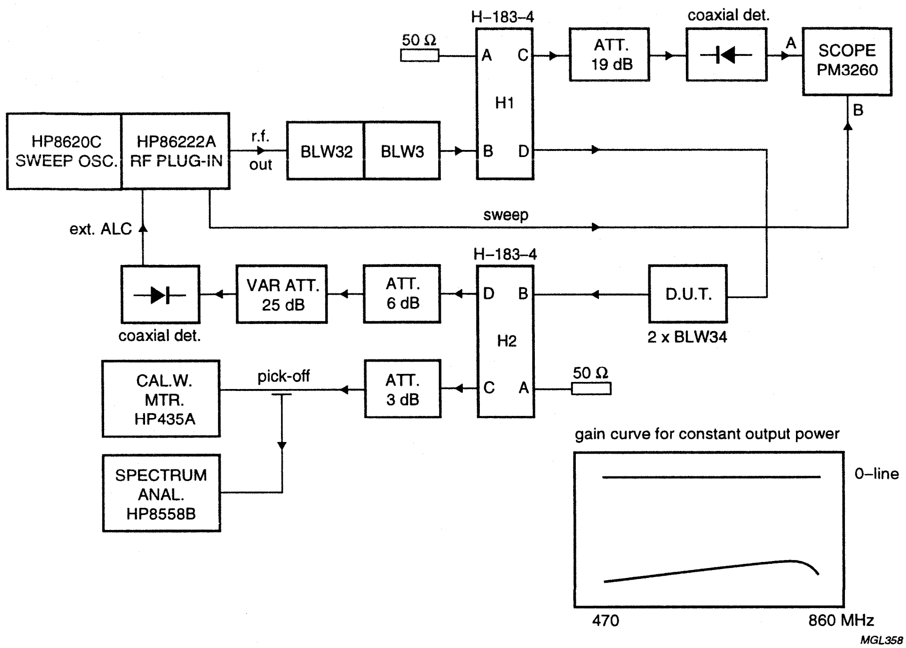
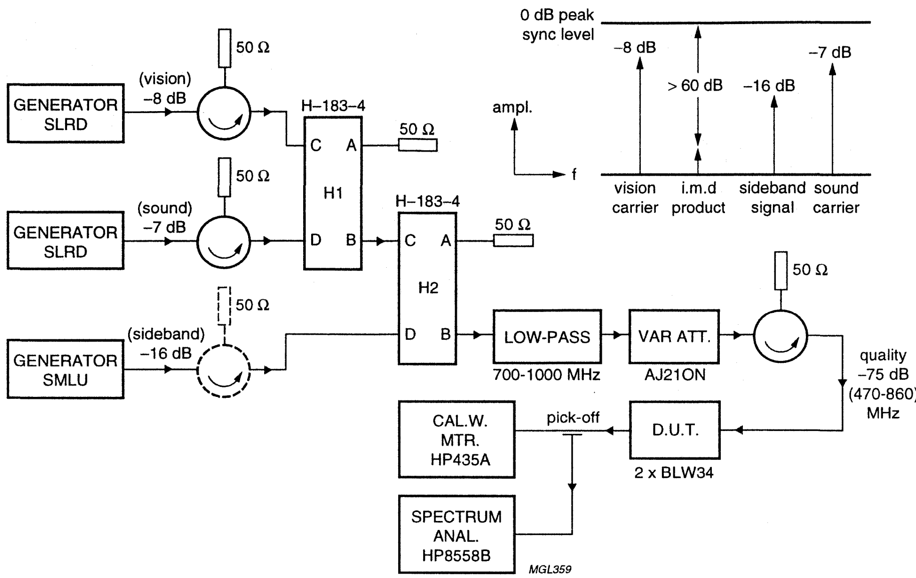


Fig.7 Dynamic compression test set-up.



Circulator ranges:
(1) 470 – 600 MHz.
(2) 600 – 800 MHz.
(3) 790 – 1000 MHz.

Fig.8 3-tone test set-up 470 – 860 MHz.

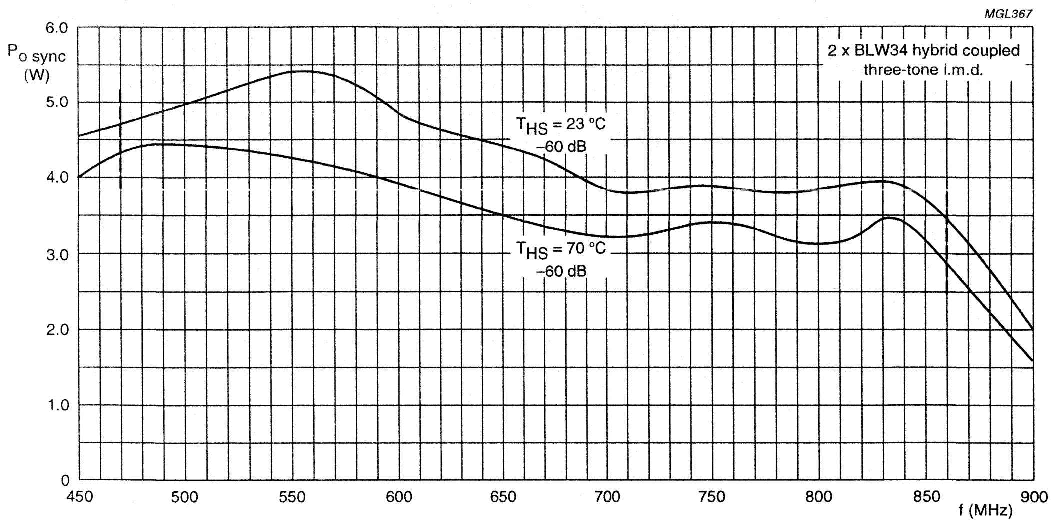

MGL367
6.0
P_o sync (W)
5.0
4.0
3.0
2.0
1.0
0
450
500
550
600
650
700
750
800
850
900
f (MHz)
2 x BLW34 hybrid coupled three-tone i.m.d.
T_{HS} = 23 °C −60 dB
T_{HS} = 70 °C −60 dB

Fig.9

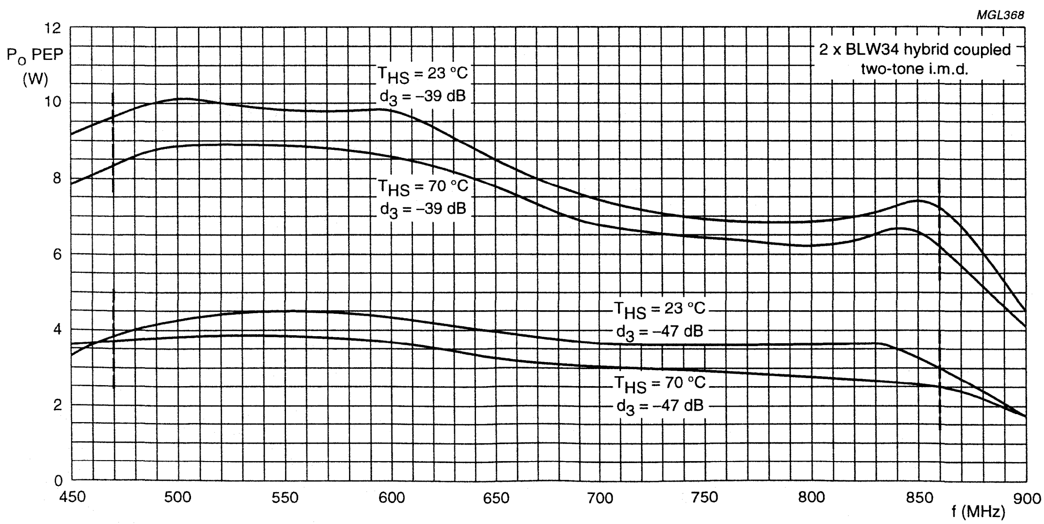

MGL368
12
P_o PEP (W)
10
8
6
4
2
0
450
500
550
600
650
700
750
800
850
900
f (MHz)
2 x BLW34 hybrid coupled two-tone i.m.d.
T_{HS} = 23 °C d_3 = −39 dB
T_{HS} = 70 °C d_3 = −39 dB
T_{HS} = 23 °C d_3 = −47 dB
T_{HS} = 70 °C d_3 = −47 dB

Fig.10

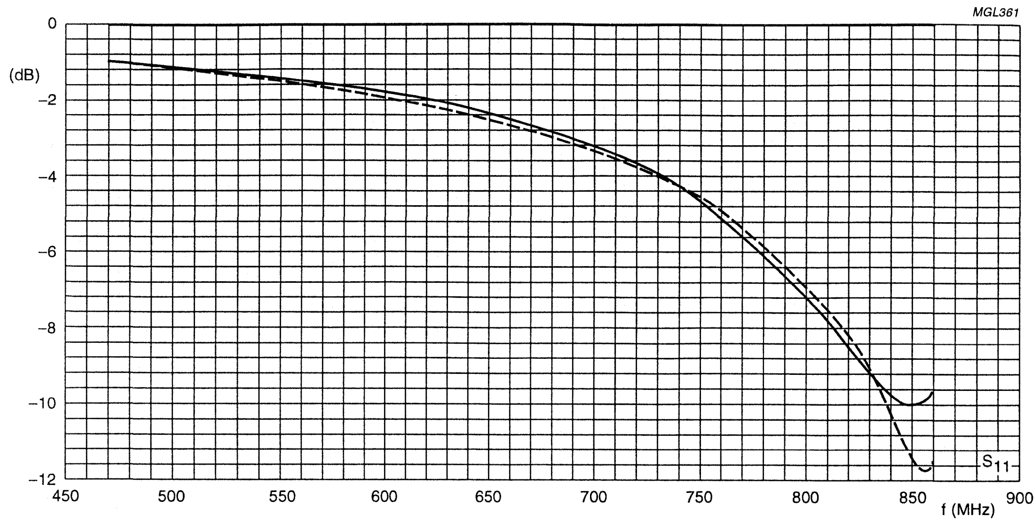

MGL361
0
(dB)
−2
−4
−6
−8
−10
−12
450
500
550
600
650
700
750
800
850
900
f (MHz)
S_{11}

Fig.11

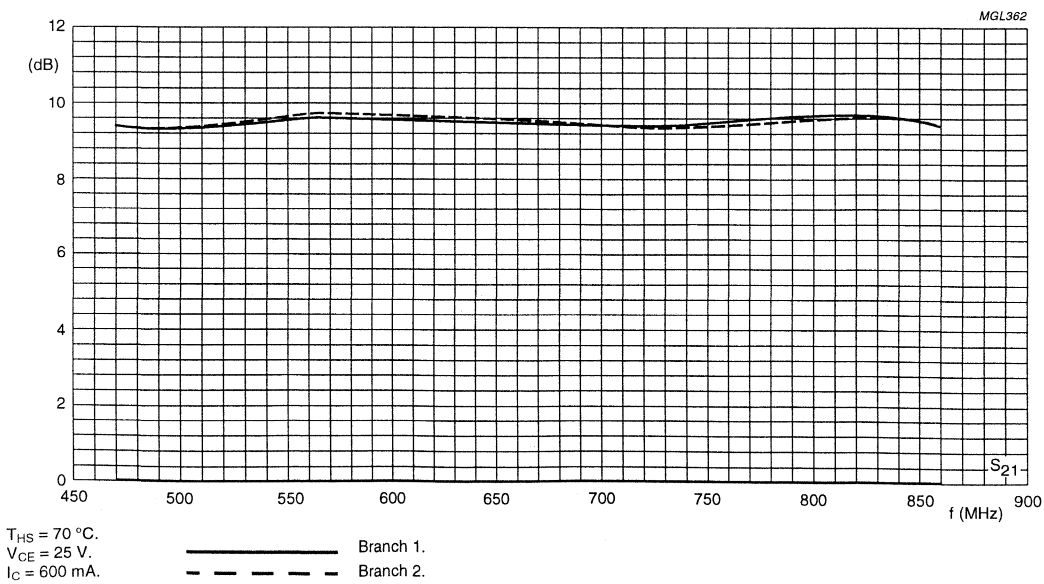

MGL362
12
(dB)
10
8
6
4
2
0
450
500
550
600
650
700
750
800
850
900
f (MHz)
S_{21}
T_{HS} = 70 °C.
V_{CE} = 25 V.
I_C = 600 mA.
Branch 1.
Branch 2.

Fig.12

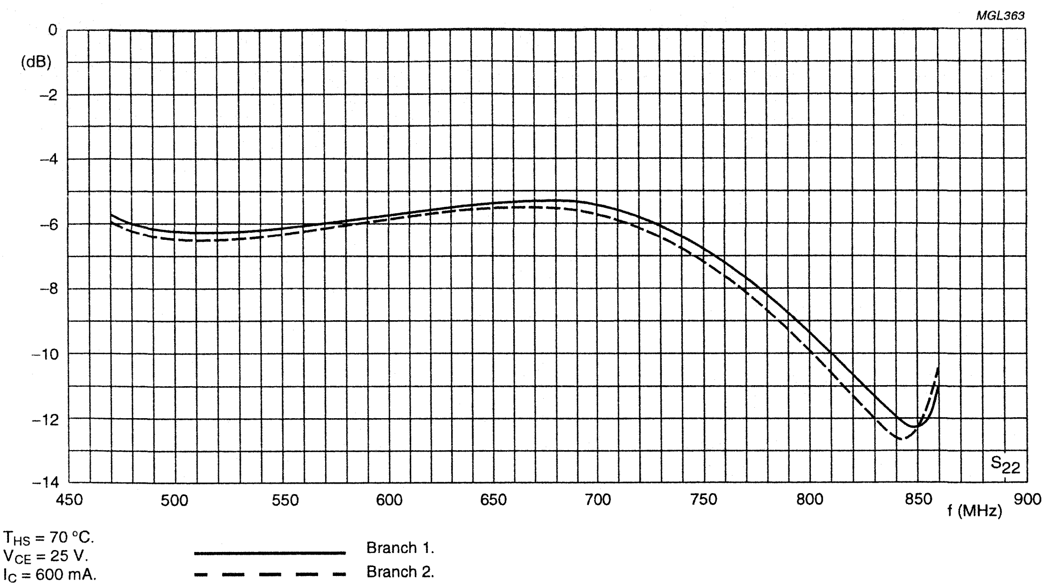

MGL363
0
(dB)
−2
−4
−6
−8
−10
−12
−14
450
500
550
600
650
700
750
800
850
900
f (MHz)
S22
T_{HS} = 70 °C.
V_{CE} = 25 V.
I_C = 600 mA.
Branch 1.
Branch 2.

Fig.13

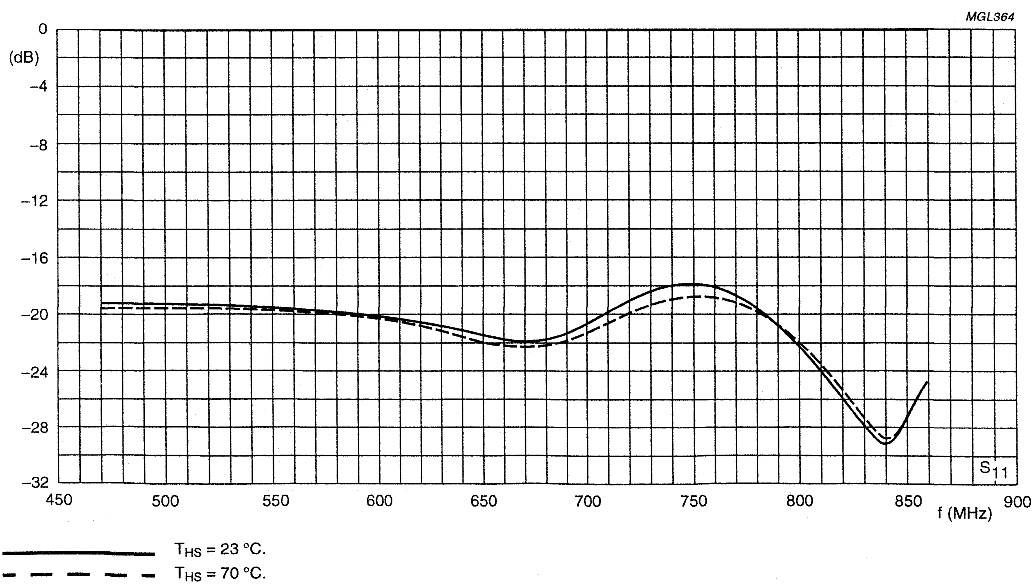

MGL364
0
(dB)
−4
−8
−12
−16
−20
−24
−28
−32
450
500
550
600
650
700
750
800
850
900
f (MHz)
S11
T_{HS} = 23 °C.
T_{HS} = 70 °C.

Fig.14

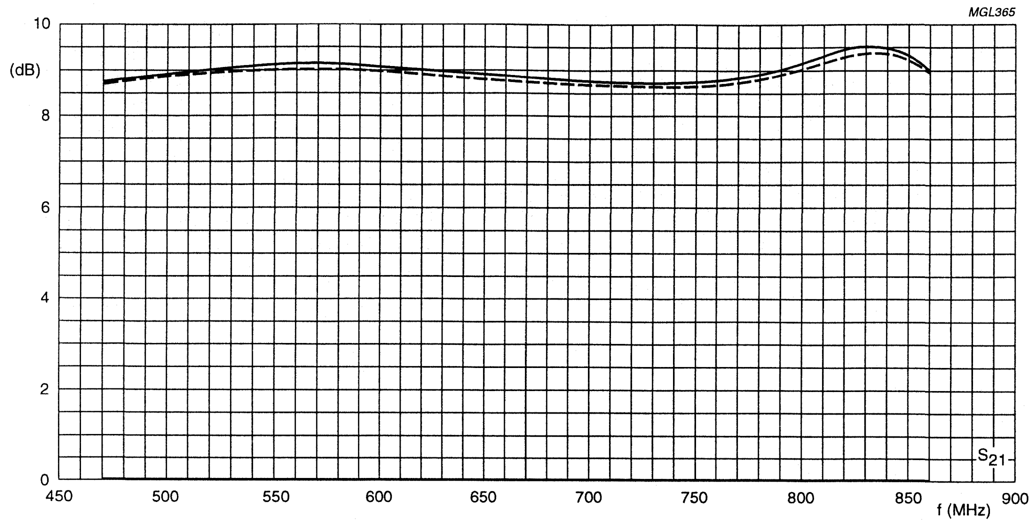

MGL365
10
(dB)
8
6
4
2
0
450
500
550
600
650
700
750
800
850
900
f (MHz)
S_{21}

Fig.15

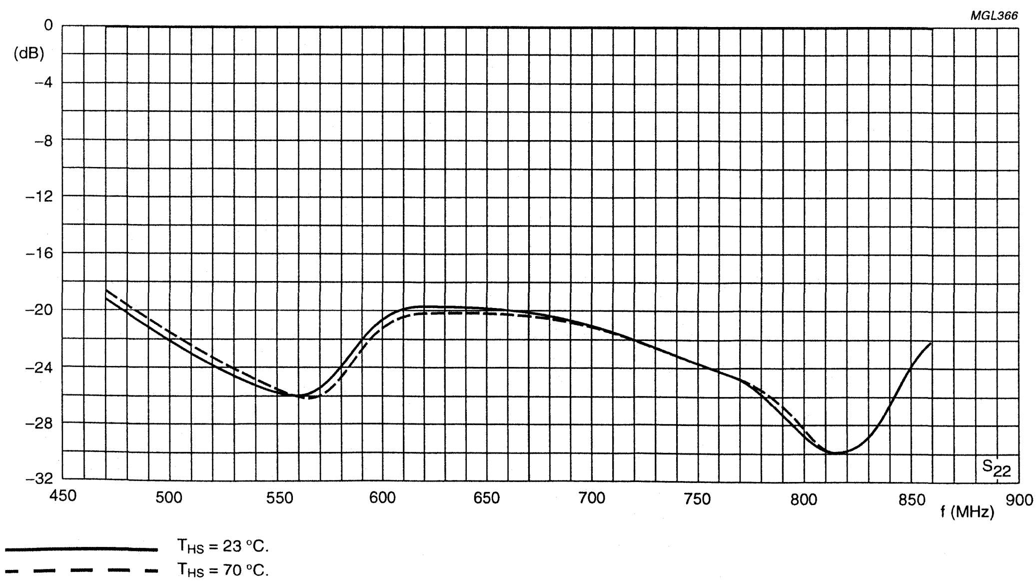

MGL366
0
(dB)
−4
−8
−12
−16
−20
−24
−28
−32
450
500
550
600
650
700
750
800
850
900
f (MHz)
S_{22}
T_{HS} = 23 °C.
T_{HS} = 70 °C.

Fig.16

Wide-band linear power amplifier (470 – 860 MHz) with two transistors BLW98

Application Note ECO7905

1 ABSTRACT

In this report a wideband linear power amplifier with 2 transistors BLW98 is described. This amplifier is intended for application in TV transposers and transmitters in band IV and V: 470 – 860 MHz. The transistors are operated in class-A at: V_{CE} = 25 V, I_C = 850 mA. The power gain varies from 7.0 to 8.1 dB. For a 3-tone I.M. distortion of –60 dB the peak sync. output power is between 6.3 and 9.2 W. At a cross-modulation of 7% the output power ranges from 6.1 to 7.8 W.

2 INTRODUCTION

The amplifier described in this report is intended for application in TV transposers and transmitters for band IV and V: 470 – 860 MHz. It is a wideband class A linear power amplifier with 2 transistors type BLW98.

The main purpose was to achieve the highest possible peak sync output power at a 3-tone I.M. distortion of –60 dB. At the same time the power gain should be at high as possible with a minimum of variation in the frequency band.

A low input VSWR will be obtained by the application of 2 equal branches coupled by means of 3 dB –90° hybrids.

3 DESIGN CONSIDERATIONS (SINGLE AMPLIFIER)

3.1 Input and load impedance; gain

For class A operation the BLW98 is specified at V_{CE} = 25 V and I_C = 850 mA.

The corresponding typical gain, input and load impedance according to the Data sheets are as follows:

Table 1

f (MHz)	GAIN (dB)	R_i (SERIES) (Ω)	X_i (SERIES) (Ω)	R_L (SERIES) (Ω)	X_L (SERIES) (Ω)
470	11.2	1.46	+j 2.04	9.98	+j 7.31
547	10.1	1.43	+j 2.45	8.53	+j 6.96
636	9.0	1.38	+j 2.91	7.10	+j 6.34
739	7.9	1.31	+j 3.44	5.77	+j 5.46
860	6.9	1.23	+j 4.04	4.55	+j 4.33

The calculation of the circuit elements for this amplifier is almost analogous to that of the amplifier with two pieces BLW34 being described in report ECO7901 (Ref.1). To facilitate calculations an approximate equivalent circuit for the transistor input and output impedance can be given. It is shown in Fig.1.

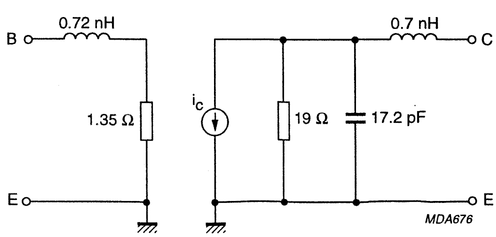


Fig.1

3.2 The output network

The circuit will be designed on double clad printed board with PTFE fibre glass as a dielectric having an $\varepsilon_r = 2.74$.

To keep the dimensions of the printed-circuit board as small as possible we have chosen for a thickness of the board of $^1\!/_{32}$ inch.

The input and output networks start with a piece of stripline having a width of 6 mm, being the width of the base and collector leads. For $^1\!/_{32}$ inch this means a characteristic resistance R_C of appr. 21 Ω.

The collector choke, tuning out the output capacitance of the transistor is executed as a stripline with a width of 2 mm, corresponding to a characteristic resistance of appr. 48 Ω.

For practical reasons the choke is connected to the main transmission line at a distance of 3 mm from the transistor edge.

There are some differences in the design procedure with respect to Ref.1.

1. The length of the transistor collector lead has been cut off at 3 mm to decrease the parasitic capacitance at this point to a minimum.
2. An extra matching section has been added, what increases the number of elements from 7 to 8 of which 7 are optimized with a computer.

More details on the design procedure can be found in Part 1 of this handbook.

The results of the calculations before and after computer optimization are given in Fig.2 and Table 2.

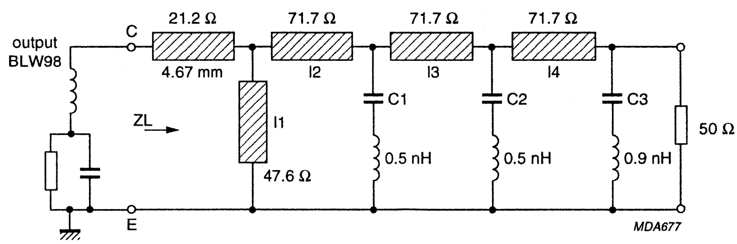


Fig.2

S_{max} is the maximum VSWR of the network.

Table 2

ELEMENT	BEFORE OPTIM.	AFTER OPTIM.	UNIT
l1	21,7	20,5	mm
l2	10,2	9,7	mm
C1	15,18	13,92	pF
l3	26,6	27,0	mm
C2	9,63	6,65	pF
l4	40,2	40,2	mm
C3	3,47	2,23	pF
S_{max}	1,777	1,202	–

The lengths given hold for air lines. The actual lengths on the printed-circuit board are shorter; the reduction factors are 1.455 for the 72 Ω lines, 1.492 for the 48 Ω line and 1.556 for the 21 Ω line.

The predicted minimum output power of the complete amplifier with two transistors BLW98 is:

$$P_{o2} = \frac{2 \times P_{o1}}{S_{max}} \times 0,95 = \frac{2 \times 3,5}{1,202} \times 0,95 = 5,53\ W$$

P_{o1} is the minimum output power of one transistor in a narrow band circuit, S_{max} is as specified above and the factor 0.95 represents the power loss of the hybrid coupler at the output.

3.3 The input network

The design procedure is again almost equal to that given in Ref.1. The differences are:

1. The length of the transistor base terminal has been reduced to 3 mm, instead of the 1.7 mm for the BLW34 transistor. The width is 6 mm, corresponding with an R_C of appr. 21 Ω.
2. The R_C of the other series lines has been chosen at appr. 72 Ω to keep the lines as short as possible.
3. An extra matching section has been added, what increases the number of elements from 5 to 7 of which 5 are optimized with a computer.
4. To obtain a high power gain, both chip capacitors between base and emitter of the BLW98 are soldered as close as possible to the transistor envelope.

See also part 1 of this handbook.

The results of the calculations are summarized in Fig.3 and Table 3.

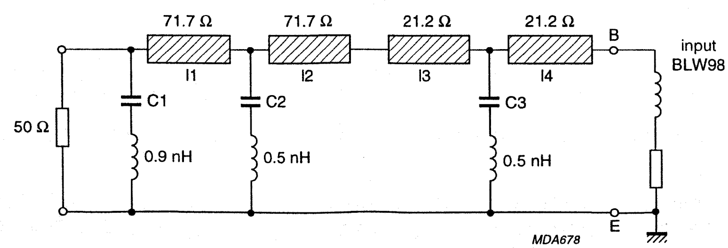


Fig.3 Input BLW98.

Table 3 see note 1

ELEMENT	BEFORE OPTIM.	AFTER OPTIM.	UNIT
C_1	1.24	1.89	pF
l_1	51.6	35.1	mm
C_2	4.42	7.66	pF
l_2	24.8	22.8	mm
l_3	3.11	3.11	mm
C_3	20.3	27.7	pF
l_4	1.56	1.56	mm
ΔG	±1.324	±0.084	dB

Note

1. Later it was discovered that during the initial calculation an error was made. However this was corrected sufficiently by the optimization procedure.

ΔG is the resulting power gain variation caused by the transistor and the input network over the frequency band. The lengths of the lines hold for air as a dielectric. Transformation to striplines on a printed-circuit board is done in the same way as in the previous section.

The minimum power gain of the complete amplifier with two transistors BLW98 is expected to be:

$$G_O = G_T - 2A_H - A_1 - A_2$$

in which: G_T = minimum power gain of BLW98 in a narrow band circuit.

A_H = power loss of one hybrid coupler

A_1 = reflection loss of input network

A_2 = reflection loss of output network.

In practical figures this means:

$$G_O = 6.5 - 2 \times 0.2 - 0.04 - 0.08 = 5.98 \text{ dB}$$

The input VSWR of a single amplifier was calculated to vary from 8.97 at 470 MHz down to 1.32 at 860 MHz.

4 THE HYBRID COUPLED AMPLIFIER

4.1 Practical considerations

On previous pages the theoretical approach of the single amplifier was discussed.

In practice, it was the intention to realize a small compact amplifier on a printed-circuit board with input and output coaxial terminals (R_c = 50 Ω) in-line for easy cascading of several amplifiers.

Besides the wide-band properties it is the intention to obtain a higher output power, so two BLW98 branches are connected in parallel with the aid of two wide-band 3 dB –90° coaxial hybrids on a 50 Ω basis.

So, by using coaxial hybrids the unacceptable situation that the amplifier shows a mismatch to the driver stage, has also been solved.

In such a configuration the output power will be nearly doubled; reduction of the input VSWR of the complete system to a value of around 1.2 may be explained from the properties of the hybrid coupler applied. The reflected power will be absorbed in the resistor matching the isolated port. This resistor is 50 Ω and consists of two 100 Ω power metal film resistors in parallel. The same has been done on the output side.

The printed-circuit board needs to be double copper clad with a PTFE glass fibre dielectric (ε_r = 2.74) for low losses at UHF. The thickness is $^1/_{32}$ inch.

Figure 4 shows the circuit diagram of the complete 2 × BLW98 class A amplifier. The biasing circuit is drawn in Fig.5.

The printed-circuit board is in Fig.6 and the amplifier lay-out in Fig.7.

For a correct earthing the upper earth sheet parts are connected to the lower sheet by soldering copper straps at the edges of the printed-circuit board. The black parts in Fig.7 are the soldered copper straps.

The emitters are grounded as short as possible by applying copper straps under the emitter leads. For that reason the holes in the board are square instead of round.

Both transistors are screwed to an intermediate brass heatsink plate of 10 mm thickness. The polished lower side of the printed-circuit board is in direct contact with the brass plate. For this, small holes are drilled or fraised in the plate.

The coaxial connectors are of the SMA 50 Ω type, being soldered to upper and lower sheet and screwed to the intermediate heatsink.

4.2 Practical optimization

We started with optimization on a small signal basis with the circuit inserted in a network analyzer chain having swept S-parameters facilities. So far, similar tuning methods have been applied as described in Refs. 1 and 2.

Because it is rather complicated to find the best compromise between an acceptable flat gain curve (S21) and sufficient output power with low i.m.d. a dynamic large signal optimization method has been applied. Figure 8 shows the block diagram.

This tuning method is based on the correlation between the single tone 1 dB compression point and the i.m.d. figure of a linear amplifier.

In this set-up the swept output power level of the amplifier under test is kept constant and the required (detected) drive power is monitored on an oscilloscope screen (PM 3260).

The swept drive power is available from the sweep generator HP8620C in combination with RF plug-in unit HP86222A. Because the output power of this system is too low viz. appr. 20 mW (+13 dBm) a combined amplifier with BLW32 and BLW33 (Ref.2) cascaded with an amplifier with 2 × BLW34 (Ref.1) have been added. The latter combination shows an overall gain of appr. 29 dB in the range 470 – 860 MHz.

When the circuit under test is inserted in the chain of Fig.8 the input power measured on port C of hybrid 1 corresponds in principle with the gain curve (S_{21}) being measured with the network analyzer; in fact one is the inverse of the other.

When the drive level is slowly increased, the shape of the gain curve changes somewhat when compression starts. By careful retuning of the amplifier the shape of the gain curve can be corrected again in the direction of the original smaller signal curve.

In this way the amplifier of Ref.1 was aligned.

Figure 8 shows that a PM5715 pulse generator is added to the chain. It creates an amplitude variation of the sweep generator (via the external AM input). So, the compression level can be monitored in a dynamical way, what improves the alignment procedure.

The actual single tone output power has been measured with the aid of calorimetric watt meter HP 435A when the action of the sweep is stopped and the external AM switched off. Figure 9 gives an idea of the screen picture with and without compression visible.

4.3 Intermodulation, VSWR and gain measurements

For i.m.d. measurements on television systems the post offices advise and apply the 3-tone test method (vision carrier −8 dB, sound carrier −7 dB, side band signal −16 dB; zero dB corresponds to peak sync level). According to the CCIR system the frequency is given by the vision carrier and the sound carrier is 5.5 MHz above this one.

The wide-band test set-up is according to the chain in report ECO7901, (Ref.1). In this set-up first the sound and vision carriers are each buffered by a circulator and then joined in a wide-band coaxial hybrid. Then the sideband signal from the (smaller) generator SMLU is added in a second hybrid (no circulator applied).

The complete 3-tone signal passes a low-pass filter (700 or 1 000 MHz cut-off depending on the input frequency), a continuously variable attenuator and a circulator (three different types are needed to cover at least the range 470 – 860 MHz).

The output power is measured with a 435 A calorimetric watt meter (multiplication factor for the 3-tone –7, –8, –16 dB operation is 2.61) and the i.m.d. observed via a loosely coupled 50 Ω pick-off device with a HP 8558B spectrum analyzer.

Figure 10 shows the 3-tone i.m.d. results measured on a complete hybrid coupled 2 × BLW98 amplifier. $P_{o\,sync}$ was measured for i.m.d. distances of –52, –56, and –60 dB. The heatsink temperature amounts to appr. 60 °C.

Finally, input and output VSWR and gain figures were measured only under small signal conditions. The VSWR figures of the input and output are expressed in reflection damping (resp. S_{11} and S_{22}) on a 50 Ω basis (see Figs 11, 12 and 13).

According to Fig.11 the minimum reflection damping of the input of the coaxial hybrid amounts to S_{11} = –19 dB at 470 MHz what corresponds with a maximum VSWR of 1.25.

On the output side the worst reflection damping amounts to S_{22} = –16 dB (VSWR = 1.38) at both band ends. Both values may be mainly explained from the specified maximum VSWR = 1.25 of the applied Anaren hybrids and the fact that the load of the isolated port consists of two metal film power resistors of 100 Ω in parallel having low frequency tolerances of 5%.

The power gain, represented by S_{21}, is at least 7 dB (Fig.12). For a second check this gain curve has been measured step by step for an output power of 600 mW. Figure 14 shows the results.

4.4 Cross-modulation

There is a trend now that the cross modulation behaviour of a linear amplifier becomes more important. For this reason tests have been done and the results given in this report (Figs 15 to 19).

These tests could be done in the 3-tone chain with the sideband carrier switched off. The vision carrier has been made equal to $P_{o\,sync}$ (0 dB), instead of –8 dB, whilst the sound carrier remains –7 dB (5 × power).

By means of a coaxial switch and a 20 dB attenuator, inserted in the vision carrier chain, this carrier can be switched from 0 to –20 dB.

Increasing both tones with the same factor and switching periodically the vision carrier from 0 to –20 dB the procentual influence on the sound carrier (with the spectrum analyzer switched to linear operation) is measured with respect to its original level.

5 CONCLUSION

On preceding pages the theoretical and practical design has been described of a wide-band (470 – 860 MHz) high quality linear amplifier being equipped with two BLW98 transistors operating in class A. The target $P_{o\,sync} \geq 6$ W and power gain ≥ 7 dB was reached.

There are some small differences between the theoretical design and the practical circuit, viz.

- The calculated value for the chip capacitors $C_7 = C_{10}$ was 3.9 pF. In practice 1.5 pF appeared to be a better choice.
- $C_{22} = C_{24}$ = 6.8 pF was too small, so $C_{21} = C_{23}$ = 1 pF has been added.
- $C_{29} = C_{32}$ was planned as a fixed chip capacitor of 1.2 pF; tuning this point with a variable capacitor of 1 – 3,5 pF gave advantages.

6 REFERENCES

Ref.1: A.H. Hilbers and M.J. Köppen - A wide-band linear power amplifier (470 – 860 MHz) with two transistors BLW34. C.A.B. report ECO7901.

Ref.2: A.H. Hilbers and M.J. Köppen - Wide-band linear power amplifiers (470 – 860 MHz) with the transistors BLW32 and BLW33. C.A.B. report ECO7806.

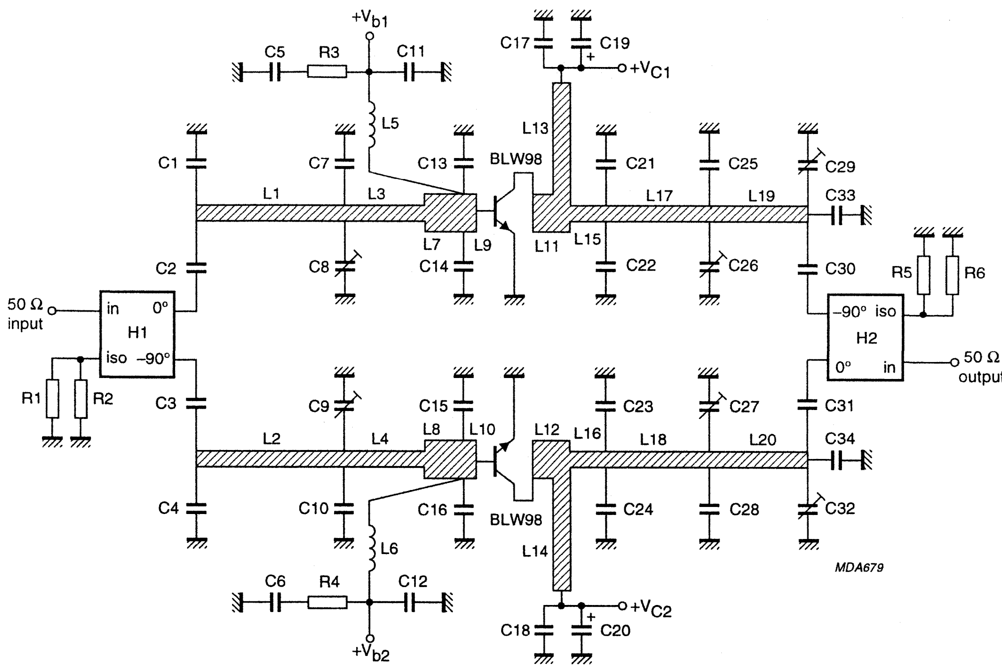


Fig.4

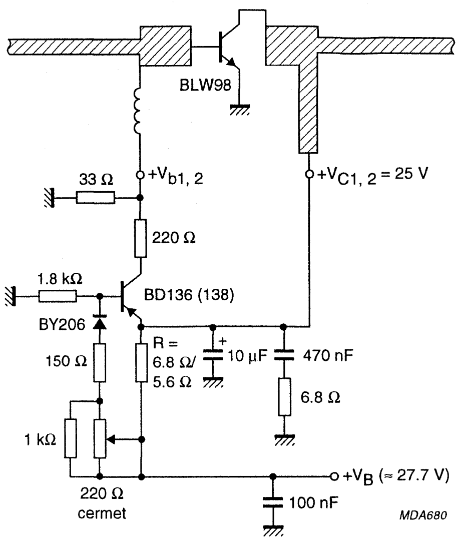

BLW98
33 Ω
+Vb1, 2
+VC1, 2 = 25 V
220 Ω
1.8 kΩ
BD136 (138)
BY206
R =
6.8 Ω/
5.6 Ω
10 µF
470 nF
150 Ω
6.8 Ω
1 kΩ
+VB (≈ 27.7 V)
220 Ω
cermet
100 nF
MDA680

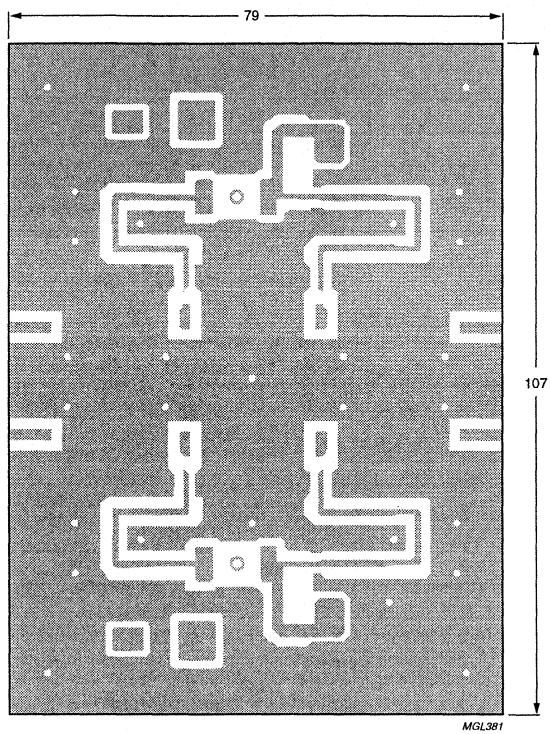
Fig.5

List of components

$C_1 = C_4 = 1.8$ pF	multilayer ceramic chip capacitor (ATC type: 100 A – 1R8 – B – P_X – 50)
$C_2 = C_3 = C_{30} = C_{31} = 100$ pF	multilayer ceramic chip capacitor (cat. no. 2222 851 13101)
$C_5 = C_6 = C_{39} = C_{40} = 100$nF	polyester capacitor
$C_7 = C_{10} = C_{25} = C_{28} = 1.5$ pF	multilayer ceramic chip capacitor (ATC type: 100 A – 1R5 – B – P_X – 50)
C8 = C9 = C26 = C27	1.4 to 5.5 pF film di-electric trimmer (cat. no. 2222 809 09001)
$C_{11} = C_{12} = C_{17} = C_{18} = 100$ pF	multilayer ceramic chip capacitor (cat. no. 2222 852 13101)
$C_{13} = C_{16} = 15$ pF	multilayer ceramic chip capacitor (cat. no. 2222 851 13159)
$C_{14} = C_{15} = 12$ pF	multilayer ceramic chip capacitor (cat. no. 2222 851 13129)
$C_{19} = C_{20} = 6.8$ µF, 63 V	electrolytic capacitor
$C_{21} = C_{24} = 2 \times 6.8$ pF in parallel	multilayer ceramic chip capacitor (ATC type: 100 A – 6R8 – J – P_X – 50)
$C_{22} = C_{23} = C_{33} = C_{34} = 1$ pF	multilayer ceramic chip capacitor (ATC type: 100 A – 1R0 – B – P_X – 50)
$C_{29} = C_{32} = 1 - 3.5$ pF	film dielectric trimmer (cat. no. 2222 809 05001)
$C_{35} = C_{36} = 10$ µF, 63 V	electrolytic capacitor
$C_{37} = C_{38} = 470$ nF	polyester capacitor
$R_1 = R_2 = R_5 = R_6 = 100\ \Omega$ (± 5%)	power metal film resistor PR37 type (cat. no. 2322 191 31001)
$R_3 = R_4 = R_{21} = R_{22} = 10\ \Omega$ (± 5%)	carbon resistor; CR25 type
$R_7 = R_8 = 1.8$ kΩ (± 5%)	CR25 type
$R_9 = R_{10} = 1$ kΩ (± 5%)	CR25 type
$R_{11} = R_{12} = 33\ \Omega$ (± 5%)	CR25 type
$R_{13} = R_{14} = 150\ \Omega$ (± 5%)	CR25 type
$R_{15} = R_{16} = 220\ \Omega$	cermet preset potentiometer
$R_{17} = R_{18} = 220\ \Omega$ (± 5%)	power metal film resistor PR52 type (cat. no. 2322 192 32201).
$R_{19} = R_{20} = 5.6\ \Omega$ (± 5%) and $6.8\ \Omega$ (± 5%)	in parallel; enamelled wire-wound resistors WR 0617 style
H1 – H2	ultra-miniature 3 dB –90° coupler model no. 10264-3, range 0.5 – 1.0 GHz; Anaren Microwave Inc.
$L_1 = L_2$	stripline ($Z_C = 72\ \Omega$), 24.1×1.0 mm^2; note 1
$L_3 = L_4$	stripline ($Z_C = 72\ \Omega$), 15.7×1.0 mm^2; note 1
$L_5 = L_6 = 5.6$ µH	29 turns closely wound enamelled Cu wire (0.2 mm); int. dia 3.0 mm
$L_7 = L_8$	stripline ($Z_C = 21\ \Omega$), 2.0×6.0 mm^2;note 1
$L_9 = L_{10}$	stripline ($Z_C = 21\ \Omega$), 1.0×6.0 mm^2; note 1
$L_{11} = L_{12}$	stripline ($Z_C = 21\ \Omega$), 3.0×6.0 mm^2; note 1
$L_{13} = L_{14}$	stripline ($Z_C = 48\ \Omega$), 13.8×2.0 mm^2; note 1
$L_{15} = L_{16}$	stripline ($Z_C = 72\ \Omega$), 6.7×1.0 mm^2; note 1
$L_{17} = L_{18}$	stripline ($Z_C = 72\ \Omega$), 18.5×1.0 mm^2; note 1
$L_{19} = L_{20}$	stripline ($Z_C = 72\ \Omega$), 27.6×1.0 mm^2; note 1

Note

1. These striplines are printed on double Cu-clad printed-circuit board with PTFE fibre-glass dielectric ($\varepsilon_r = 2.74$); thickness 1⁄32 inch.



Copper strap soldered between upper and lower sheet.

Fig.6 printed-circuit board.

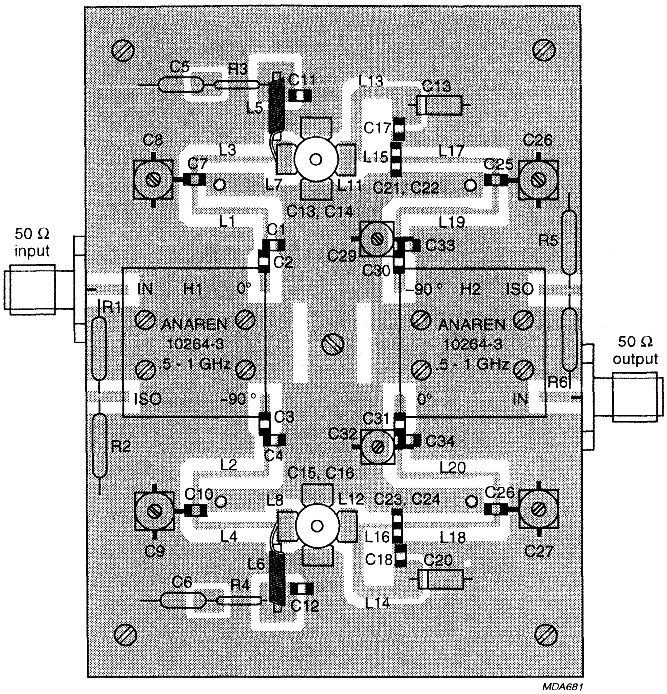


Fig.7 Amplifier lay-out.

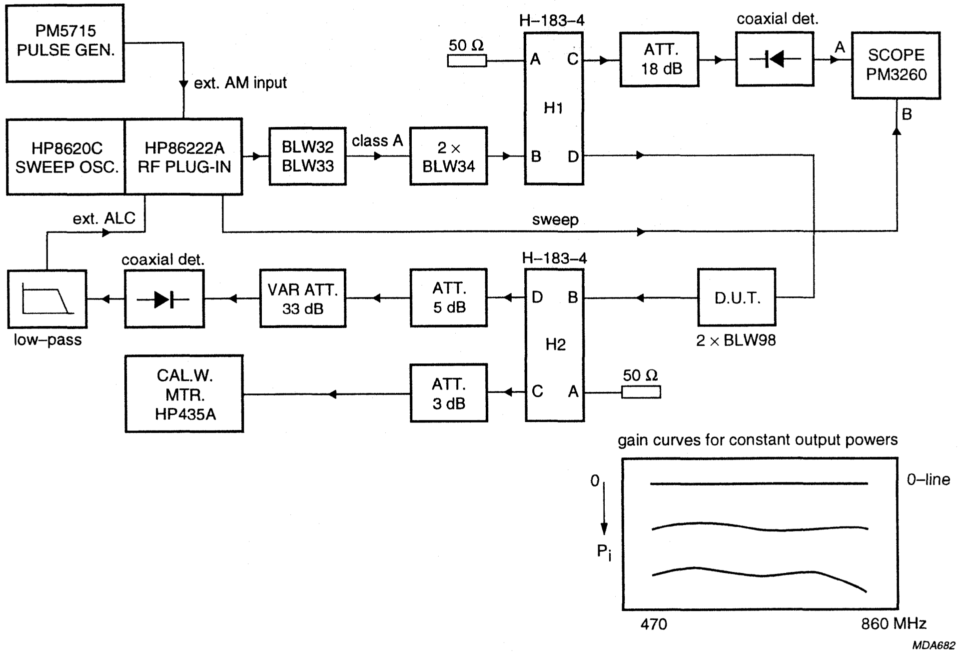


Fig.8 Dynamic compression test set-up.

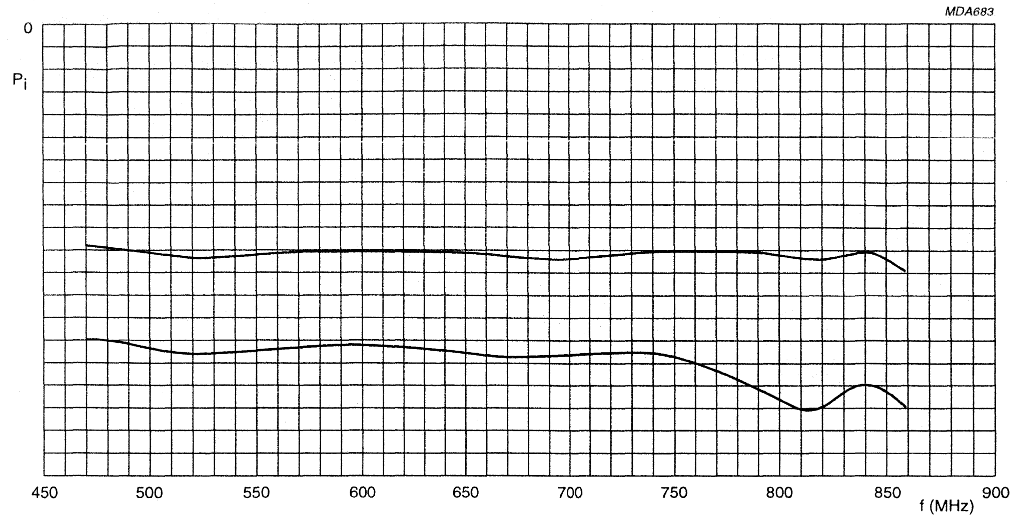

MDA683
0
P_i
450
500
550
600
650
700
750
800
850
900
f (MHz)

Fig.9

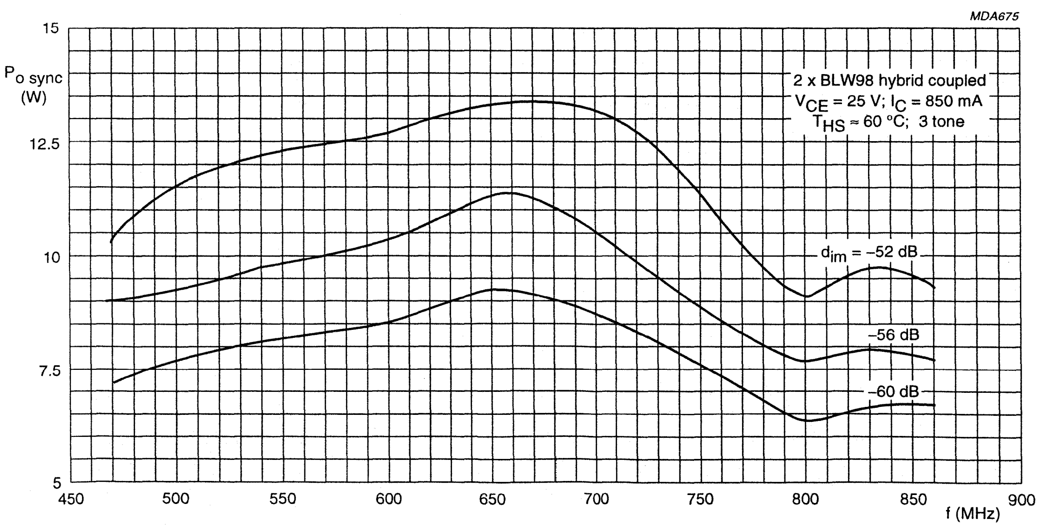

MDA675
15
$P_{o\ sync}$ (W)
12.5
10
7.5
5
2 x BLW98 hybrid coupled
V_{CE} = 25 V; I_C = 850 mA
T_{HS} ≈ 60 °C; 3 tone
d_{im} = −52 dB
−56 dB
−60 dB
450
500
550
600
650
700
750
800
850
900
f (MHz)

Fig.10

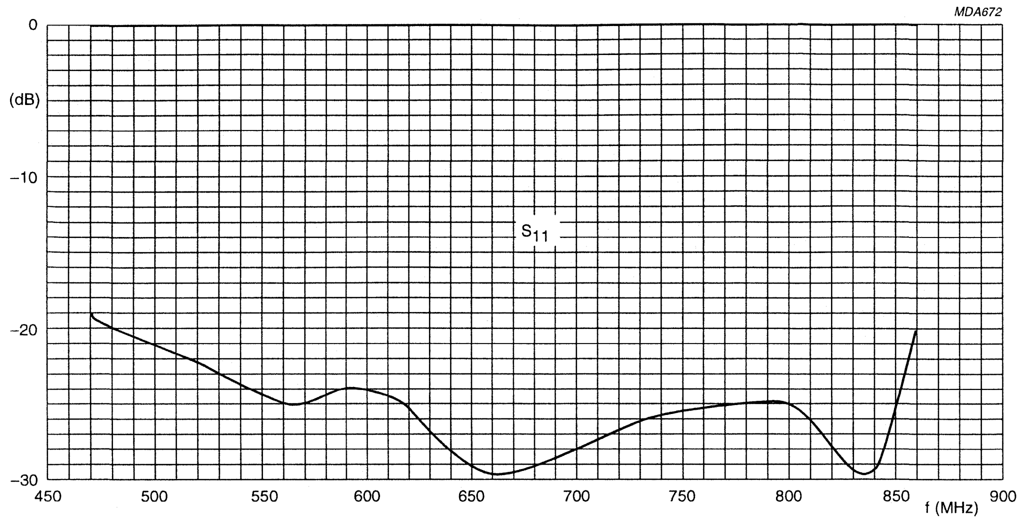

MDA672
0
(dB)
−10
s_{11}
−20
−30
450
500
550
600
650
700
750
800
850
900
f (MHz)

Fig.11

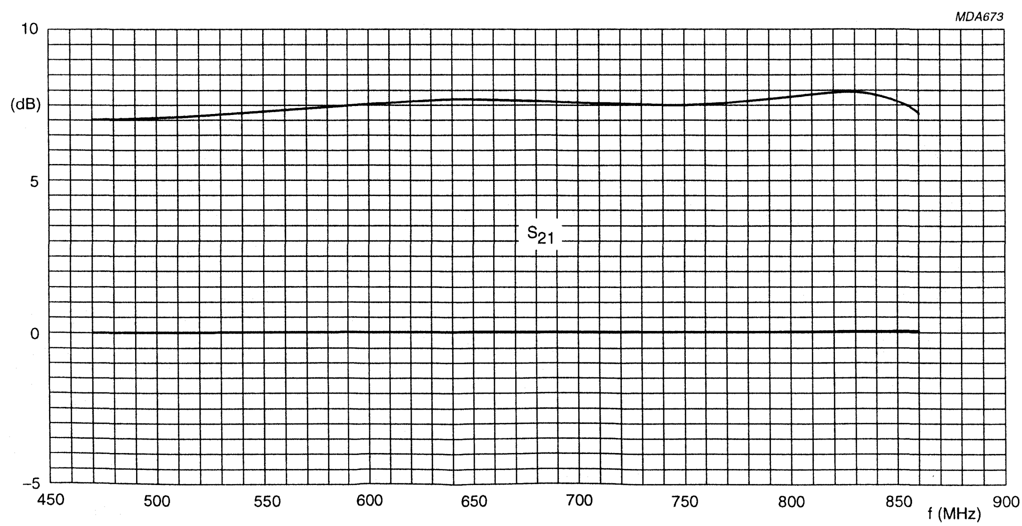

MDA673
10
(dB)
5
s_{21}
0
−5
450
500
550
600
650
700
750
800
850
900
f (MHz)

Fig.12

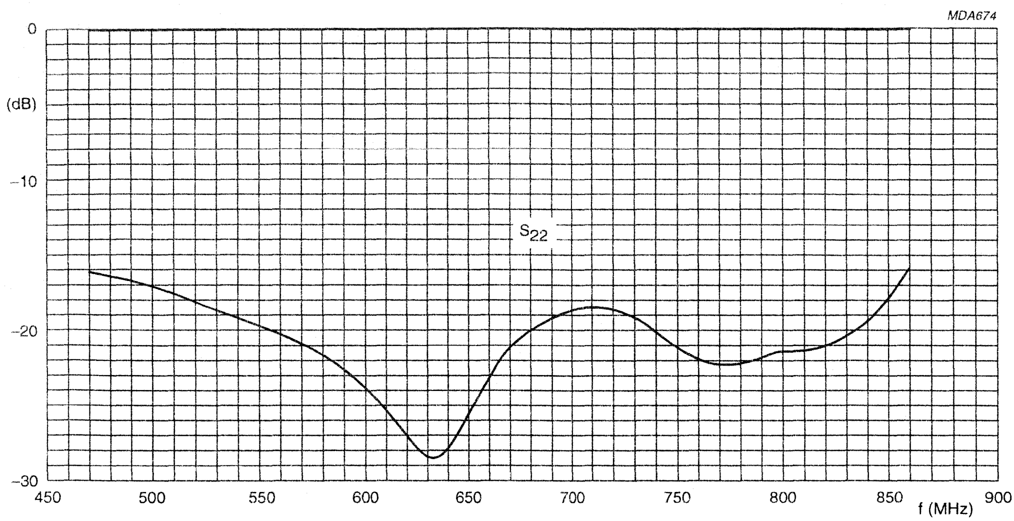

MDA674
0
(dB)
−10
S_{22}
−20
−30
450
500
550
600
650
700
750
800
850
900
f (MHz)

Fig.13

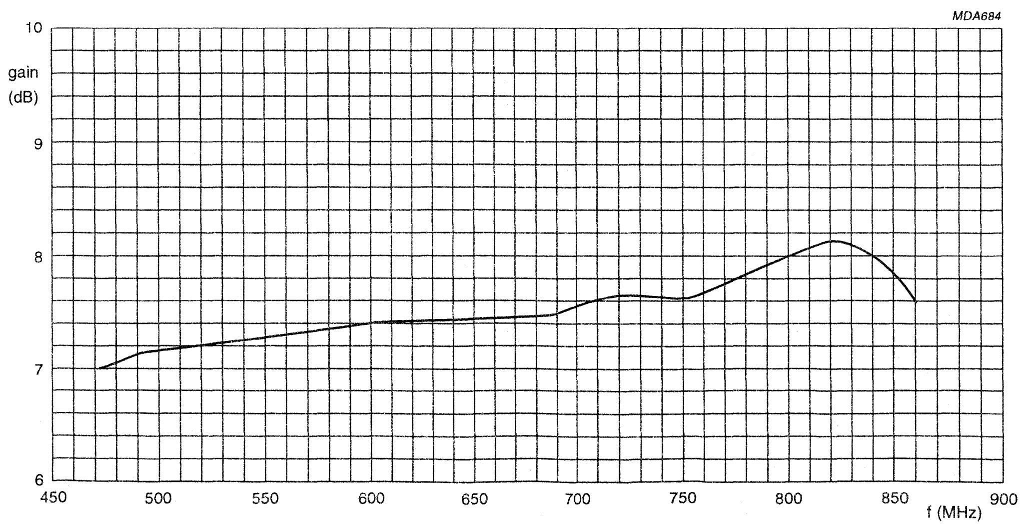

MDA684
10
gain
(dB)
9
8
7
6
450
500
550
600
650
700
750
800
850
900
f (MHz)

Fig.14

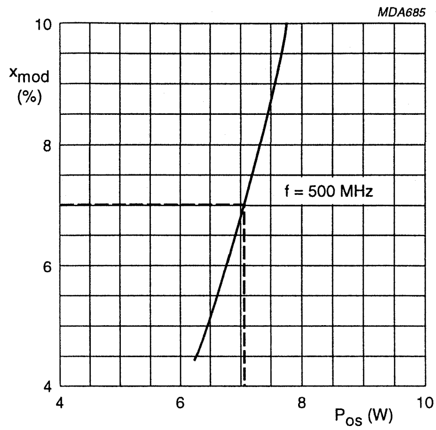

MDA685
10
x_{mod}
(%)
8
6
4
4
6
8
10
f = 500 MHz
P_{os} (W)

Fig.15

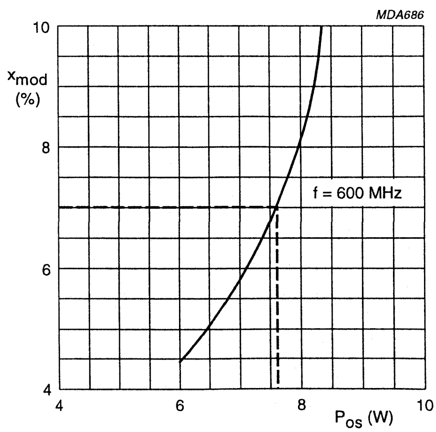

MDA686
10
x_{mod}
(%)
8
6
4
4
6
8
10
f = 600 MHz
P_{os} (W)

Fig.16

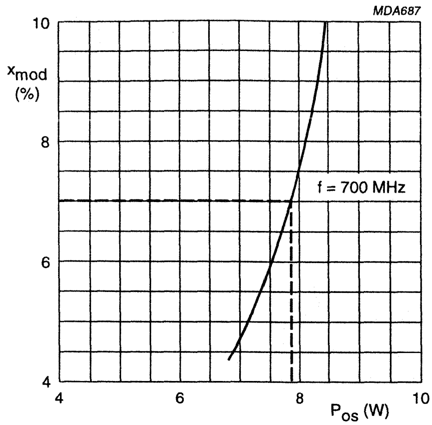

MDA687
10
x_{mod} (%)
8
6
4
4
6
8
10
P_{os} (W)
f = 700 MHz

Fig.17

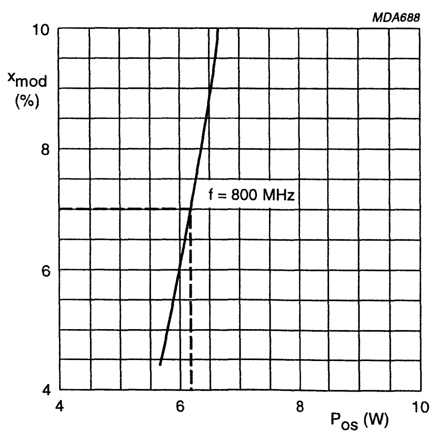

MDA688
10
x_{mod} (%)
8
6
4
4
6
8
10
P_{os} (W)
f = 800 MHz

Fig.18

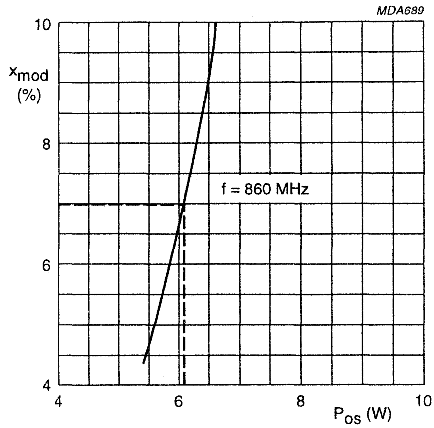


Fig.19

A Wideband hybrid coupled amplifier (470 – 860 MHz) with 2 balanced transistors BLV57

Application Note NCO8101

1 ABSTRACT

For application in TV transposers in band 4 and 5 (470 – 860 MHz) a wideband linear power amplifier has been designed with two balanced transistors BLV57 coupled by means of 3 dB –90° hybrids. The class-A DC-setting of the transistors is $I_C = 2 \times 850$ mA and $V_{CE} = 25$ V. The main properties of the two prototypes are:

Table 1

470 – 860 MHz	UNIT	AMPLIFIER 2	AMPLIFIER 3
Gain ($P_i = 1$ mW)	dB	9.3 ±0.5	9 ±0.5
Return losses input	dB	≥17	≥16
Return losses output	dB	≥19	≥19
P_o at 1 dB gain compression	W	≥28	≥28
P_o at –55 dB intermod. (3-tone, –7, –8 and –16 dB)	W	≥17.5	≥17.5
Cross modulation at $P_o = 15$ W	%	≤9.4	≤8.8

2 INTRODUCTION

For application in TV transposers for band 4 and 5 (470 – 860 MHz) a wideband linear power amplifier has been designed with two transistors BLV57 in class-A. The BLV57 is a balanced transistor (two identical chips) in a single envelope with a ceramic cap (SOT-161).

3 DESIGN OF THE AMPLIFIER

3.1 General remarks

The schematic line-up of the complete amplifier is given in Fig.1.

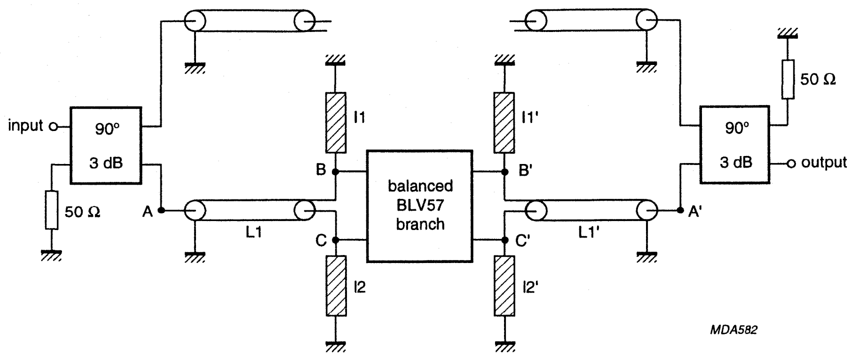


Fig.1 Schematic line-up of the complete amplifier.

The amplifier consists of 2 balanced circuits, both equipped with a BLV57 and coupled in parallel by means of a wideband 3 dB –90° coaxial hybrid at the input and output. Each BLV57 has 2 input circuits (one for each chip) connected to a coax balun (L1 and L1') which splits a 50 Ω unbalanced port (A) in two 25 Ω ports (B and C). The phase-shift between B and C is 180°. The baluns (L1 and L1') are 50 Ω semi-rigid coax cables, soldered over the whole length atop a transmission line (l_1 or l_1') of 2 mm width. To maintain circuit symmetry another shorted stub (l_2 or l_2') with the same length has been added. For the amplifier a printed-circuit board has been applied of PTFE fibreglass with an $\varepsilon_r = 2.74$, copper clad on both sides with a thickness of $1/32$ inch. To get a good contact between upper and lower side, rivets have been used at several places and copper straps have been soldered at the edges of the board.

3.2 Bias circuit

Each transistor has its own bias unit to obtain a stable DC-setting (see Fig.4). This bias unit enables the adjustment of the base current of each chip of the BLV57 by means of potentiometer R_8, to obtain equal collector currents. The potentiometer R_1 adjusts both base currents simultaneous. After an accurate measurement of the values of resistors R_{12} and R_{13} the collector currents of the BLV57, and the difference between them, can be determined easily by measuring the voltage-drop over these resistors. The supply voltage of this bias unit is 28 V. Figure 5 shows the positive copy of the printed-circuit board and the lay-out of the bias unit.

3.3 Some properties of the BLV57

For class-A operation the BLV57 is specified at $I_C = 2 \times 850$ mA and $V_{CE} = 25$ V. The typical gain, input and load impedance of a half BLV57 (one chip) are given in Table 2.

Table 2

FREQUENCY (MHz)	GAIN (dB)	INPUT IMPEDANCE (Ω)	LOAD IMPEDANCE (Ω)
470	13.13	1.11 + j 2.62	9.75 + j 6.52
507	12.57	1.13 + j 2.88	9.00 + j 6.29
547	12.02	1.14 + j 3.17	8.26 + j 5.99
590	11.49	1.16 + j 3.47	7.52 + j 5.60
636	10.98	1.18 + j 3.80	6.80 + j 5.14
686	10.49	1.21 + j 4.16	6.10 + j 4.60
739	10.03	1.25 + j 4.55	5.44 + j 3.99
797	9.60	1.30 + j 5.00	4.80 + j 3.29
860	9.20	1.37 + j 5.50	4.20 + j 2.52

3.4 Output network

The 25 Ω of the balun has to be transformed into the optimum load for the half transistor (one chip), which is given in Table 2. This is done by means of an L – C output network. The circuit has been calculated according to Ref. 1 and submitted to a computer optimization program. Because the BLV57 is a balanced transistor with two identical chips, there are two identical output circuits with a virtual ground between them. Figure 2 shows the calculated output circuit connected to the balun, described in Section 3.1. Two capacitors of 2.2 pF and a resistor of 12 Ω prevent oscillation at higher frequencies.

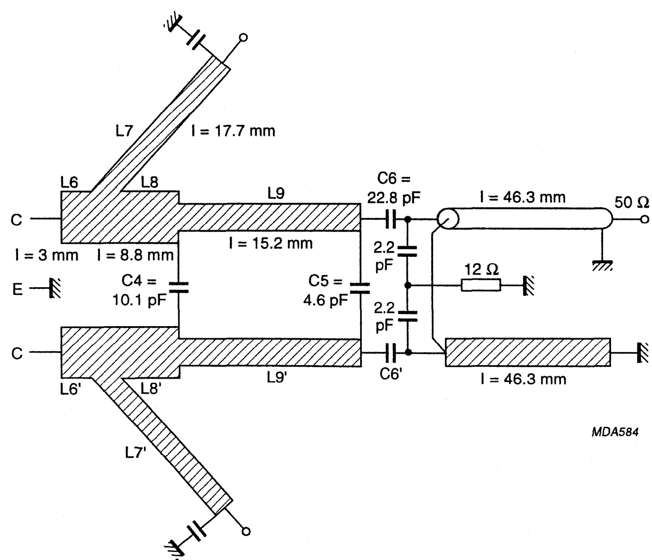


Fig.2 Calculated output circuit.

The stripline L_6 (width 3 mm) is the soldering place for the collector lead. The transistor is biased through the stripline L_7 (width 2 mm). This stripline has been connected to L_6 and L_8 at a distance of 3 mm from the transistor. L_8 is a stripline with a width of 3 mm and L_9 with a width of 1.5 mm. C_4 consists of a chip capacitor in parallel with a film dielectric trimmer. C_5 is a film dielectric trimmer and C_6 is a chip capacitor.

3.5 Input network

In the frequency range of 470 – 860 MHz the gain of a half BLV57 (one chip) varies about 4 dB (see Table 2). To decrease this gain slope an appropriate mismatch at the lower frequencies is necessary. The increasing insertion losses of the network approximately compensate the increasing gain at the lower frequencies. This method is described in Ref. 2. For the same reason as described in Section 3.4 there are two identical input circuits with a virtual ground between them. Figure 3 shows the calculated input circuit after computer optimization connected to the coaxial balun, described in Section 3.1.

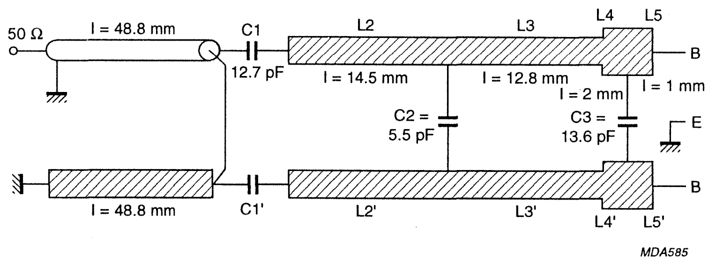


Fig.3

The striplines L_4 and L_5 (width 3 mm) form together the soldering place of the base lead. The width of the striplines L_2 and L_3 is 1.5 mm. The capacitors C_1, C_2, and C_3 are chip capacitors. The circuit of a complete branch (see Fig.1) is given in Fig.6.

4 ADJUSTMENT OF THE AMPLIFIER

4.1 Output circuit

To obtain the highest possible output power it is essential that the transistor is given that load admittance which gives the least distortion in the used frequency range. Therefore, for tuning, the transistor has to be replaced by a dummy consisting of a resistor and a capacitor in parallel to represent the complex conjugate of the optimum load admittance. The value of this dummy (soldered between the connection points of both collectors) has been calculated on

39 Ω//8.2 pF. With the help of this dummy the output circuit has to be adjusted for good return losses at the output of L_{10} by tuning the capacitors C_{10} and C_{17} and by shifting the capacitors C_{13} and C_{14} on L_7 and L_{17} (see Fig.6). The position of the capacitors C_{13} and C_{14} on the striplines determines the value of L_7 and L_{17}. A typical curve of the return losses at the output of L_{10} after tuning is given in Fig.7.

4.2 Input circuit

Before tuning the input circuit, the dummy has to be replaced by the transistor, with a DC-adjustment of $I_C = 2 \times 850$ mA and $V_{CE} = 25$ V. To decrease the gain-slope of the branch the input circuit has a mismatch at lower frequencies (see Section 3.5). To achieve a sufficient flat gain the capacitance of C_1, C_2, C_3, and C_4 and also the position of C_3 and C_4 (see Fig.6) can be optimized in a sweep set-up under small signal conditions ($P_i = 1$ mW). A typical gain curve of a balanced branch (one BLV57) and the corresponding return losses are given in Figs 9 to 11. It is obvious that the worse return losses at the lower frequencies are produced by the mismatch of the input circuit.

5 THE HYBRID COUPLED AMPLIFIER

In the previous section the adjustment of a balanced branch with one BLV57 has been discussed. The gain is made flat at the cost of impermissibly high return losses. Therefore, in practice, two wideband branches are coupled in parallel by means of two wideband 3 dB –90° coaxial hybrids. The properties of these hybrids reduce the return losses to at least 16 dB. The reflected power of the balanced branches is absorbed by a 50 Ω resistance at the isolated port (see Fig.1). Figure 12 gives a positive copy of the printed-circuit board of the complete amplifier. It also shows the lay-out of this complete amplifier.

6 MEASURED PERFORMANCE

6.1 Small signal gain and return losses

Figures 13 to 15 show the gain and return losses as a function of the frequency, measured under small signal conditions. Results:

Table 3

470 – 860 MHz	UNIT	AMPLIFIER 2		AMPLIFIER 3	
		MIN.	MAX.	MIN.	MAX.
Gain	dB	8.8	9.8	8.5	9.5
Return losses input	dB	17	30.5	16	30
Return losses output	dB	17	39	18	40

6.2 Gain compression

Figures 16 and 17 show the measured P_o versus P_i curves at 600 MHz, which is the most critical frequency in the range. Gain compression of 1 dB occurs at an output power of about 28 W for both amplifiers.

6.3 Intermodulation

In Fig.18 the output power ($P_{o\,sync}$) is given as a function of the frequency at three intermodulation levels. It has been measured according the 3-tone test method (vision carrier: –8 dB, sound carrier: –7 dB and sideband signal: –16 dB). Zero dB corresponds to the peak sync. level. The minimum output power at –60 dB intermodulation amounts to 12.4 W for amplifier 2 and 12.2 W for amplifier 3.

6.4 Cross modulation

Figure 19 shows the cross modulation as a function of the frequency at two $P_{o\ sync}$ levels. It is a 2-tone measurement (vision carrier: 0 dB and sound carrier: –7 dB). The amplitude of the vision carrier is changed from white level (–20 dB) to peak sync level (0 dB). The observed change of the voltage amplitude of the sound carrier is called cross modulation. It is expressed as a percentage of the amplitude of the sound carrier (vision carrier at white level). It has been measured with a spectrum analyser operating in linear mode. At a $P_{o\ sync}$ level of 15 W the cross modulation of amplifier 2 varies from 3.4 to 9.4% and of the amplifier 3 from 4.1 to 8.8%.

7 CONCLUSIONS

It is possible to build a linear power amplifier with excellent performance with two transistors BLV57. The main properties of the two prototypes are shown in Table 4.

Table 4

BAND 4/5	UNIT	AMPLIFIER 2	AMPLIFIER 3
Gain (P_i = 1 mW)	dB	9.3 ±0.5	9 ±0.5
Return losses input	dB	≥17	≥16
Return losses output	dB	≥19	≥19
P_o at 1 dB gain compression	W	≥28	≥28
$P_{o\ sync}$ at –55 dB intermod. (3-tone, –7, –8 and –16 dB)	W	≥17.5	≥17.5
cross modulation at P_o = 15 W	%	≤9.4	≤8.8

8 REFERENCES

Ref.1
G.L. Matthaei.
Tables of Chebychev impedance transforming networks of low pass filter form.
Proc. of the IEEE, August 1964.

Ref.2
O. Pitzalis Jr. and R.A. Gibson.
Tables of impedance matching networks which approximate prescribed attenuation versus frequency slopes.
IEEE transactions on microwave theory and techniques, vol. MTT 119, no. 4, April 1971.

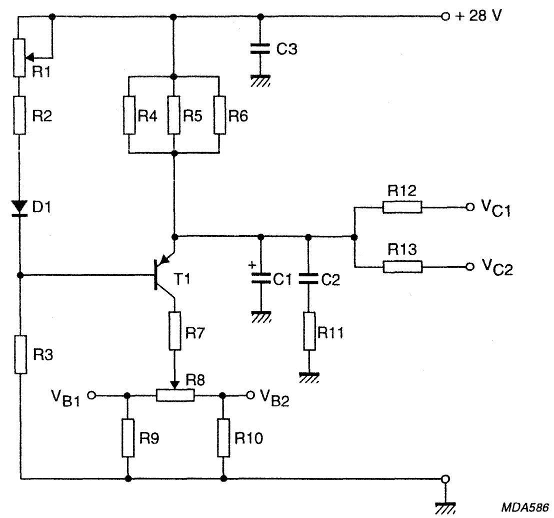


Fig.4 Bias circuit.

Table 5 Parts list of bias circuit (Fig.4)

C_1 = 10µF	63 V electrolytic capacitor	2222 030 28109
C_2 = 470 nF	metallised film capacitor	4322 352 45474
C_3 = 100 nF	metallised film capacitor	2222 352 45104
R_1 = 100 Ω	cermet potentiometer	2122 350 00066
R_2 = 120 Ω	CR 25 type	2322 211 13121
R_3 = 1 500 Ω	CR 25 type	2322 211 13152
$R_4 = R_5 = R_6$ = 4.7 Ω	enamelled wire-wound	2322 330 22478
R_7 = 82 Ω	enamelled wire-wound	2322 330 22829
R_8 = 20 Ω	cermet potentiometer	2122 350 00057
$R_9 = R_{10}$ = 39 Ω	CR 25 type	2322 211 13399
R_{11} = 10 Ω	CR 25 type	2322 211 13109
$R_{12} = R_{13}$ = 0.15 Ω	wire-wound PM 10 type	2322 326 51157
D_1 = BY 206		
T_1 = BD 140		

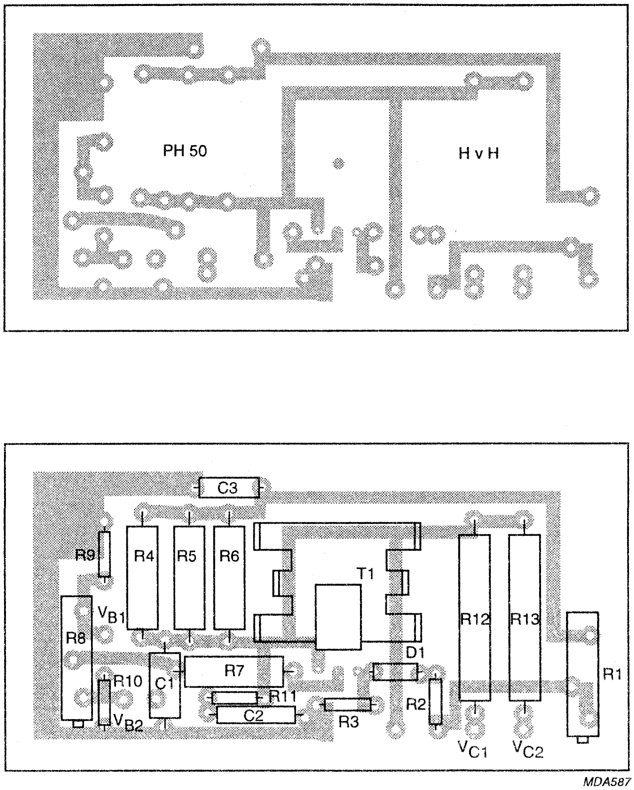


Fig.5 Printed-circuit board lay-out of the bias unit.

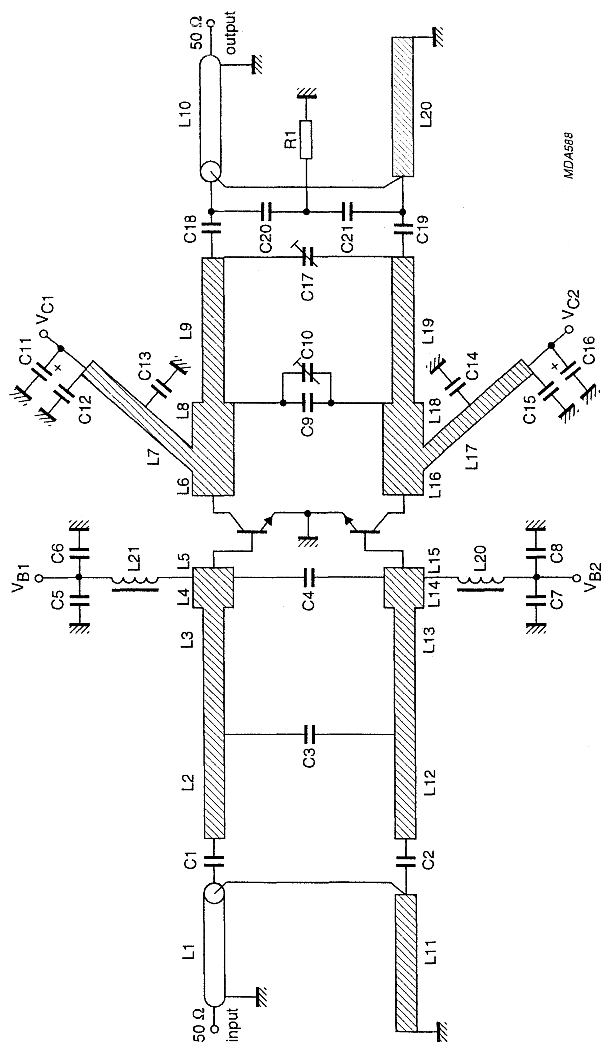


Fig.6 Circuit of a BLV57 branch.

Table 6 List of components BLV57 branch

$C_1 = C_2 = 10$ pF chip capacitor	Philips NPO	2222 851 13109
$C_3 = 3.9$ pF chip capacitor	Johanson	no. 500 R 15 N 3R9 CA
$C_4 = 12$ pF chip capacitor	Philips NPO	2222 851 13129
$C_5 = C_7 = C_{12} = C_{15} = 100$ nF chip capacitor	Philips NPO	2222 855 48104
$C_6 = C_8 = 100$ pF chip capacitor	Philips NPO	2222 852 13101
$C_9 = 8.2$ pF chip capacitor	ATC	8R2J
$C_{10} = C_{17} = 1 - 3.5$ pF film dielectric trimmer	Philips	2222 809 05001
$C_{11} = C_{16} = 6.8$ µF, 40 V, electrolytic capacitor	Philips	2222 030 37688
$C_{13} = C_{14} = 110$ pF chip capacitor	ATC	111J
$C_{18} = C_{19} = 22$ pF chip capacitor	Philips NPO	2222 851 13229
$C_{20} = C_{21} = 2.2$ pF chip capacitor	Johanson	no. 500 R 15 N 2R2 BA
$L_1 = 49$ mm semi-rigid coax, 2.2 mm ∅	$Z_C = 50\ \Omega$	PTFE dielectric, soldered on 2 mm stripline
$L_2 = L_{12}$ = stripline	$Z_C = 57\ \Omega$	14.5 × 1.5 mm
$L_3 = L_{13}$ = stripline	$Z_C = 57\ \Omega$	12.8 × 1.5 mm
$L_4 = L_{14}$ = stripline	$Z_C = 36\ \Omega$	2 × 3 mm
$L_5 = L_{15}$ = stripline	$Z_C = 36\ \Omega$	1 × 3 mm
$L_6 = L_{16}$ = stripline	$Z_C = 36\ \Omega$	3 × 3 mm
$L_7 = L_{17}$ = stripline	$Z_C = 48\ \Omega$	17.7 × 2 mm
$L_8 = L_{18}$ = stripline	$Z_C = 36\ \Omega$	8.8 × 3 mm
$L_9 = L_{19}$ = stripline	$Z_C = 57\ \Omega$	15.2 × 1.5 mm
$L_{10} = 46$ mm semi-rigid coax, 2.2 mm ∅	$Z_C = 50\ \Omega$	PTFE dielectric, soldered on 2 mm stripline
L_{11} = stripline	$Z_C = 50\ \Omega$	49 × 2 mm
L_{20} = stripline	$Z_C = 50\ \Omega$	46 × 2 mm
$L_{21} = L_{22} = 470$ nH micro choke		4322 057 04771
$R = 12\ \Omega$	CR 25 type,	2322 211 13129

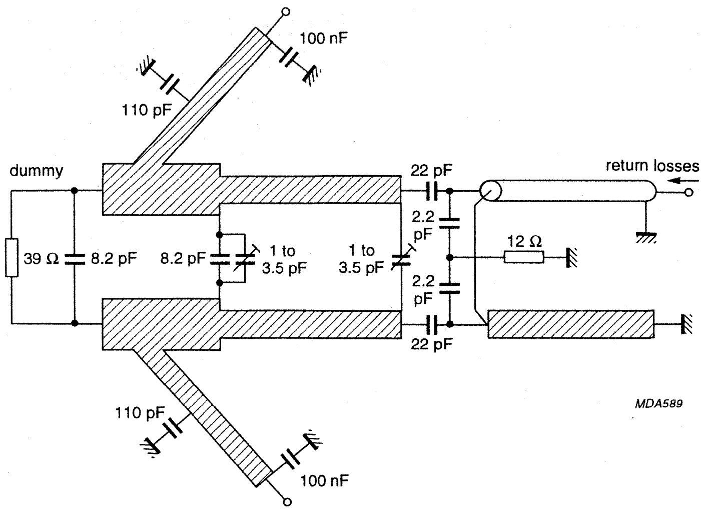


Fig.7 Tuning circuit of the output.

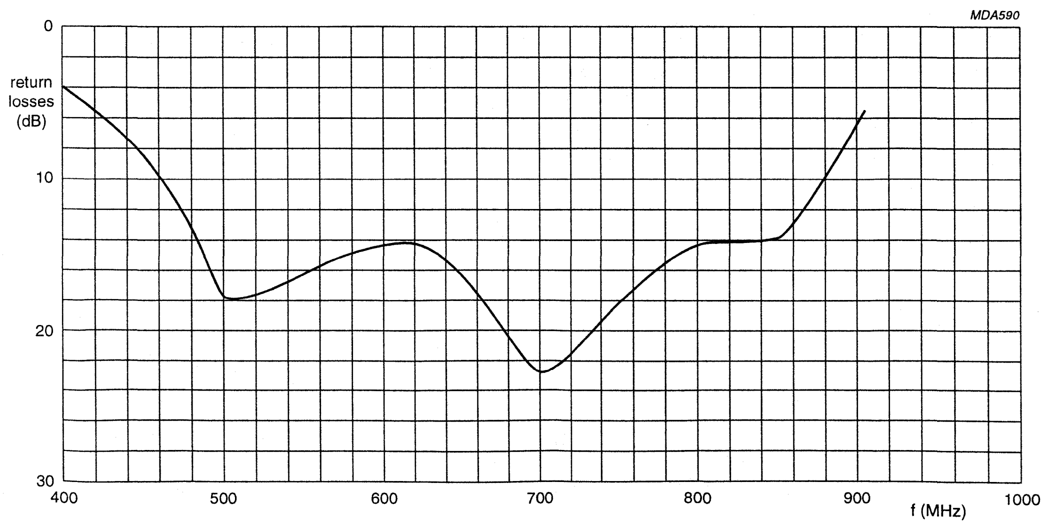


Fig.8 Tuning of the output circuit.

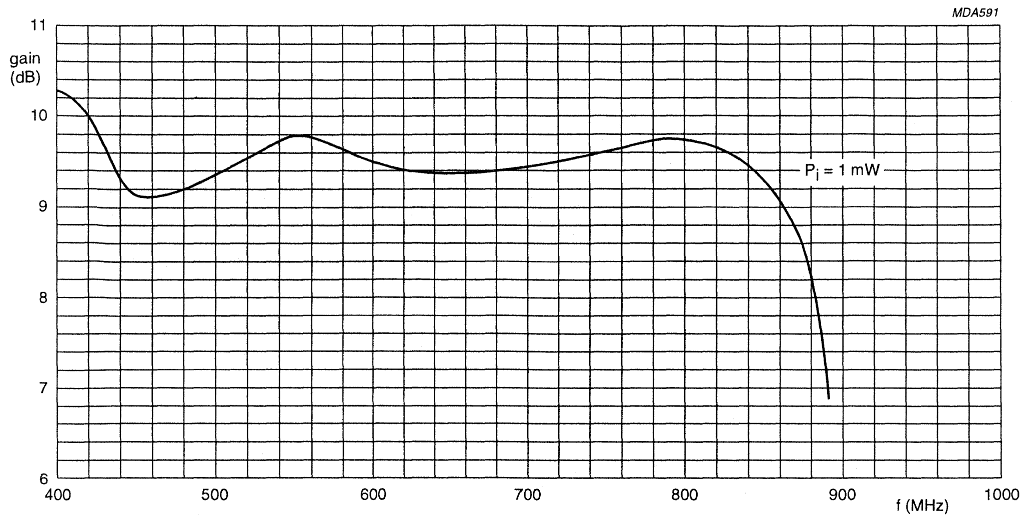


Fig.9 Gain of a BLV57 branch.

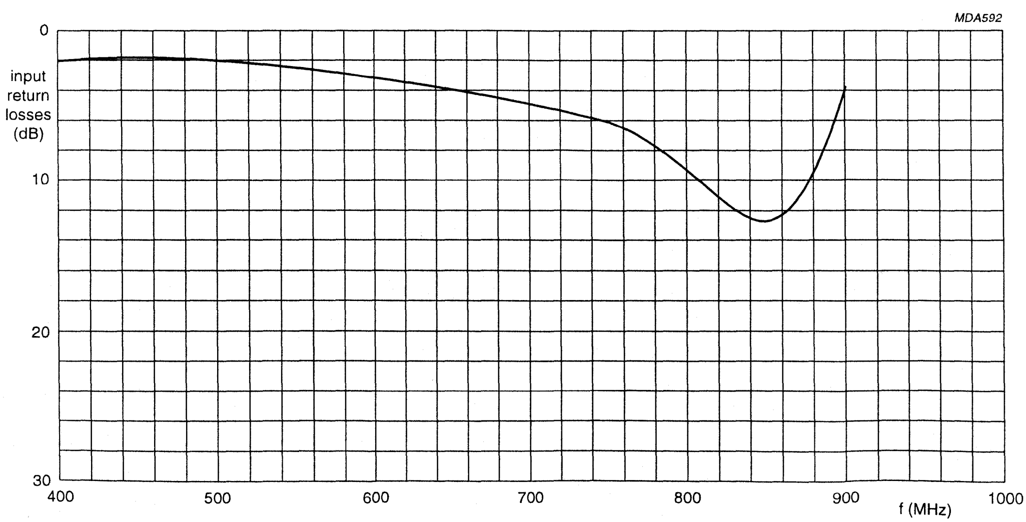


Fig.10 Return losses of a BLV57 branch.

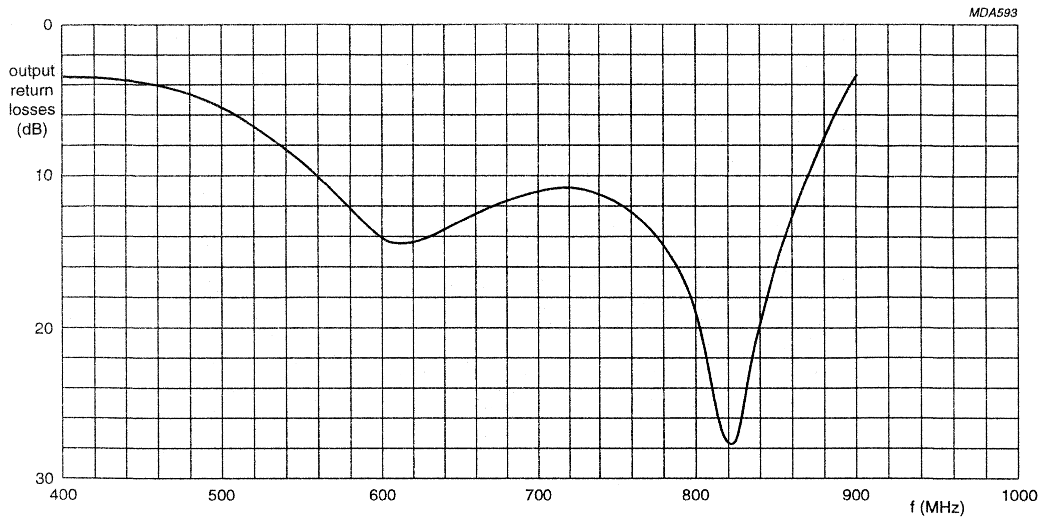


Fig.11 Return losses of a BLV57 branch.

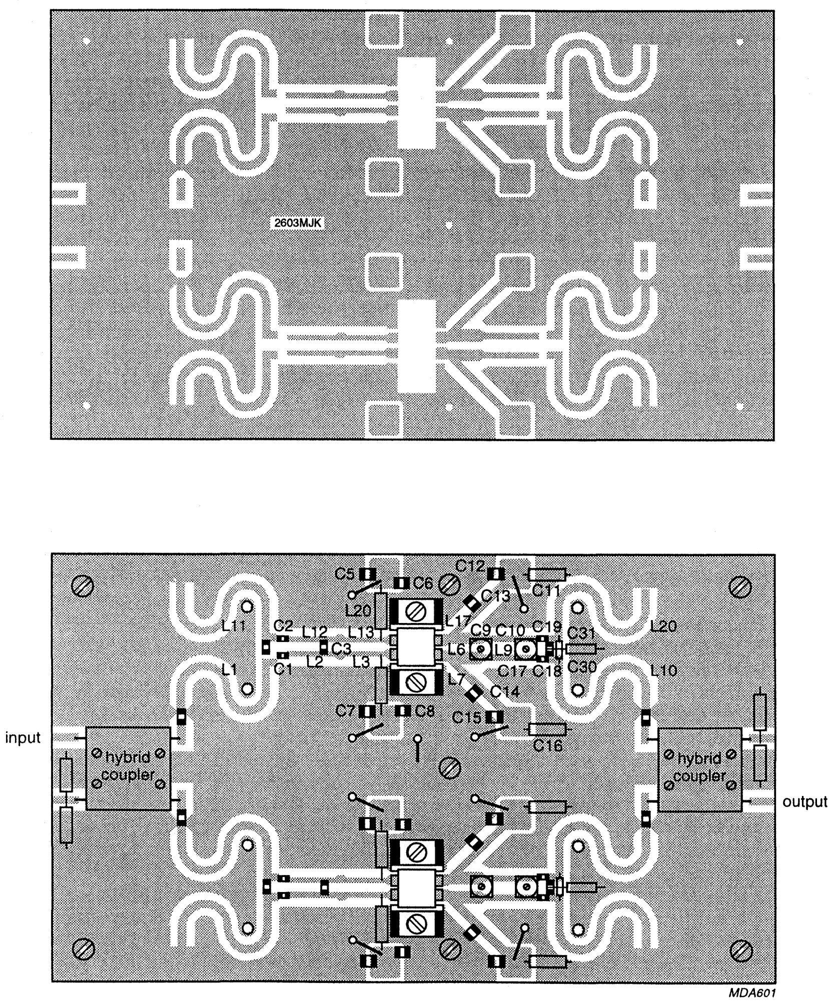


Fig.12 printed-circuit board and lay-out of the BLV57 amplifier.

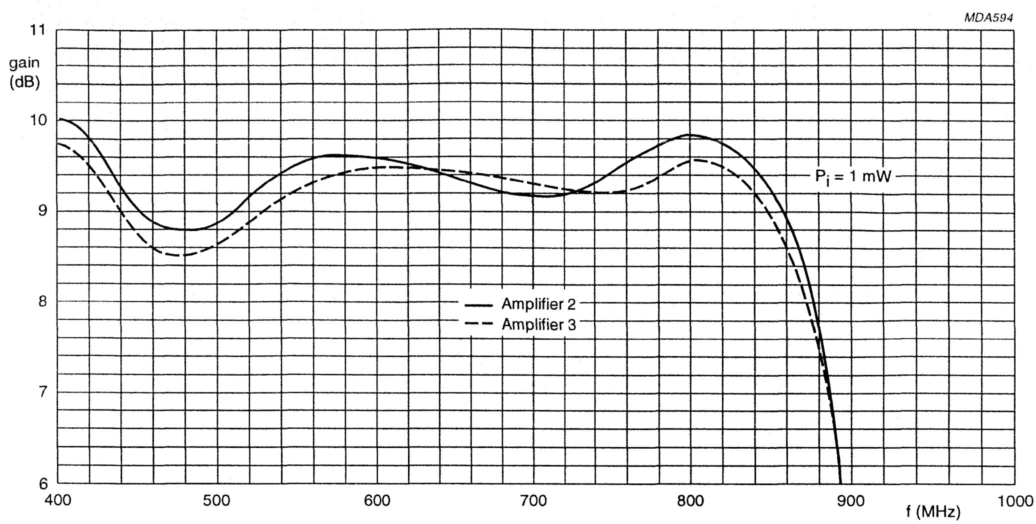


Fig.13 Gain of the BLV57 amplifier.

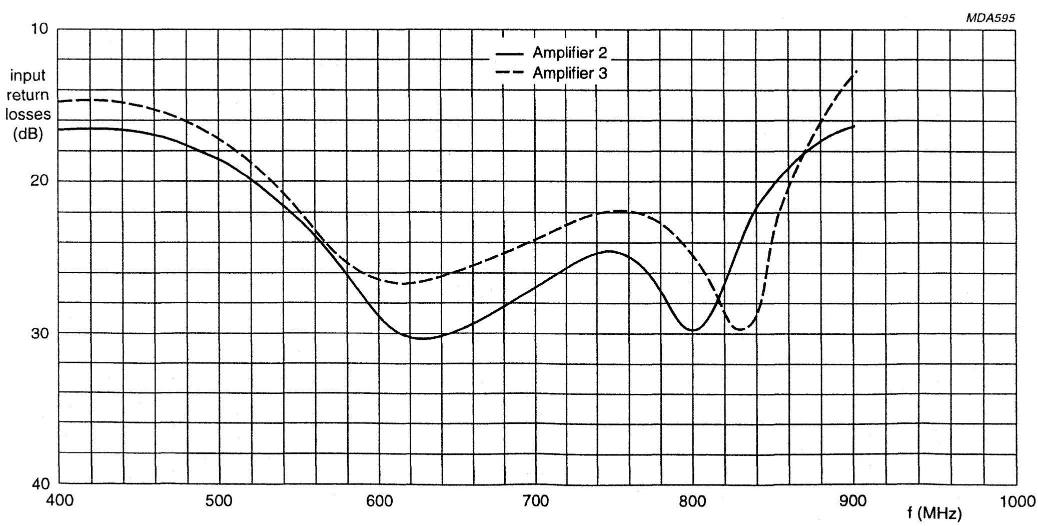


Fig.14 Return losses of the BLV57 amplifier.

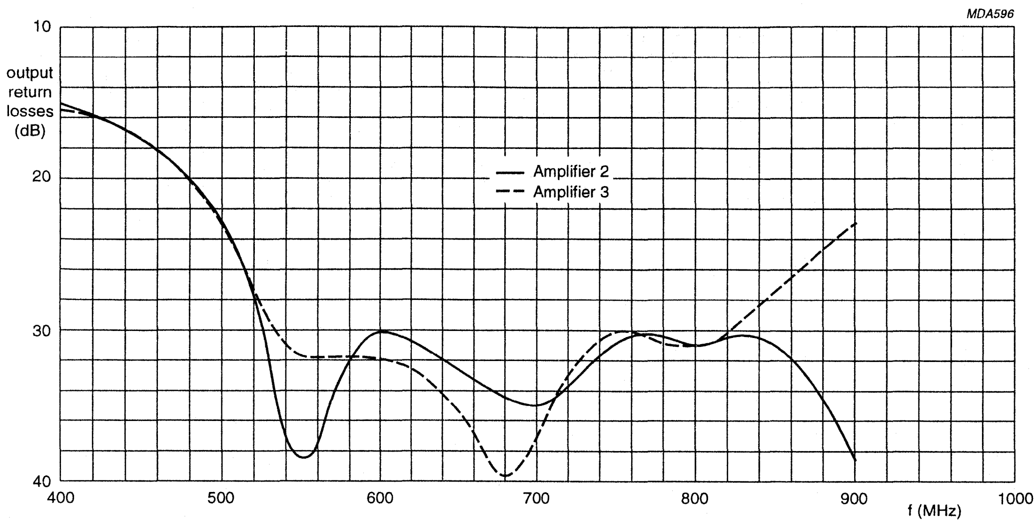


Fig.15 Return losses of the BLV57 amplifier.

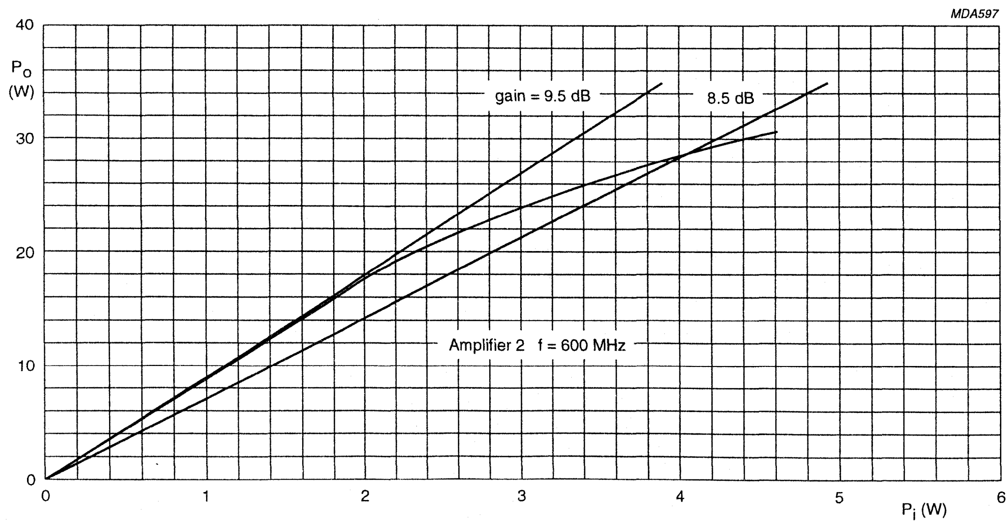


Fig.16 Gain compression of the BLV57 amplifier.

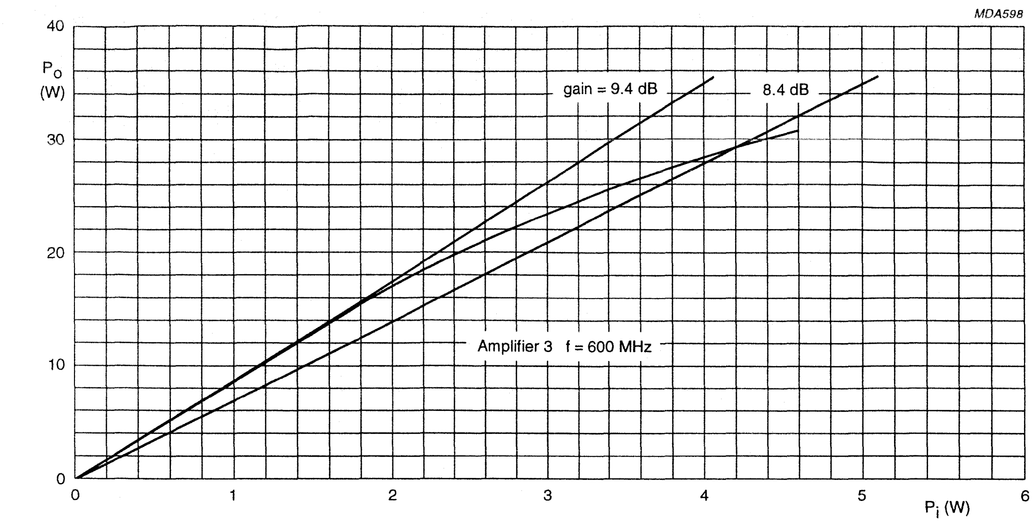


Fig.17 Gain compression of the BLV57 amplifier.

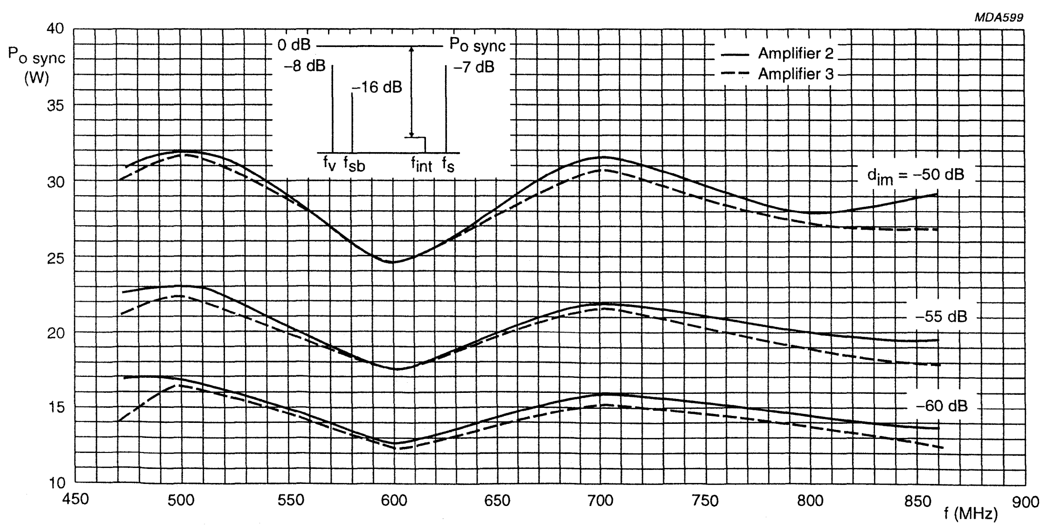


Fig.18 Output power $P_{o\ sync}$ of the BLV57 amplifier.

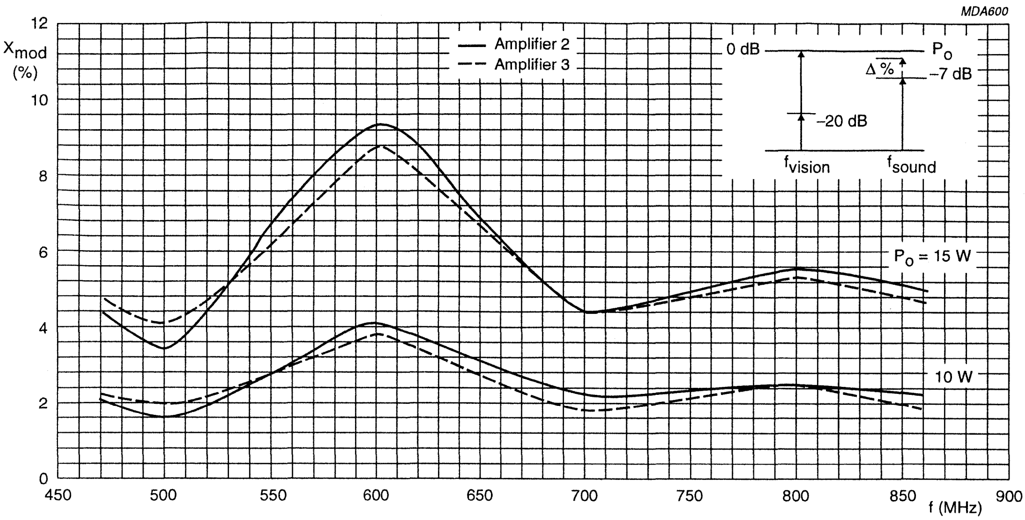


Fig.19 Cross modulation of the BLV57 amplifier.

Construction of the 470 – 860 MHz BLV57 wideband amplifier

Application Note
NCO8201

1 INTRODUCTION

In the application report NCO8101 two amplifiers for band 4/5 with BLV57 transistors have been described. Reactions on this report proved the necessity to give more information about the construction of these amplifiers. This construction has been based on a heatsink with a printed-circuit board at the upper side and the bias circuits and a forced air-cooling at the lower side.

2 PRINTED CIRCUIT BOARD

In the printed-circuit board rectangular holes have been made to mount the BLV57 transistors on the heatsink. For fastening of the printed-circuit board on the heatsink by means of screws, 7 holes of 3.1 mm ∅ and for fastening of the hybrid couplers 8 holes of 2.6 mm ∅ have been made on the indicated places (see Figs 1 and 2). Hereby has been taken into account the use of Anaren hybrid couplers, type 10264 – 3, suited for the frequency range of 500 – 1 000 MHz. Because the 2 bias units have been situated at the lower side of the heatsink, the connections from these units to the circuit take place through the printed-circuit board and the heatsink. For this purpose 9 holes of 2 mm ∅ are necessary (4 collectors, 4 bases and 1 ground). To make a good ground contact between the upper and the lower side of the printed-circuit board the following measures have been taken:

- On 8 spots rivets have been used and soldered at both sides to the metallization of the printed-circuit board. The holes of 2 mm ∅ , needed for these rivets, have been situated as indicated in Figs1 and 2.
- Copper straps with a thickness of 0.2 mm have been soldered at all edges of the printed-circuit board.
- A good emitter to ground contact has been achieved by soldering 8 copper straps from the upper to the lower side of the printed-circuit board on the spots of each emitter lead.
- The input connector and the output connector have been screwed to the heatsink but the ground also has been soldered to the printed-circuit board.

3 HEATSINK

For the BLV57 amplifiers, described in report NCO8101, a blackened heatsink of Seifert Electronic, type KL-117 with a length of 191 mm has been used (see Fig.3). At the lower side forced air-cooling has been applied with a fan trade mark Etri, type 99 XU 01 - 81 with an air displacement of 16 litres per second). By applying this air-cooling the thermal resistance decreased from 0.5 °C/W to 0.2 °C/W.

4 MECHANICAL MACHINING OF THE HEATSINK

The raised edges at the top side of the heatsink have been removed because the printed circuit board has a width of 113 mm (see Fig.3). To fit the heatsink to the printed-circuit board the following machinings have been carried out:

- Rectangular holes of 2.8 mm deep have been mould in the heatsink because the transistor leads have to be soldered on the printed-circuit board. Also it was necessary to make savings of 4 mm wide and 0.6 mm deep at the positions of the straps on the printed-circuit board. The transistors have been fastened with M 2.5 screws in the heatsink (see Fig.4).
- To achieve that the printed-circuit board lays tight to the heatsink also savings have been made in the heatsink on the spots of the 8 rivets through the printed-circuit board.
- For fastening the printed-circuit board on the heatsink on 7 places, holes with M 3 screwthread have been made in the top side of the heatsink, corresponding with indicated holes in the printed-circuit board.
- The two hybrid couplers also have been fastened in the heatsink with screws through the printed-circuit board. Therefore 8 holes have been made with M 2.5 screwthread, corresponding with the printed-circuit board.
- The input and output connectors have been fastened to the heatsink with M 3 screws. The mid contact of each connector makes contact with the printed-circuit board.

5 CONCLUSIONS

With the construction of the BLV57 amplifiers a good thermal resistance (0.2 °C/W) has been achieved by means of a forced air-cooling. Attention has been payed to a good mechanical contact between heatsink and printed circuit board and a good ground contact on the printed-circuit board by means of rivets and straps at the edges and under the emitter leads.

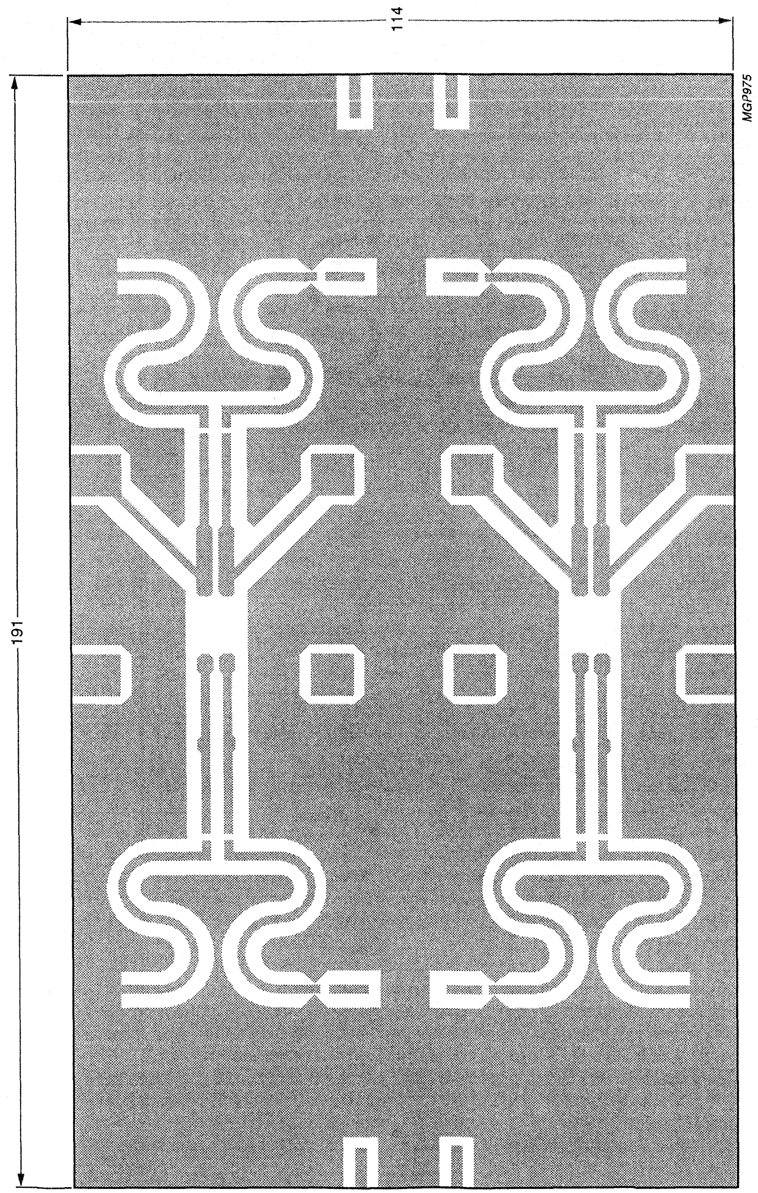


Fig.1 Printed circuit board.

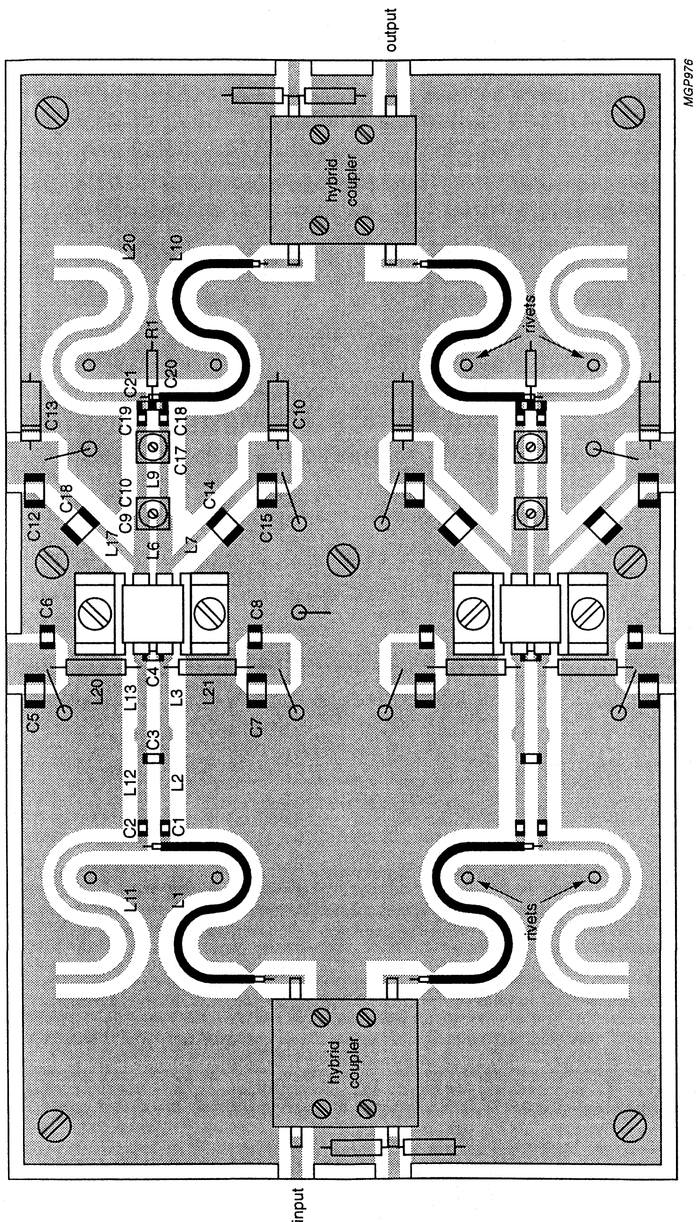


Fig.2 Printed-circuit board.

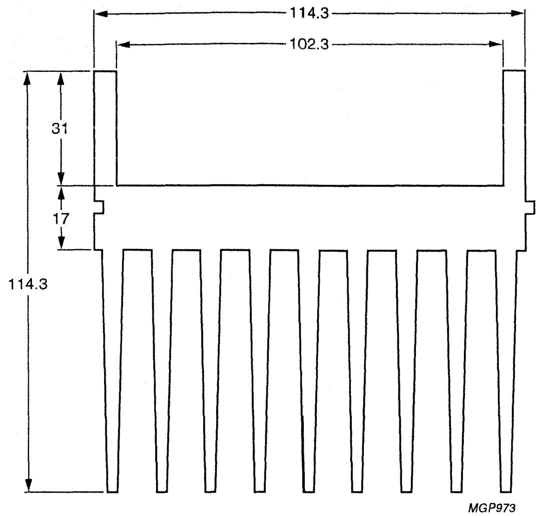


Fig.3 Heatsink.

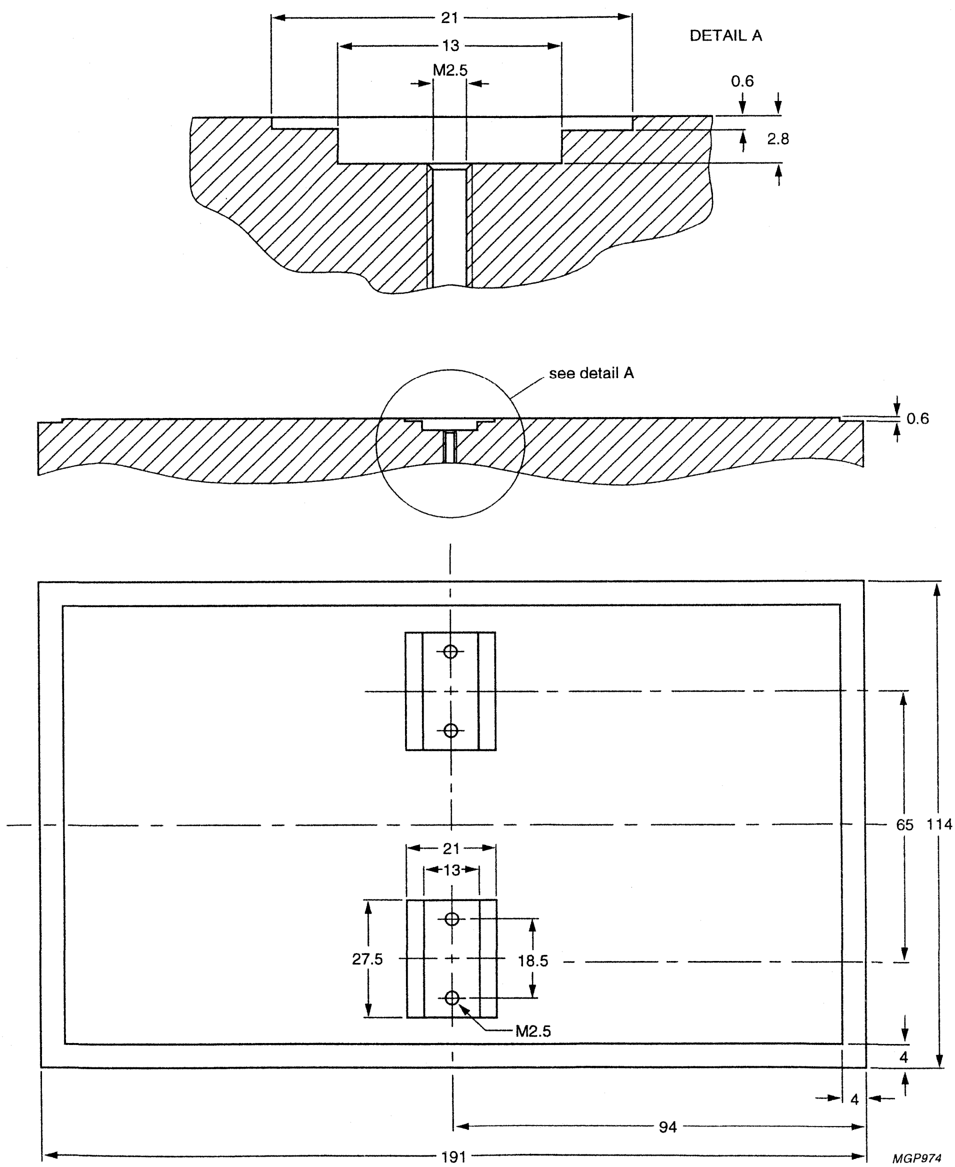


Fig.4 Heatsink savings.

A wide-band class-AB hybrid coupled amplifier (470 – 860 MHz) with two balanced transistors BLV57

Application Note NCO8205

1 SUMMARY

For application in TV transmitters in band 4/5 a wideband linear power amplifier has been designed with two balanced transistors BLV57 in a class AB DC-setting (V_{CE} = 25 V and I_{CZ} = 2 × 100 mA).
A class A amplifier designed around the BLV57 has been described in reports NCO8101 and NCO8201.
The results of the class AB input and output circuit calculations are about similar to the results of the class A application. Therefore the p.c.-board design of the class A-amplifier can be used.
The applied circuit board is a double copper clad PFTE fibre-glass print with an ε_r = 2.74 and a thickness of 1/32 inch.
The heatsink has a forced air cooling.
The main results are given in Table 1.

Table 1

DC-setting	I_{CZ} = 4 × 100 mA, V_{CE} = 25 V
Gain at P_{out} = 5 W	≥6 dB
P_{out} at 1 dB gain compression	≥42.5 W
Efficiency at 1 dB gain compression	≥45%

2 INTRODUCTION

The BLV57 is a balanced transistor in an 8 lead envelope (SOT161) for class A operation in TV-transposers for band 4/5. A class A amplifier, designed around two transistors BLV57, has been described in report NCO8101 and the construction of this amplifier in report NCO8201.
Because there is also a typical class AB specification a wide-band power amplifier has been designed around two transistors BLV57 in class AB.
The quiescent current I_{CZ} = 100 mA per chip and the V_{CE} = 25 V.

3 DESIGN OF THE AMPLIFIER

3.1 General remarks

The schematic line-up of the complete amplifier is given in Fig.1.

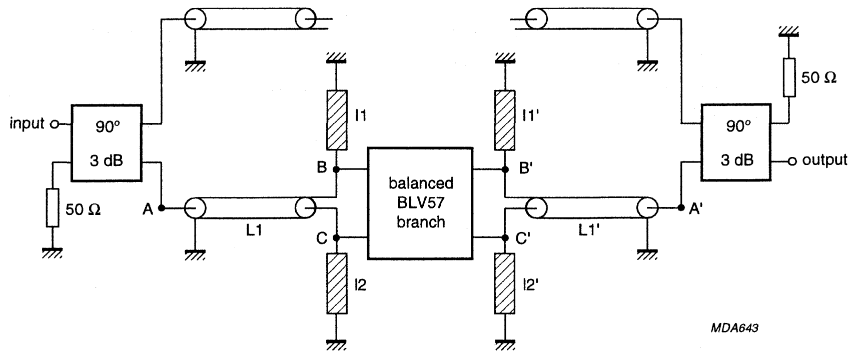


Fig.1 Schematic line-up.

The amplifier consists of two branches, both with a BLV57 transistor, which are coupled by means of a wide-band 3 dB – 90° coaxial hybrid coupler at the input and output.
Each BLV57 has 2 input circuits and 2 output circuits (one for each chip) connected to a coax balun (L_1 and L'_1) which connects the 25 Ω balanced ports B and C to the unbalanced 50 Ω port A.
The phase-shift between B and C is 180°.
The p.c.-board design, the material and the construction of the amplifier is equal to the class A amplifier described in the reports NCO8101 and NCO8201.

3.2 Bias circuit

Each transistor has its own bias unit to obtain a stable DC-setting for class AB operation (see Fig.2). This bias unit enables a stable adjustment of the collector currents of the BLV57 by means of potentiometer R_2.
To follow the temperature variation of the BLV57 the transistor T_1 has been situated on the heatsink near to the HF-transistor for a good thermal contact (see Fig.5).

3.3 Some properties of the BLV57

The optimum DC-setting of the BLV57 for class AB operation is V_{CE} = 25 V and a quiescent current of I_{CZ} = 100 mA for each transistor chip. The typical gain, input and load impedance of a half BLV57 (one chip) are given in Table 2. These figures have been calculated with the aid of a large signal equivalent circuit (P_O = 17.5 W).

Table 2

FREQUENCY (MHz)	GAIN (dB)	INPUT IMPEDANCE (Ω)	OUTPUT IMPEDANCE (Ω)
400	11.95	1.21 + j1.71	10.52 + j4.04
500	10.29	1.24 + j2.53	9.06 + j4.02
600	9.01	1.28 + j3.32	7.70 + j3.63
700	7.99	1.36 + j4.11	6.50 + j2.98
800	7.17	1.49 + j4.93	5.49 + j2.13
900	6.48	1.68 + j5.81	4.67 + j1.17

3.4 Input and output circuit

The calculation of the input and output circuit is the same as described in NCO8101 *"input and output network"*.
The results are about similar to the results of the class A application, making it possible to apply the same p.c.-board design.
The tuning of the output circuit is also as described in report NCO8101. The dummy now consists of a 30 Ω resistance in parallel with an 8.2 pF capacitance.
In Fig.3 the return losses at the output of one branch are given after tuning the output circuit with the help of this dummy.
To achieve a sufficiently flat gain the capacitance of C_3 and C_4 and also the position of C_3 (see Fig.4 and Table 4) can be optimized in a sweep set-up with a constant output power of 5 W. The position of C_4 and C_5 is close to the ceramic cap of the BLV57.

3.5 Hybrid coupled amplifier

As mentioned in Chapter 4 of NCO8101 the two branches are coupled by means of 3 dB – 90° hybrid couplers. Figure 5 gives the p.c.-board of the complete amplifier and the lay-out.

4 MEASURED PERFORMANCE

4.1 Gain and return losses

Figures 6 and 7 show the gain and input return losses as a function of the frequency at a constant output power P_O = 5 W. The gain varies from 6 to 6.9 dB. The input return losses are at least 12 dB.
Figures 10 and 11 show the gain versus output power at the frequencies 500 and 800 MHz. The increase of gain at low power level can be reduced at the cost of the average gain level by decreasing the quiescent current.

4.2 Output power

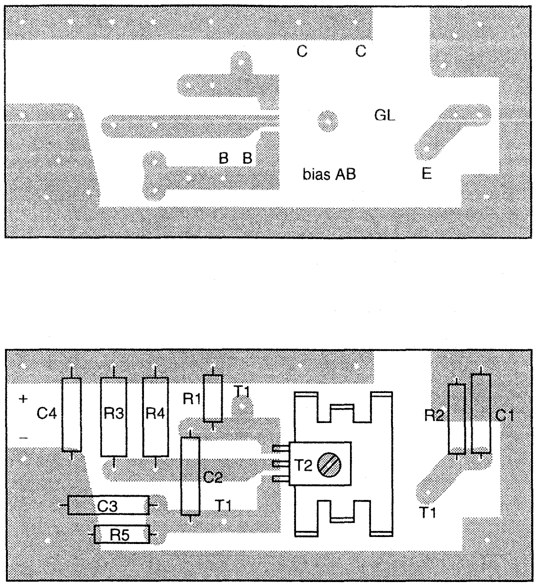
Figures 8 and 9 show the output power and efficiency as a function of the frequency at 1 dB gain compression. The output power is at least 42.5 W and above 530 MHz between 50 and 60 W. The average efficiency at 1 dB gain compression is 50%.

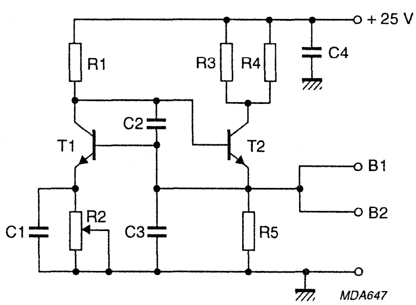
5 CONCLUSION

This report shows that it is possible to operate the class A transistor BLV57 with a class AB DC-setting in a hybrid coupled wideband amplifier (470 to 860 MHz) with good performances.
The main properties of the amplifier are given in Table 3.

Table 3

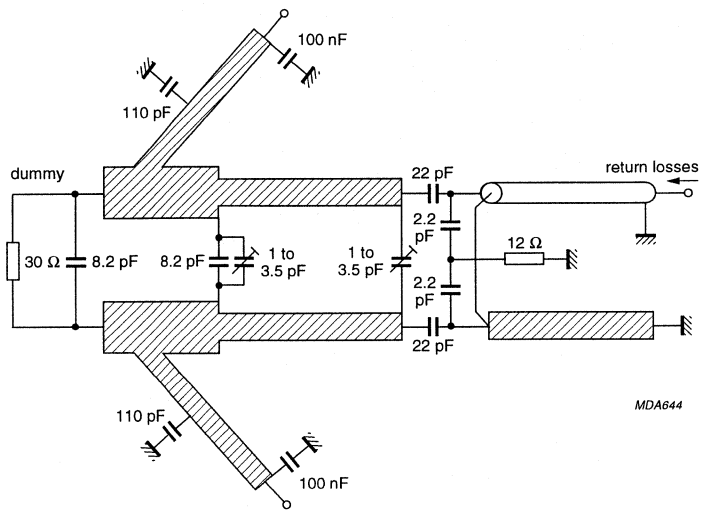
BLV57 BAND 4/5 AMPLIFIER	
DC-setting	$I_{CZ} = 4 \times 100$ mA, $V_{CE} = 25$ V
Gain at $P_{out} = 5$ W	≥6 dB
P_{out} at 1 dB gain compression	≥42.5 W
Efficiency at 1 dB gain compression	≥45%





$C_1 = C_2 = C_3 = C_4$ = 150 nF, metallised film capacitor, cat. no. 2222 352 45154.
R_1 = 1500 Ω, CR 25 type, cat. no. 2322 211 13152.
R_2 = 10 Ω, cermet potentiometer, cat. no. 2122 350 00056.
$R_3 = R_4$ 120 Ω, CR 52 type, cat. no. 2322 213 13121.
R_5 = 150 Ω, CR 25 type, cat. no. 2322 211 13151.
$T_1 = T_2$ BD 139.

Fig.2 Bias circuit and lay-out.



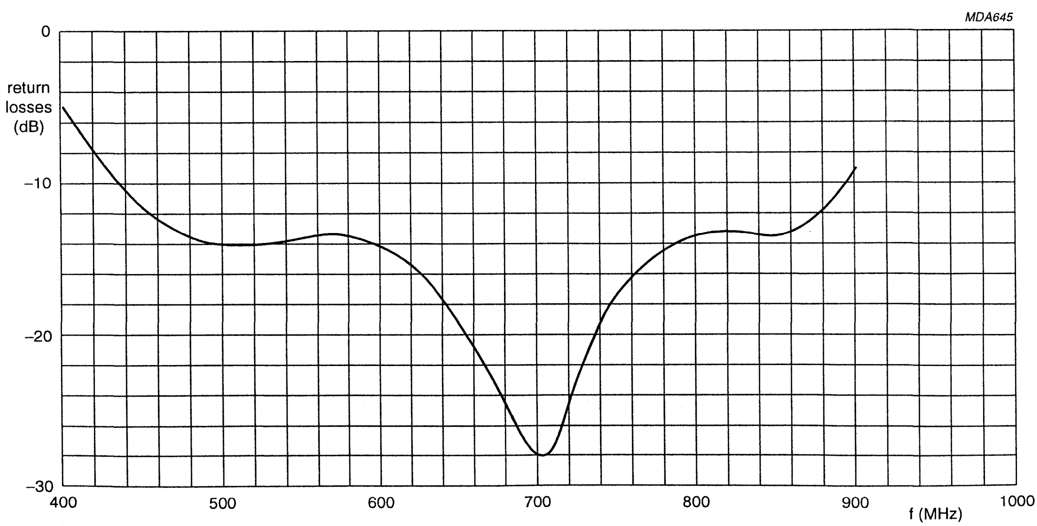


Fig.3 Tuning of the output circuit.

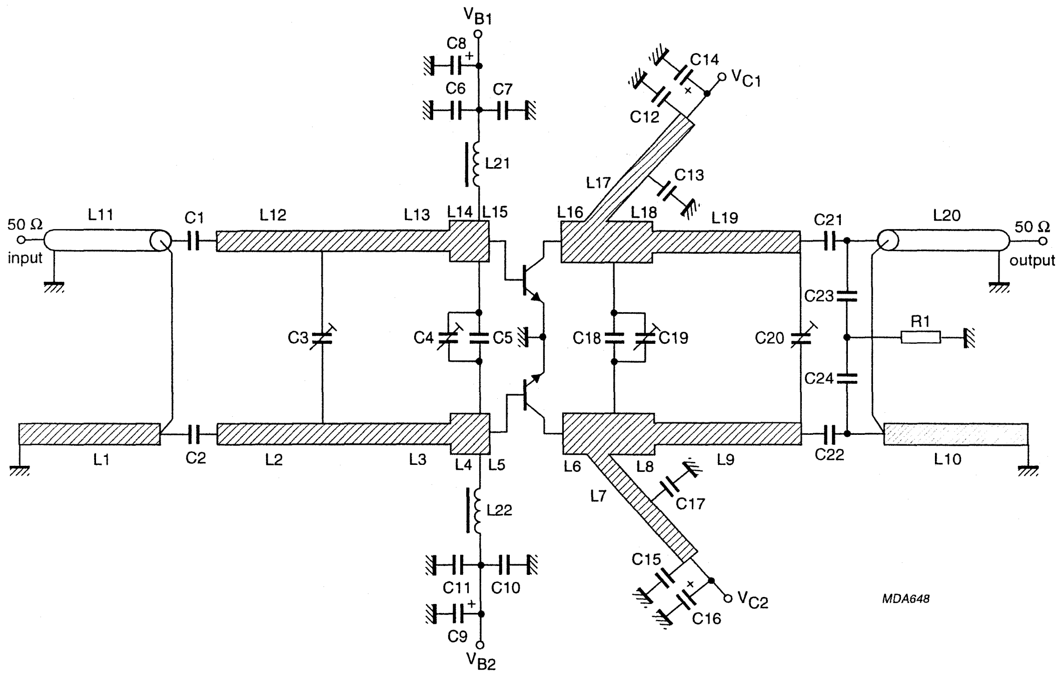


Fig.4 Circuit of one BLV57 branch.

Table 4 List of components BLV57 class AB (one branch)

$C_1 = C_2 = 12$ pF	chip capacitor, Philips NPO, cat.no. 2222 851 13129
$C_3 = C_4 = C_{19} = C_{20} = 1 - 3.5$ pF	film dielectric trimmer, Philips cat.no. 2222809 05001
$C_5 = C_{18} = 8.2$ pF	chip capacitor, ATC, 8R2J
$C_6 = C_{11} = C_{12} = C_{15} = 100$ nF	chip capacitor, Philips NPO, cat.no. 2222855 48104
$C_7 = C_{10} = 100$ pF	chip capacitor, Philips NPO, cat.no. 2222852 13101
$C_8 = C_9 = C_{14} = C_{16} = 6.8$ µF, (40 V)	electrolytic capacitor, Philips, cat.no. 2222 030 87688
$C_{13} = C_{17} = 110$ pF	chip capacitor, ATC, 111J
$C_{21} = C_{22} = 22$ pF	chip capacitor, Philips NPO, cat.no. 2222 851 13229
$C_{23} = C_{24} = 2.2$ pF	chip capacitor, Johanson, no. 500 R, 15 N, 2R2BA
L_1 = stripline	($Z_C = 50\ \Omega$), 49×2 mm
$L_2 = L_{12}$ = stripline	($Z_C = 57\ \Omega$), 14.5×1.5 mm
$L_3 = L_4$ = stripline	($Z_C = 57\ \Omega$), 12.8×1.5 mm
$L_4 = L_{14}$ = stripline	($Z_C = 36\ \Omega$), 2×3 mm
$L_5 = L_{15}$ = stripline	($Z_C = 36\ \Omega$), 1×3 mm
$L_6 = L_{16}$ = stripline	($Z_C = 36\ \Omega$), 3×3 mm
$L_7 = L_{17}$ = stripline	($Z_C = 48\ \Omega$), 17.7×2 mm
$L_8 = L_{18}$ = stripline	($Z_C = 36\ \Omega$), 8.8×3 mm
$L_9 = L_{19}$ = stripline	($Z_C = 57\ \Omega$), 15.2×1.5 mm
L_{10} = stripline	($Z_C = 50\ \Omega$), 46×2 mm
L_{11} = 49 mm semi-rigid coax, 2.2 mm ∅, $Z_C = 50\ \Omega$, PTFE dielectric, soldered on 2 mm stripline	
L_{20} = 46 mm semi-rigid coax, 2.2 mm ∅, $Z_C = 50\ \Omega$, PTFE dielectric, soldered on 2 mm stripline	
$L_{21} = L_{22} = 0.1$ µH	microchoke, cat.no. 2322 057 01071
$R = 12\ \Omega$	CR 25 type cat.no. 2322 211 13129

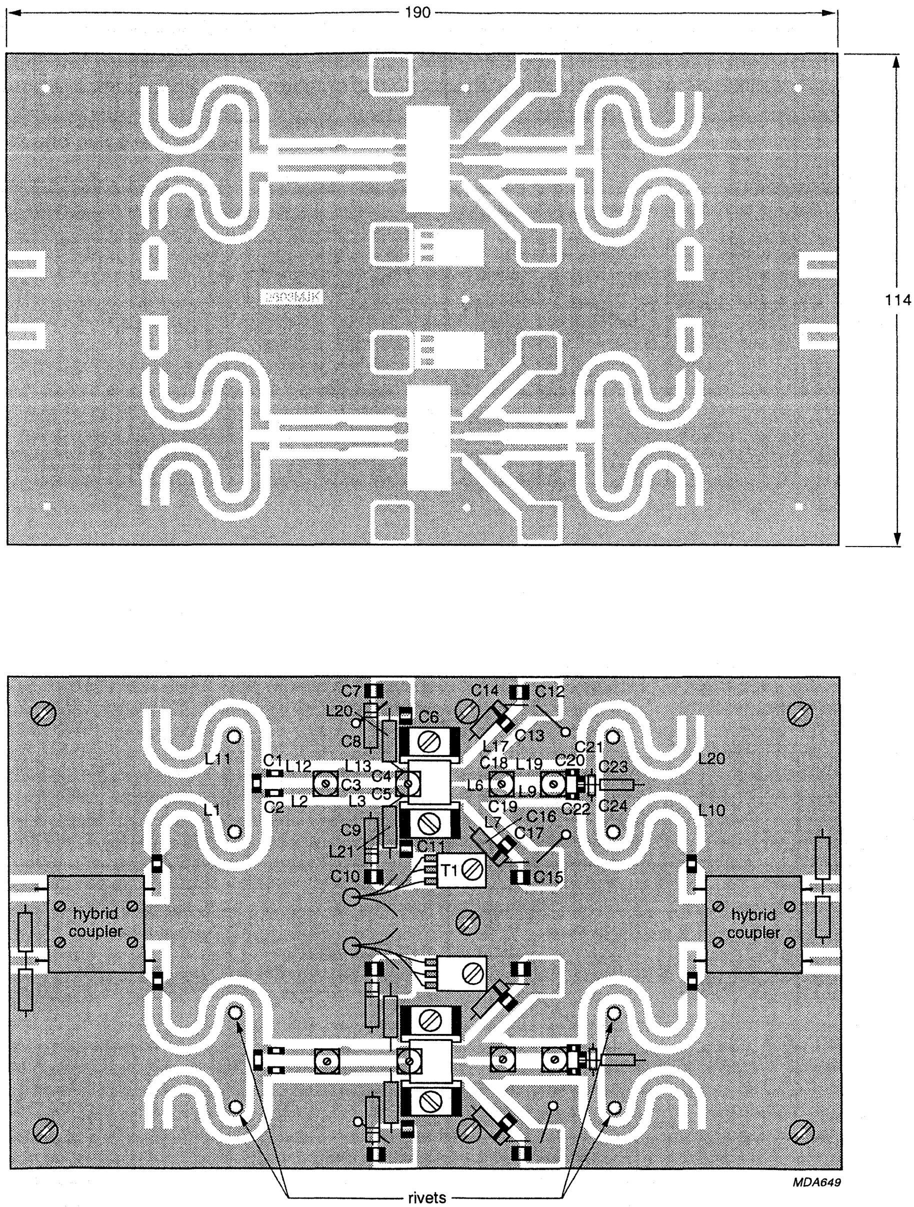


Fig.5 Lay-out and PC-board of the BLV57 amplifier.

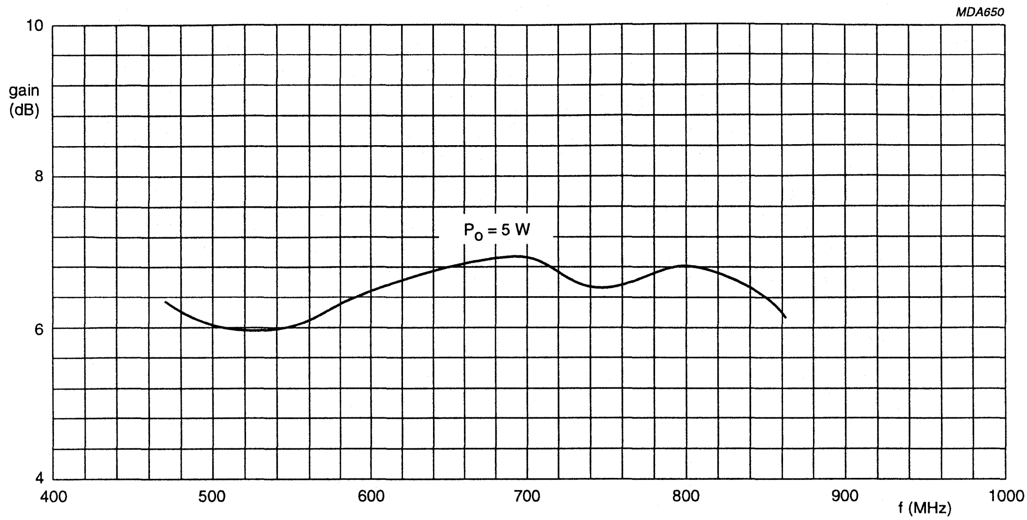


Fig.6 Gain versus frequency.

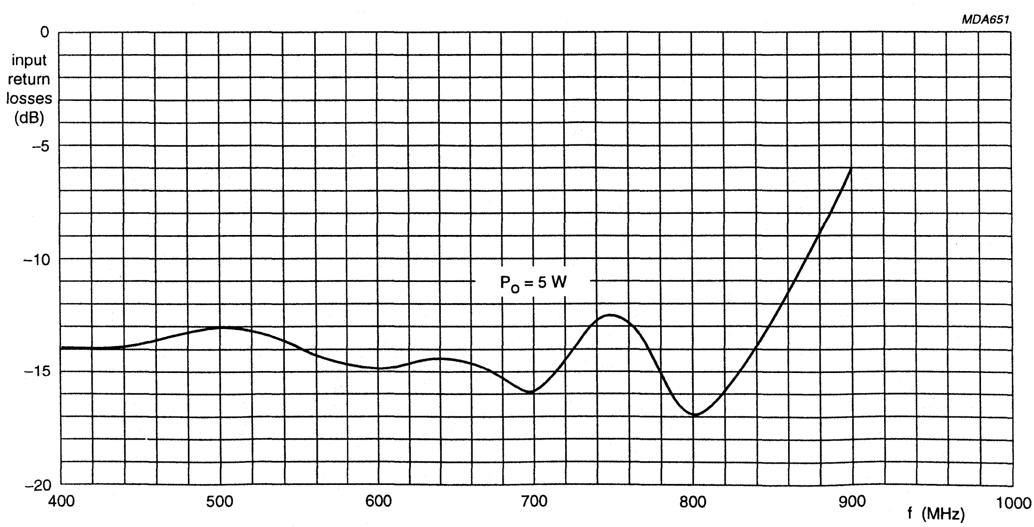


Fig.7 Return losses versus frequency.

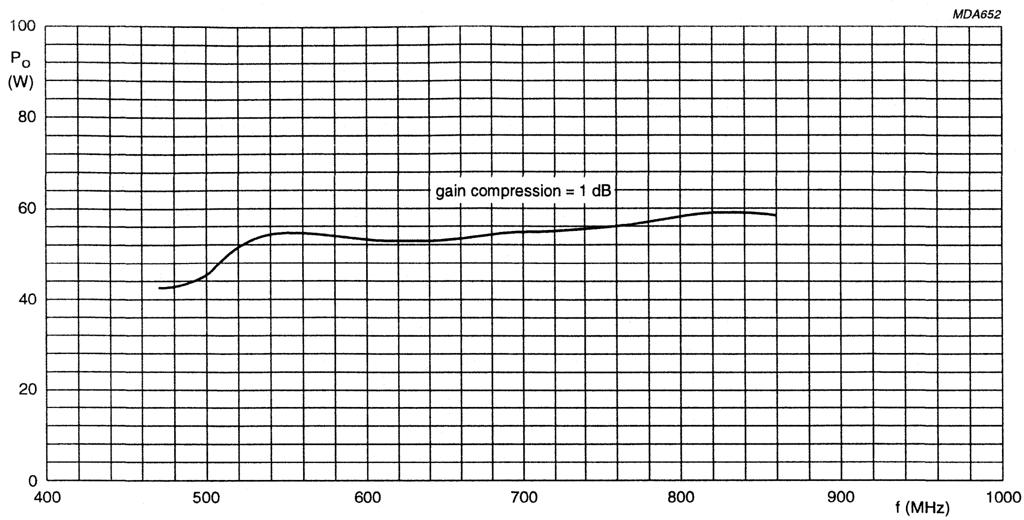


Fig.8 Output power versus frequency.

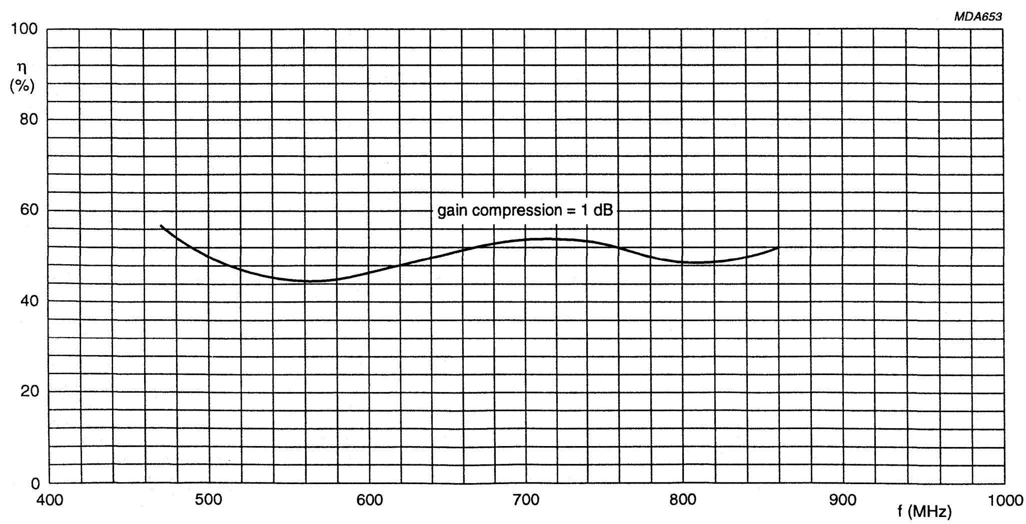


Fig.9 Efficiency versus frequency.

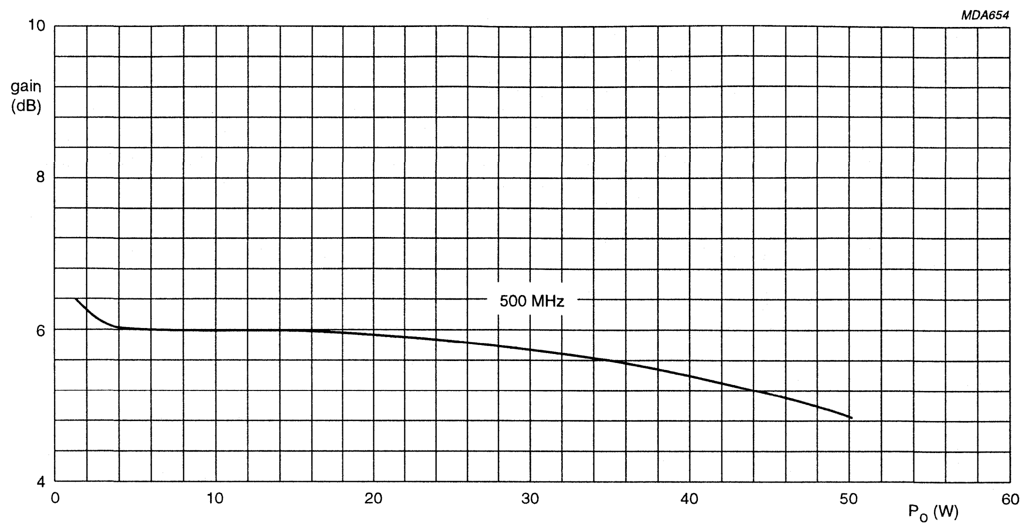


Fig.10 Gain versus output power.

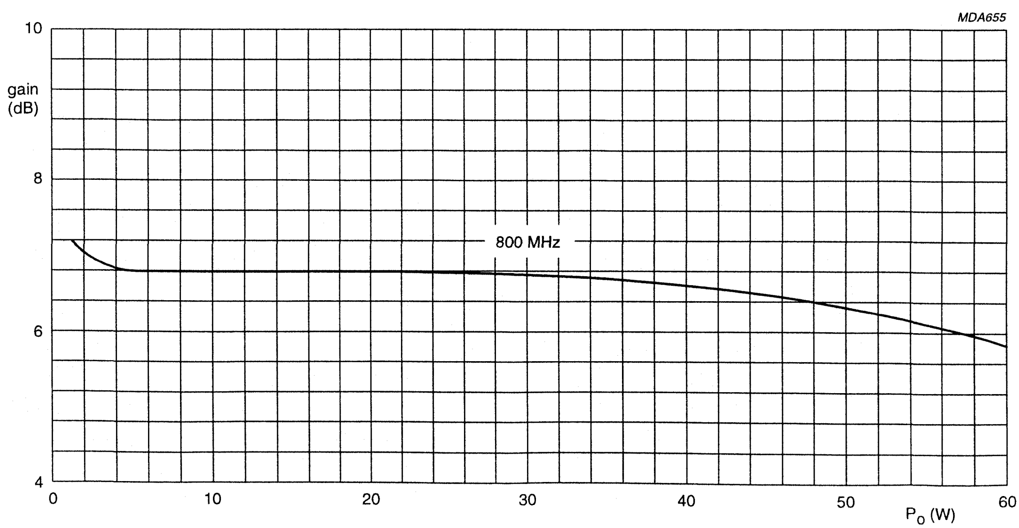


Fig.11 Gain versus output power.

BASE STATION

APPLICATION NOTES

5 W Class-AB Amplifier with the BLV904 for 935 – 960 MHz

Application Note AN98019

INTRODUCTION

This application note contains information on a 5 W class-AB amplifier based on the SMD transistor BLV904. The amplifier described can be used for driver stages in cellular radio base stations in the GSM band 935 – 960 MHz. The next chapters contain information on the transistor, the amplifier construction and the typical RF performance obtained.

TRANSISTOR BACKGROUND

The BLV904 is an NPN bipolar RF power transistor in an 8-lead SMD package called SOT409. The package contains an Aluminium Nitride (AlN) substrate to enhance its thermal performance. The bottom surface is fully metallized to enable reflow soldering of the transistor to the printed-circuit board. All leads are isolatad from the bottom surface and a ceramic lid is used to cover the transistor. The BLV904 features internal input matching for easy wide band matching over the 935 – 960 MHz frequency band. When operated from a 26 V supply in class-AB mode the transistor has a minimum power gain of 13 dB and a minimum collector efficiency of 50%. Two tone IMD performance is typically below –30 dBc.

AMPLIFIER DESCRIPTION

Figure 1 shows the schematic diagram of the amplifier. The matching circuits applied are fixed tuned two-stage lowpass networks using striplines and multilayer chip capacitors. Conventional bias decoupling networks are applied with improved decoupling for two-tone operation. The list of components and stripline dimensions is given inTable 2.
Figure 2 contains the printed-circuit board layout and components topology of the amplifier. The printed-circuit board contains a footprint of solder pads for collector and base lead interconnect and a thermal pad with vias to provide a low thermal resistance path to the package. Pads with vias for RF grounding of the emitter leads are integrated with the thermal pad. All SMD components were reflow soldered to the printed-circuit board. The printed-circuit board was soldered to a heatsink in the same process step. More details on the mounting considerations for the SOT409B can be found in application note AN98017.
The pc-board material used is Rogers RT/Duroid 6010 with a dielectric constant of 10.2 and a thickness of 0.64 mm.

AMPLIFIER PERFORMANCE

The amplifiers performance was measured at V_{CE} = 26 V and I_{cq} = 15 mA. The heatsink temperature was held at 25 °C during the measurement. A summary of the performance is given in the Table 1.

Table 1

	UNIT	SINGLE-TONE	TWO-TONE
Frequency band	MHz	935 – 960	935 – 960
Load power	W	5	5 (PEP)
Power gain	dB	15.5	15.5
Power gain flatness	dB	1.9	–
Collector efficiency	%	53	40
Intermodulation distortion	dBc	–	–30 up to 5 W PEP

Single-tone performance curves are presented in:
Figure 3; Load power (Pl) versus drive power (Pd);
Figure 4; Power gain (Gp) and collector efficiency (Eff) versus load power (Pl).

Two-tone performance curves are presented in:
Figure 5; Load power (Pl-PEP) versus drive power (Pd-PEP)
Figure 6; Power gain (Gp) and collector efficiency (Eff) versus load power (Pl-PEP)
Figure 7; Intermodulation distortion (d3) as function of load power (Pl-PEP)

CONCLUSION

An AlN based surface mountable transistor BLV904 has been used to develop an amplifier for driver application in GSM base stations. Biased at 26 V and 15 mA this amplifier has shown a 5 W CW power output capability with a gain of 15 dB and a collector efficiency 53%. For two-tone operation the IMD performance is better than –31 dBc up to 5 W PEP. In addition the IMD over a wide dynamic range can be further optimized by adding a base series resistor of a few Ω combined with a good selection of I_{cq} as described in application note AN98026.

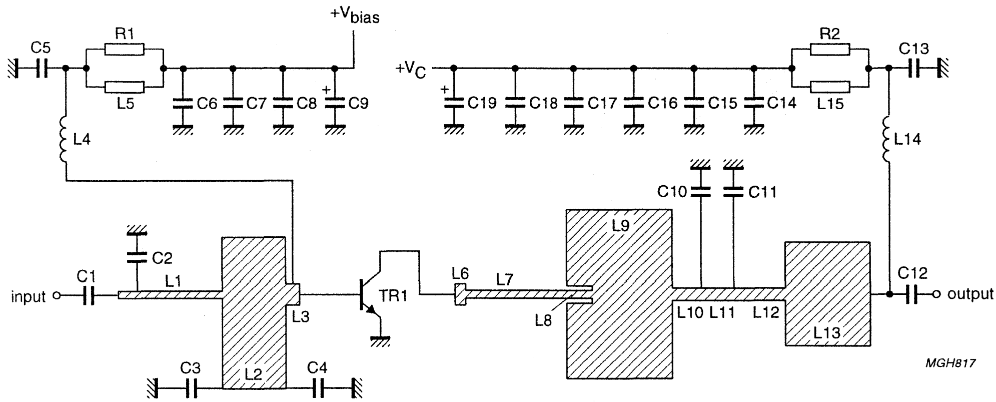


Fig.1 Schematic diagram.

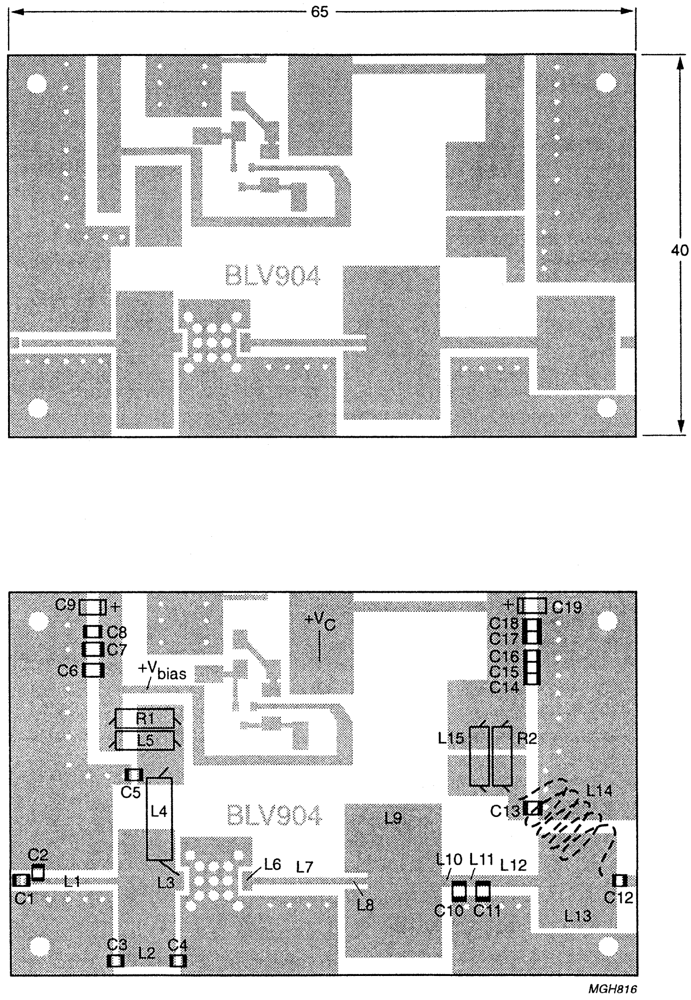


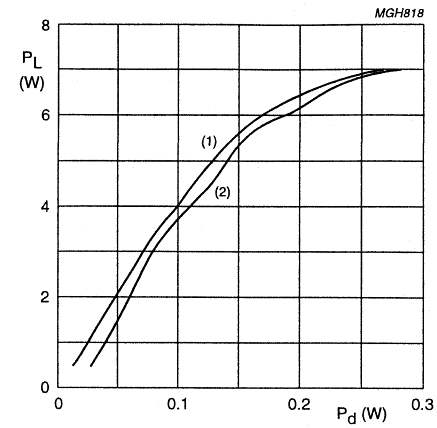
Fig.2 Printed-Circuit board and layout amplifier.

Table 2

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C12	multilayer ceramic chip capacitor; note 1	24 pF		
C2	multilayer ceramic chip capacitor; note 1	3.3 pF		
C3	multilayer ceramic chip capacitor; note 1	2.2 pF		
C4	multilayter ceramic chip capacitor; note 1	1.6 pF		
C5, C6, C13, C18	multilayer ceramic chip capacitor; note 2	200 pF		
C7, C17	multilayer ceramic chip capacitor; note 2	100 pF		
C8, C14, C15, C16	multilayer ceramic chip capacitor	100 nF		2222 581 16641
C9, C19	tantal SMD capacitor	35 V, 10 μF		
C10	multilayer ceramic chip capacitor; note 1	1.8 pF		
C11	multilayer ceramic chip capacitor; note 1	13 pF		
L1	stripline; note 3	50 Ω	8.2 × 0.65 mm	
L2	stripline; note 3	4.9 Ω	6 × 14 mm	
L3, L6	stripline; note 3	24.5 Ω	1.5 × 2 mm	
L4	RF-choke	0.22 μH		
L5, L15	grade 4S2 ferroxcube chip-bead			4330 030 36301
L7	stripline; note 3	46.3 Ω	12.22 × 0.7 mm	
L8	stripline: L8 not connected over total length, only 7.58 mm. connected; note 3	4.3 Ω	7.58 × 16.1 mm	
L9	stripline; note 3	4.3 Ω	10 × 16.1 mm	
L10	stripline; note 3	34.3 Ω	1.9 × 1.2 mm	
L11	stripline; note 3	34.3 Ω	3.2 × 1.2 mm	
L12	stripline; note 3	34.3 Ω	4.8 × 1.2 mm	
L13	stripline; note 3	6.7 Ω	8 × 9.9 mm	
L14	5 turns enamelled 1 mm copper wire			
R1	metal film resistor	100 Ω; 0.4 W		
T1	RF transistor	BLV904		

Notes

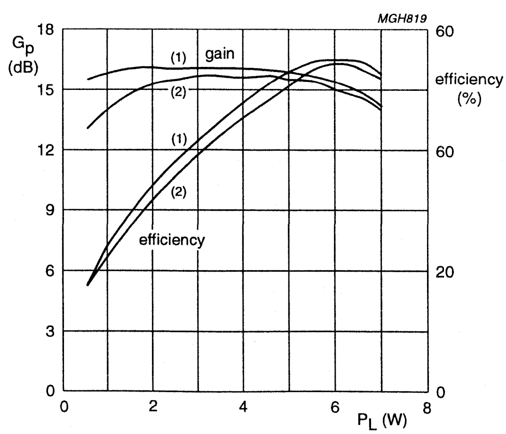
1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. The striplines are on double copper-clad printed-circuit board RT/Duroid 6010 (ε_r = 10.2); thickness 0.64 mm.



(1) f = 960 MHz.
(2) f = 935 MHz.

Pd(W); Class AB: V_{ce} = 26 V; I_{cq} = 15 mA; 5 W loadline, f = 960 MHz.

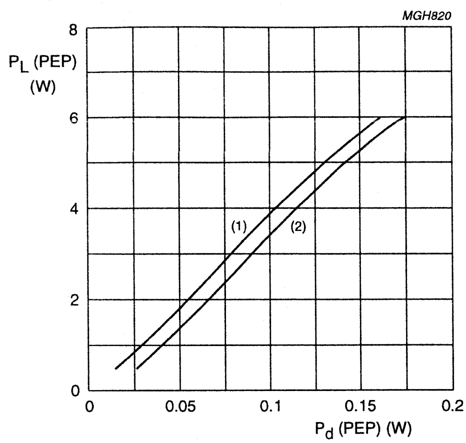
Fig.3 PL = f (Pd).



(1) f = 960 MHz.
(2) f = 935 MHz.

PL(W); Class AB: V_{ce} = 26 V; I_{cq} = 15 mA; 5 W loadline, f = 960 MHz.

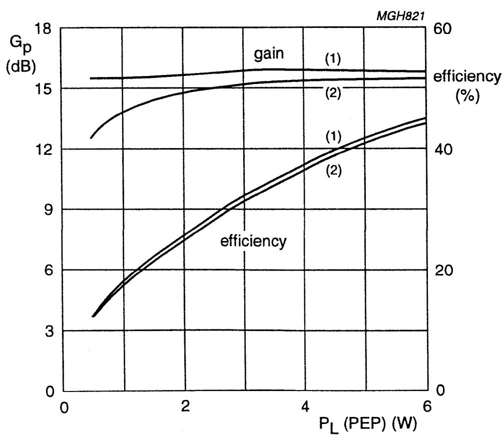
Fig.4 Gp and Eff. = f(PL).



(1) f = 960 MHz.
(2) f = 935 MHz.

Pd-PEP(W); Class AB: V_{ce} = 26 V; I_{cq} = 15 mA; 5 W PEP loadline; delta-f = 0.1 MHz, f1 = 960 MHz, f2 = 960.1 MHz.

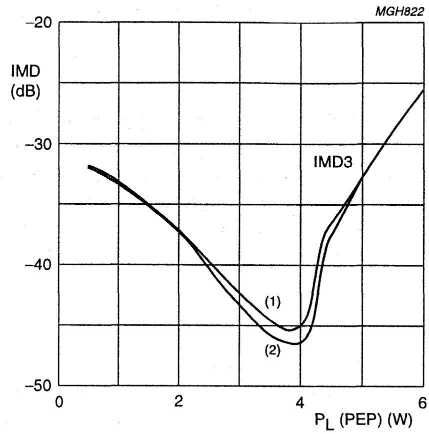
Fig.5 PL-PEP = f (Pd).



(1) f = 960 MHz.
(2) f = 935 MHz.

PL-PEP(W); Class AB: V_{ce} = 26 V; I_{cq} = 15 mA; 5 W PEP loadline; delta-f = 0.1 MHz, f2 = 960.1 MHz.

Fig.6 Gp and Eff. = f (PL-PEP).



(1) f = 960 MHz.
(2) f = 935 MHz.

PL-PEP(W); Class AB: V_{ce} = 26 V; I_{cq} = 15 mA; 5 W PEP loadline; delta-f = 0.1 MHz, f1 = 960 MHz, f2 = 960.1 MHz.

Fig.7 IMD = f (PL-PEP).

9 W Linear Class-AB Amplifier with the BLV909 for 935 – 960 MHz

Application Note
AN98020

1 INTRODUCTION

This application note contains information on a 9 W class-AB amplifier based on the SMD transistor BLV909.
The amplifier described can be used for driver stages in cellular radio base stations in GSM band 935 – 960 MHz. The next sections contain information on the transistor, the amplifier construction and the typical RF performance obtained.

2 TRANSISTOR BACKGROUND

The BLV909 is an NPN bipolar RF power transistor in an 8-lead SMD package called SOT409. The package contains an Aluminium Nitride (AlN) substrate to enhance its thermal performance. The bottom surface to is fully metallized to enable reflow soldering of the transistor to the PCB. All leads are isolated from the bottom surface and a ceramic lid is used to cover the transistor. The BLV909 features internal input matching for easy wide band matching over the 935 – 960 MHz frequency band. When operated from a 26 V supply in class-AB mode the transistor has a minimum power gain of 9.5 dB and a minimum collector efficiency of 50%. Two tone IMD performance is typically –30 dBc.

3 AMPLIFIER BACKGROUND

Figure 1 shows the schematic diagram of the amplifier. The matching circuits applied are fixed tuned two-stage lowpass networks using striplines and multilayer chip capacitors. Conventional bias decoupling networks are applied with improved decoupling for two-tone operation. The list of components and stripline dimensions is given in Tabel 2.
Figure 2 contains the printed-circuit board lay-out and components topology of the amplifier. The printed-circuit board contains a footprint of solder pads for collector and base lead interconnect and a thermal pad with vias to provide a low thermal resistance path to the package. Pads with vias for RF grounding of the emitter leads are intergrated with the thermal pad. All SMD components were reflow soldered to the printed-circuit board. The printed-circuit board was soldered to a heatsink in the same process step. More details on the mounting considerations for the SOT409B can be found in application note AN98017. The printed-circuit board material used is Rogers RT/Duroid 6010 with a dielectric constant of 10.2 and thickness of 0.64 mm.

4 AMPLIFIER PERFORMANCE

The amplifiers performance was measured at V_{ce} = 26 V and I_{cq} = 25 mA. The heatsink temperature was held at 25 °C during the measurement. A summary of the performance is given in Table 1.

Table 1

	UNIT	SINGLE-TONE	TWO-TONE
Frequency band	MHz	935 – 960	935 – 960
Load power	W	9	9 (PEP)
Power gain	dB	11	11.5
Power gain flatness	dB	<0.5	–
Collector efficiency	%	50	40
Intermodulation distortion	dBc	–	–32 @ 9 W PEP

Single-tone performance curcves are presented in:
Figure 3; Load power (P1) versus drive power (Pd).
Figure 4; Power gain (Gp) and collector efficiency (Eff) versus load power (P1).

2-tone performance curves are presented in:
Figure 5; Load power (P1-PEP) versus drive power (Pd-PEP)
Figure 6; Power gain (Gp) and collector efficiency (Eff) versus load power (P1-PEP)
Figure 7; Intermodulation distortion (d3) as function of load power (P1-PEP).

5 CONCLUSIONS

An AIN based surface mountable transistor BLV909 has been used to develop an amplifier for driver application in GSM base stations. Biased at 26 V and 25 mA this amplifier has shown a 9 W CW power output capability with a gain of 11 dB and a collector efficiency 50%. For 2-tone operation the IMD performance is better than –32 dBc at 9 W PEP. In addition the IMD over a wide dynamic range can be further optimized by adding a base series resistor of a few ohms combined with a good selection of Icq as described in application note AN98026.

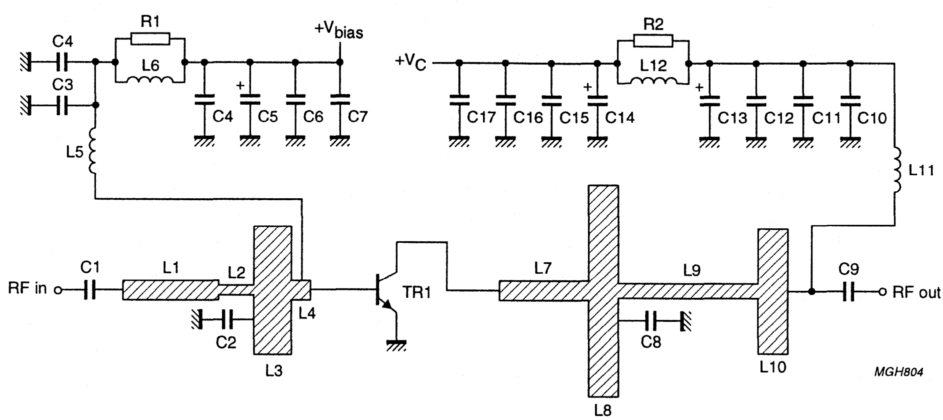


Fig.1 Circuit diagram.

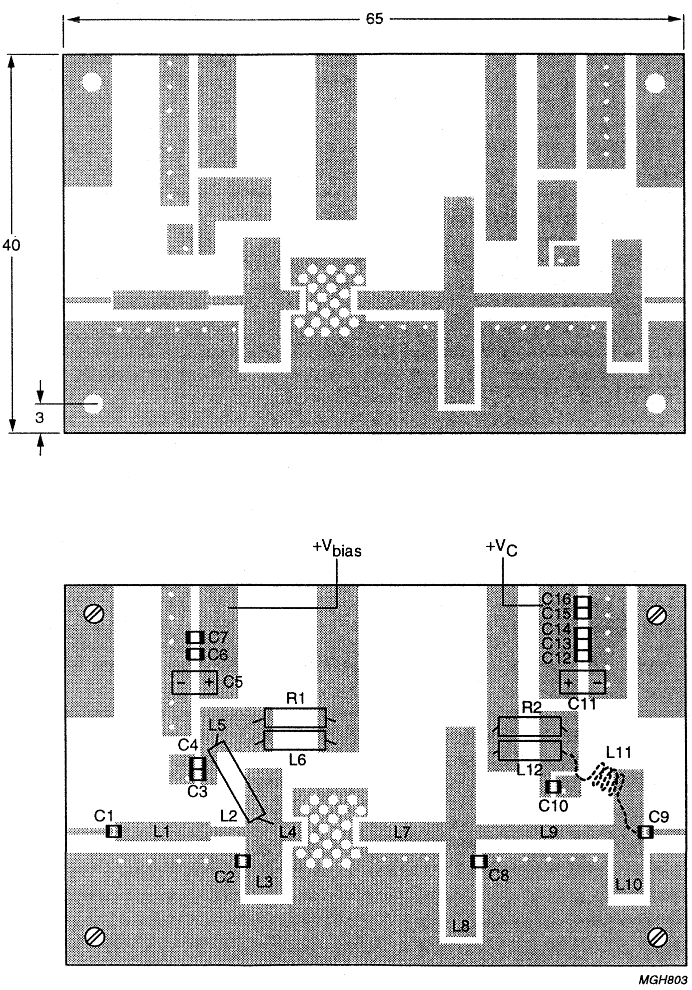


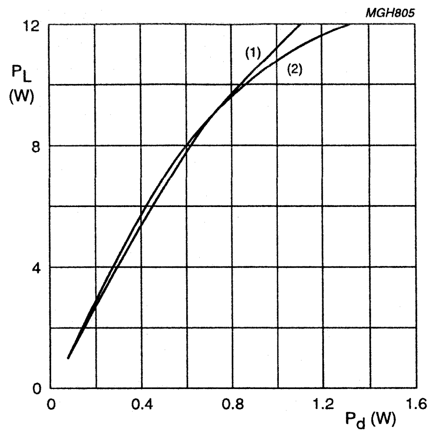
Fig.2 Printed-circuit board and lay-out amplifier.

Table 2

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1 and C9	multilayer ceramic chip capacitor; note 1	24 pF		
C2	multilayer ceramic chip capacitor; notes 1 and 2	5.6 pF		
C3, C7, C10 and C16	multilayer ceramic chip capacitor; note 3	110 pF		
C4 and C15	multilayer ceramic chip capacitor; note 3	200 pF		
C5 and C11	tantal SMD capacitor	35 V; 10 μF		
C6, C12, C13 and C14	ceramic chip capacitor	100 nF		2222 852 47104
C8	multilayer ceramic chip capacitor; note 1	8.2 pF		
L1	stripline	24.3 Ω	9.85 × 2 mm	
L2	stripline	37.5 Ω	3.63 × 1 mm	
L3	stripline	5.11 Ω	4.1 × 13.3 mm	
L4	stripline	24.3 Ω	2 × 2 mm	
L5	RF choke	0.22 μH		
L6, L12	grade 4S2 ferroxcube chip-bead			4330 030 36301
L7	stripline	24.3 Ω	9.2 × 2 mm	
L8	stripline	3.2 Ω	3.1 × 22 mm	
L9	stripline	29.4 Ω	14.4 × 1.5 mm	
L10	stripline	5.22 Ω	3.2 × 13 mm	
L11	5 turns enamelled 1 mm copper wire	35 nH	int. dia. = 3.2 mm pitch = 1.23 mm	
R1 and R2	metal film resistor	100 Ω; 0.4 W		
T1	RF transistor	BLV909		

Notes

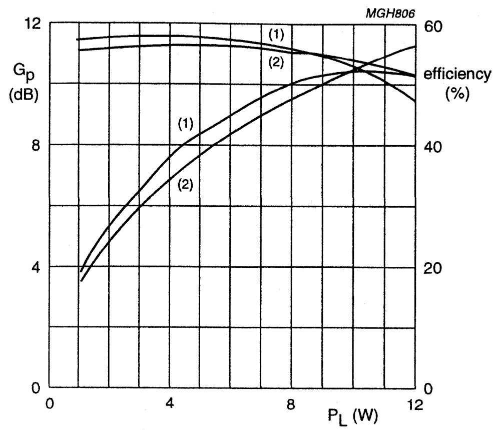
1. American Technical Ceramics type 100A or capacitor of same quality.
2. For operation 820 – 900 MHz: C_2 = 6.2 pF.
3. American Technical Ceramics type 100B or capacitor of same quality.



(1) f = 960 MHz.
(2) f = 935 MHz.

Class AB: V_{ce} = 26 V, I_{cq} = 25 mA, 9 W loadline, f = 960 MHz.

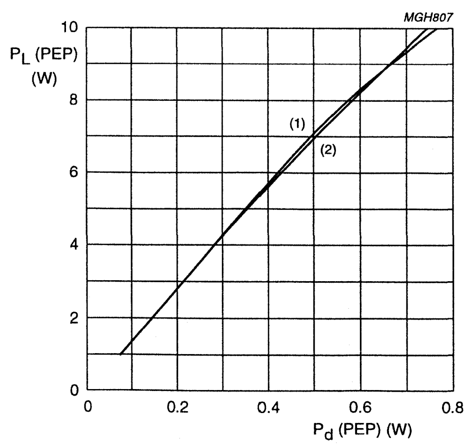
Fig.3 BLV909 PL = f (Pd).



(1) f = 935 MHz.
(2) f = 960 MHz.

Class AB: V_{ce} = 26 V, I_{cq} = 25 mA, 9 W loadline, f1 = 960 MHz.

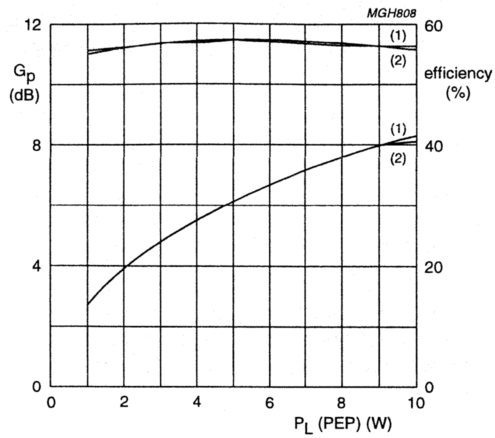
Fig.4 BLV909 Gp and Eff. = f (PL).



(1) f = 960 MHz.
(2) f = 935 MHz.

Class AB: V_{ce} = 26 V, I_{cq} = 25 mA, 9 W PEP loadline delta-f = 0.1 MHz, f1 = 960.1 MHz.

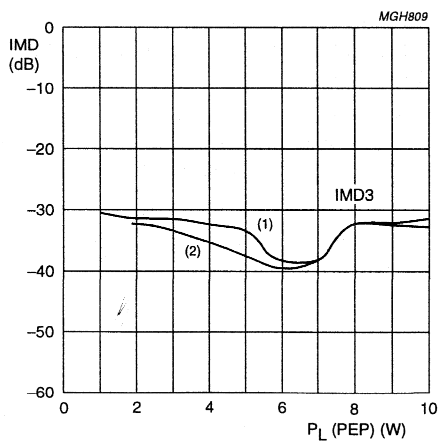
Fig.5 BLV909 PL-PEP = f (Pd).



(1) f = 960 MHz.
(2) f = 935 MHz.

Class AB: V_{ce} = 26 V, I_{cq} = 25 mA, 9 W PEP loadline, delta-f = 0.1 MHz, f1 = 960 MHz, f2 = 960 MHz.

Fig.6 BLV909 Gp and Eff. = f (PL-PEP).



(1) f = 960 MHz.
(2) f = 935 MHz.

Class AB: V_{ce} = 26 V, I_{cq} = 25 mA, 9 W PEP loadline, delta-f = 0.1 MHz, f1 = 960 MHz, f2 = 960.1 MHz.

Fig.7 BLV909 IMD = f (PL PEP).

1 INTRODUCTION

In order to achieve the highest channel capacity available in wireless communications bands, power amplifiers used in these systems must have a carrier-to-intermodulation distortion (IMD) ratio of –60 dBc. The most common way to reach these IMD levels is the feedforward compensation method. With a dualloop feedforward system, a 30 dB improvement in IMD can be achieved. Therefore, the power amplifier in the feedforward system should have at least an IMD of –30 dBc.

When a power amplifier is operated in class A, the –30 dBc IMD can be met. However, collector efficiency of such an amplifier is low. As a result, it is preferable to operate the power amplifier in class AB mode, which gives a higher collector efficiency (typically 35 to 40 percent under two-tone conditions) that improves overall system efficiency considerably. When a bipolar amplifier is operated in class AB, the IMD caused by a combination of the nonlinearities in the RF power transistors' transfercharacteristics (both amplitude and phase) and the amplifier's circuit parameters under certain circumstances results in the amplifier falling short of the –30 dBc IMD that is required.

This article shows the typical behaviour of a 900 MHz amplifier operating in the class AB mode and describes a method to create suppression of the intermodulation products to better than –30 dBc over a 40 dB dynamic range (1 mW to 10 W peak envelope power (PEP)). A 10 W PEP amplifier is used as an example. The used power transistor[1] is a 10 W device for 900 MHz applications operating at 26 V supply voltage. The amplifier has been designed for the 869 to 894 MHz band. Tuning was not applied when the data were recorded.

2 IMD AND POWER GAIN

IMD is related to the output power level (P_{out}) of an RF power device. An RF power amplifier operating in class AB, with a 1 dB compression point of 10 W CW should be able to deliver a PEP of 10 W with a two-tone IMD of –30 dBc. The amplifier's 1 dB compression point is the point where the power gain G_p is decreased by 1 dB when compared to G_p in the linear region. The P_{sat} saturation power is the point where $\Delta P_{out}/\Delta P_{in} = 1$ as shown in Fig.1. Figure 2 shows the method of defining two-tone IMD.

The most common way to specify two-tone intermodulation is to relate it to the level of one of the two carriers f_1 or f_2. The two-tone IMD is expressed in dBc, meaning dB below one carrier. In cases where two-tone IMD is related to the PEP level, the IMD X is a figure that is 6 dB better. In case the transistor is operated in the linear region, the PEP is 3 dB above the average power. The average power is the addition of the average power levels of the carriers f_1 and f_2. For example, $P(f_1) = 1$ W and $P(f_2) = 1$ W, therefore PEP = 4 W.

In class A operation, the IMD will get worse as the output power levels increase. However, when a silicon bipolar transistor is operated in the class AB mode, interesting effects are observed when the device's quiescent current (I_{cq}), that is, the DC collector current when no RF is applied at the input of the amplifier, is varied.

Figure 3 shows the third-order IMD d3 of the devices as a function of the PEP and I_{cq}. The test is performed with a 60 kHz carrier separation. I_{cq} variations change the shape of the d3 curve. A low (5 mA) I_{cq} gives a better d3 at power levels above 8 W PEP. Higher I_{cq} (50 mA) gives better d3 at lower power levels. The effects on the fifth- and seventh-order distortion products is not shown. The change in I_{cq} also affects these IMD products, but the final results show that IMD suppression is sufficient. At the same time, G_p is affected by the change in I_{cq}, as shown in Fig.4.

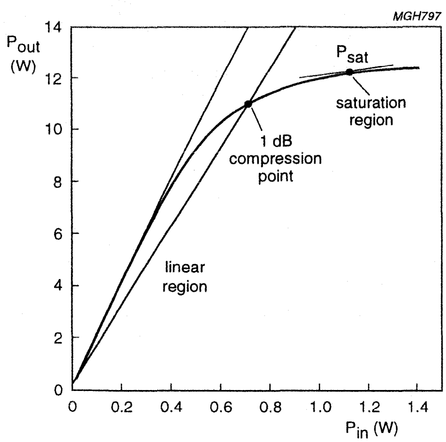


Fig.1 The power amplifier's typical transfer characteristics.

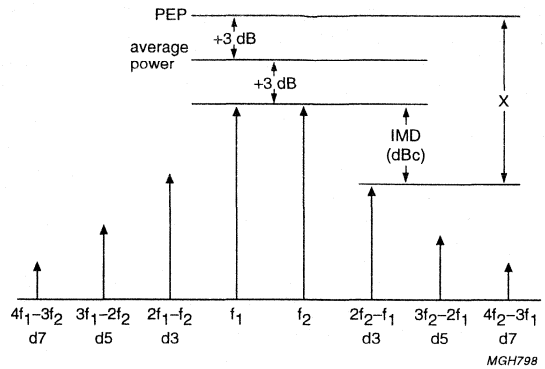
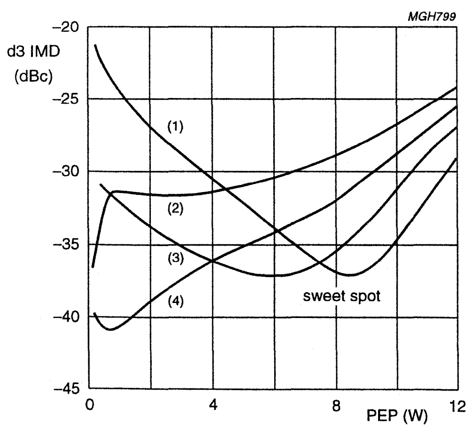
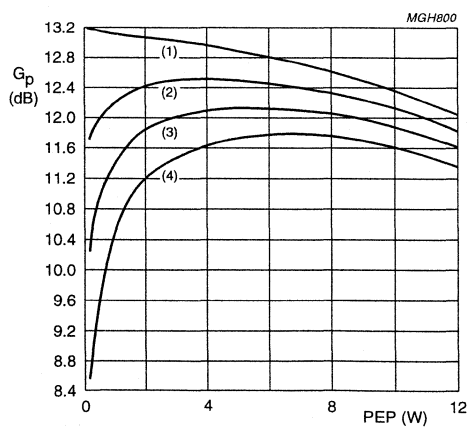


Fig.2 Two-tone IMD.



(1) 5 mA.
(2) 20 mA.
(3) 50 mA.
(4) 100 mA.

Fig.3 Two-tone, third-order IMD vs. PEP and I_{cq}.



(1) 100 mA.
(2) 50 mA.
(3) 20 mA.
(4) 5 mA.

Fig.4 Power gain vs. PEP and I_{cq}.

3 IMD IMPROVEMENT

The ideal situation is an amplifier with a flat response on G_p (gain as a function of output power and gain as a function of frequency) to ensure perfect intermodulation cancellation and an IMD better than −30 dBc over a 40 dB dynamic range to meet the −60 dBc IMD requirement for the complete feedforward amplifier. Considering two-tone, third-order IMD and G_p, a 50 mA I_{cq} is a good choice for power levels below 6 W PEP. For higher power levels the sweet spot (dip in the IMD curve) can be used to obtain a good IMD. However, the sweet spot moves when different I_{cq} are used. A 5 mA I_{cq} gives lower IMD at higher power levels, but will cause more gain compression over the total dynamic range of the amplifier. A sliding I_{cq} as a function of output power is the solution where a range of output power levels is expected. This solution can be achieved by adding a series resistor after the base bypass network, as shown in Fig.5. An increase in RF output power causes an increase in the DC collector current, and thus an increase in the DC-base current. This resistor is marked R. The allowed G_p compression and the desired IMD behaviour as a function of output power determine the value of R. The best way to determine the value of R is to set a goal for the IMD at both low and high power levels. By changing I_{cq}, the desired IMD at these two power levels can be reached. The voltage and the current at point Y have to be recorded for both the low and high power levels, which can be done without the series resistor present. The value of the resistor can be calculated with

$$R = \frac{\Delta V_{be}}{\Delta I_b} = \frac{V_{be1} - V_{be2}}{I_{b2} - I_{b1}} (\Omega)$$

where

R = series resistor (Ω)

V_{be1} = DC voltage a low power level (mV)

V_{be2} = DC voltage at high power level (mV)

I_{b1} = DC base current at lower power level (mA)

I_{b2} = DC base current at high power level (mA).

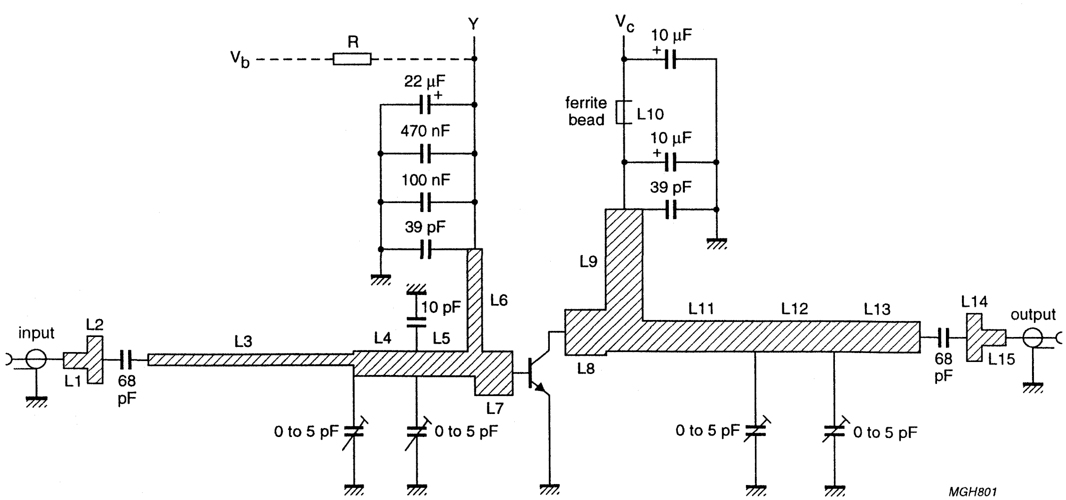
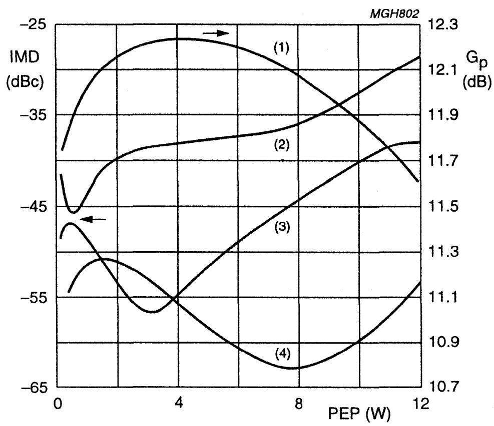


Fig.5 Schematic diagram of the 869 to 894 MHz base station amplifier.

As an example, a power amplifier's desired IMD at 0.4 PEP is < –40 dBc, which means I_{cq} should be 50 mA. The recorded data are V_{be1} = 746 mV and I_{b1} = 1 072 mA. The desired IMD and 10 W PEP is < –30 dBc, which means I_{cq} must be 20 mA. The results are V_{be2} = 710 mV and I_{b2} = 5417 mA. Therefore $R = \frac{(746-710)}{(5417-1072)}$, which approximately equals 8.29 Ω.

Figure 6 shows the G_p and the third-, fifth- and seventh-order IMD products as a function of PEP when an 8.2 Ω resistor is added to the circuit at I_{cq} = 50 mA. Comparison of the IMD data with and without the 8.2 Ω resistor for I_{cq} = 50 mA shows that d3 increases by 4 dB at a P_{out} of 10 W. However, the G_p decreases by 0.3 dB when the 8.2 Ω series resistor is used. In the case where less G_p compression is required, the transistor value should be lowered since this reduces the shift in I_{cq} as a function of output power.

A lower resistor value also impacts the shapes of the IMD curves (d3, d5 and d7). A higher I_{cq} is needed to increase the G_p at low output power levels, impacting IMD.



(1) G_p.
(2) d3.
(3) d5.
(4) d7.

Fig.6 IMD and G_p vs. PEP with the added 8.2 Ω series resistor.

4 CONCLUSION

Using the typical characteristics of a silicon bipolar transistor in the class AB mode, it is possible to improve IMD for medium and high output power levels by adding a series resistor in the base bias network. This simple and reliable method allows the power amplifier to be operated in the class AB mode, which increases amplifier and overall system efficiency considerably. The presented class AB amplifier shows an IMD performance of better then –32 dBc over a 40 dB dynamic range up to 10 W PEP. This performance makes it possible to use the amplifier in a feedforward system, meeting a –60 dBc IMD requirement. The trade-off is a slight increase in gain compression over the total dynamic range. A good selection of I_{cq} and the series resistor value will give a usable compromise.

5 REFERENCES

1. Philips Semiconductors data sheet. BLV910 UHF Power Transitor.
2. P.B. Kenington, 'Efficiency of Feedforward Amplifiers, IEEE Proceeding-G, Vol. 139, No. 5, October 1992, pp. 592-593.
3. Eid E. Eid, Fadhel M. Ghannouchi, Francois Beauregard, 'Optimal Feedforward Linearization System Design,' Microwave Journal, Vol. 38, No. 11, November 1995, pp. 78-86.

Korne Vennema received his B Eng degree in electrical engineering from the Hogere Technische School in Utrecht, the Netherlands in 1987. In March 1987, he joined Philips Semiconductors in Nijmegen, the Netherlands, where he worked as a development engineer on the design of RF power transistors. Since July 1993, Vennema has been with Philips Semiconductors, Slatersville, RI, as an RF application and product engineer.

4 W Linear Class-AB amplifier with the BLV2042 for 1930 –1990 MHz

Application Note AN98018

1 INTRODUCTION

This application note contains information on a 4 W class-AB amplifier based on the SMD transistor BLV2042. The amplifier described can be used for driver stages in cellular radio base stations in the PCS band 1930 – 1990 MHz. The next sections contain information on the transistor, the amplifier construction and the typical RF performance obtained.

2 TRANSISTOR BACKGROUND

The BLV2042 is an NPN bipolar RF power transistor in an 8-lead SMD package called SOT409. The package contains an Aluminium Nitride (AlN) substrate to enhance its thermal performance. The bottom surface is fully metallized to enable reflow soldering of the transistor to the printed-circuit board. All leads are isolated from the bottom surface and a ceramic lid is used to cover the transistor. The BLV2042 features internal input matching for easy wide band matching over the 1930 – 1990 MHz frequency band. When operated from a 26 V supply in class-AB mode the transistor has a minimum power gain of 11 dB and a minimum collector efficiency of 40%. Two tone IMD performance is typically –30 dBc.

3 AMPLIFIER DESCRIPTION

Figure 1 shows the schematic diagram of the amplifier. The matching circuits applied are fixed tuned two-stage lowpass networks using striplines and multilayer chip capacitors. Conventional bias decoupling networks are applied with improved decoupling for two-tone operation. The list of components and stripline dimensions is given in Table 2. Figure 2 contains the printed-circuit board layout and components topology of the amplifier. The printed-circuit board contains a footprint of solder pads for collector and base lead interconnect and a thermal pad with vias to provide a low thermal resistance path to the package. Pads with vias for RF grounding of the emitter leads are integrated with the thermal pad. All SMD components were reflow soldered to the printed-circuit board. The printed-circuit board was soldered to a heatsink in the same process step. More details on the mounting considerations for the SOT409B can be found in application note AN98017. The pc-board material used is Rogers RT/Duroid 6006 with a dielectric constant of 6.15 and a thickness of 0.64 mm.

4 AMPLIFIER PERFORMANCE

The amplifiers performance was measured at V_{ce} = 26 V and I_{cq} = 15 mA. The heatsink temperature was held at 25 °C during the measurement. A summary of the performance is given in Table 1.

Table 1

	UNIT	SINGLE-TONE	TWO-TONE
Frequency band	MHz	1930 – 1990	1930 – 1990
Load power	W	4	4 (PEP)
Power gain	dB	11	11.5
Power gain flatness	dB	1.5	–
Collector efficiency	%	45	35
Intermodulation distortion	dBc	–	–32 @ 4 W PEP

Single-tone performance curves are presented in

Figure 3; Load power(PL) versus drive power(Pd)

Figure 4; Power gain (Gp) and collector efficiency(Eff) versus load power (PL).

Two-tone performance curves are presented in

Figure 5; Load power (PL-PEP) versus drive power (Pd-PEP)

Figure 6; Power gain (Gp) and collector efficiency (Eff) versus load power (PL-PEP).

Figure 7; Intermodulation distortion (d3) as function of load power (PL-PEP).

5 CONCLUSION

An AlN based surface mountable transistor BLV2042 has been used to develop an amplifier for driver application in PCS base stations. Biased at 26 V and 15 mA this amplifier has shown a 4 W CW power output capability with a gain of 11 dB and a collector efficiency 45%. For two-tone operation the IMD performance is better than –32 dBc at 4 W PEP.
In addition the IMD over a wide dynamic range can be further optimized by adding a base series resistor of a few ohms combined with a good selection of I_{cq} as described in application note AN98026.

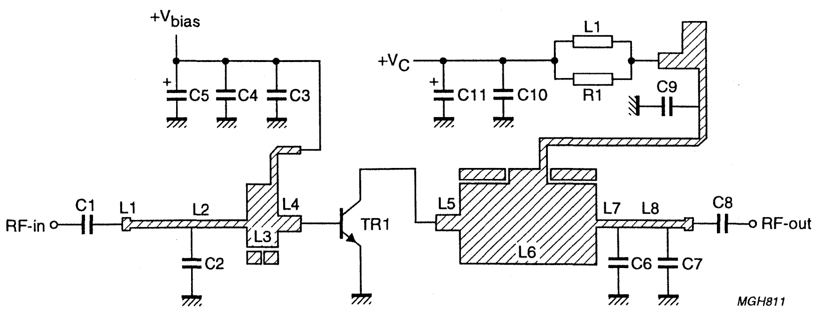


Fig.1 Schematic diagram.

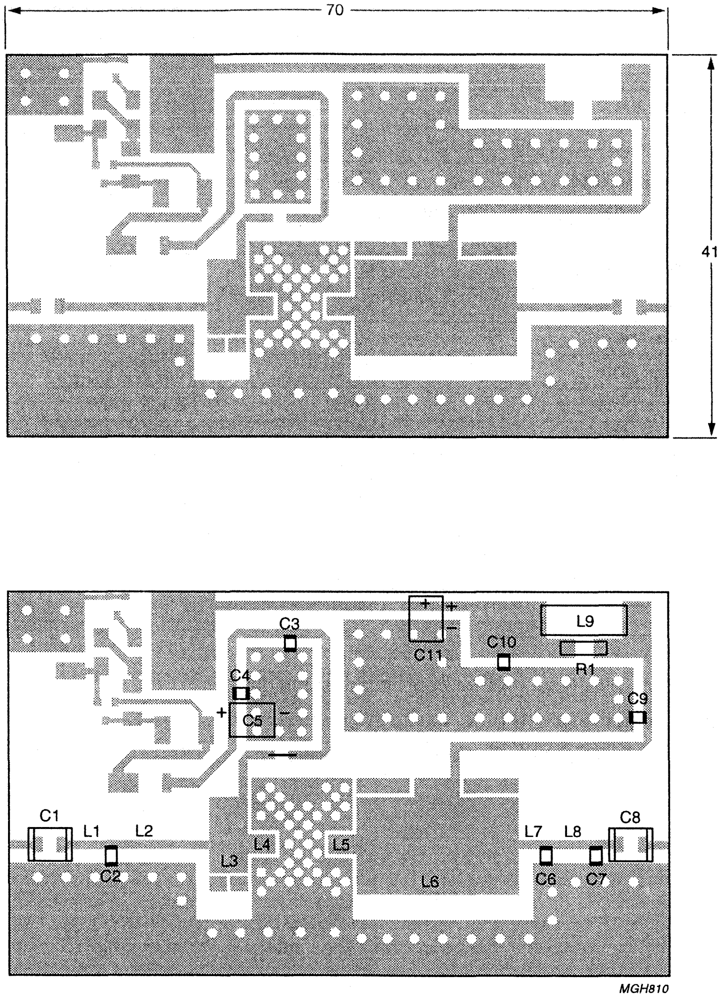


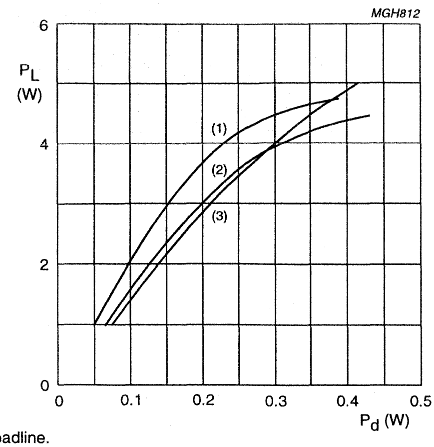
Fig.2 Printed-circuit board and layout.

Table 2

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1 and C9	multilayer ceramic chip capacitor; note 1	100 pF		
C2 and C6	multilayer ceramic chip capacitor; note 2	3.0 pF		
C3 and C8	multilayer ceramic chip capacitor; note 2	27.0 pF		
C4 and C10	multilayer ceramic chip capacitor	100 pF		2222 581 16641
C5 and C11	tantal SMD capacitor	35 V; 47 μF		
C7	multilayer ceramic chip capacitor; note 2	1.2 pF		
L1	stripline; note 3	50 Ω	9.91 × 0.91 mm	
L2	stripline; note 3	50 Ω	13 × 0.91 mm	
L3	stripline; note 3	10 Ω	4 × 8 mm	
L4	stripline; note 3	31 Ω	3 × 2 mm	
L5	stripline; note 3	31 Ω	3 × 2 mm	
L6	stripline; note 3	8.3 Ω	17.25 × 10.3 mm	
L7	stripline; note 3	50 Ω	2.42 × 0.91 mm	
L8	stripline; note 3	50 Ω	6.14 × 0.91 mm	
L9	grade 4S2 ferroxcube chip-bead			4330 030 36301
R1	metal film resistor	100 Ω; 0.4 W		
T1	RF transistor	BLV2042		

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. American Technical Ceramics type 100A or capacitor of same quality.
3. The stripline are on double copper-clad printed-circuit board RT/Duroid 6006 (ε_r = 6.15); thickness 0.64 mm.



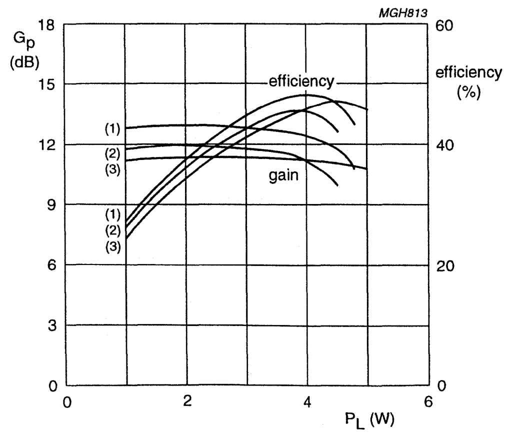
Class AB: V_{ce} = 26 V; I_{cq} = 15 mA; 4 W loadline.

(1) f = 1930 MHz.

(2) f = 1990 MHz.

(3) f = 1950 MHz.

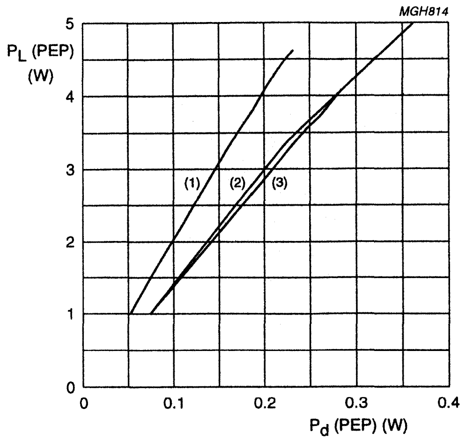
Fig.3 PL = f (Pd).



Class AB: V_{ce} = 26 V; I_{cq} = 15 mA; 4 W loadline.

Gian:	Efficiency
(1) f = 1930 MHz.	(1) f = 1930 MHz.
(2) f = 1990 MHz.	(2) f = 1990 MHz.
(3) f = 1950 MHz.	(3) f = 1950 MHz.

Fig.4 Gp and Eff. = f (PL).



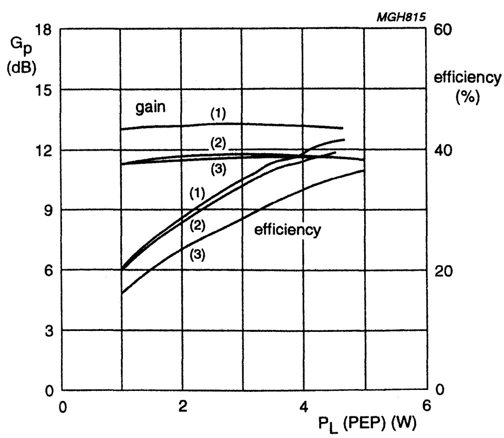
Class AB: V_{ce} = 26 V; I_{cq} = 15 mA; 4 W PEP loadline; delta-f = 0.1 MHz.

(1) f = 1930 MHz.

(2) f = 1990 MHz.

(3) f = 1950 MHz.

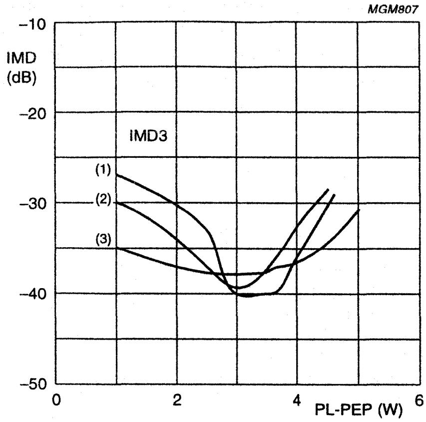
Fig.5 f = PL-PEP = f (Pd).



Class AB: V_{ce} = 26 V; I_{cq} = 15 mA; 4 W PEP loadline; delta-f = 0.1 MHz.

Gian:	Efficiency
(1) f = 1930 MHz.	(1) f = 1930 MHz.
(2) f = 1990 MHz.	(2) f = 1990 MHz.
(3) f = 1950 MHz.	(3) f = 1950 MHz.

Fig.6 Gp and Eff. = f (PL-PEP).



Class AB: V_{ce} = 26 V; I_{cq} = 15 mA; 4 W PEP loadline; delta-f = 0.1 MHz.

(1) f = 1930 MHz.

(2) f = 1990 MHz.

(3) f = 1950 MHz.

Fig.7 IMD = f (PL PEP).

15 W class-AB amplifier with the BLV2044 for 1930 – 1990 MHz (PCS)

Application Note
AN98022

1 INTRODUCTION

In this application note a 15 W linear base station amplifier for the 1930 – 1990 MHz PCS band is given.
The amplifier is equipped with the Philips BLV2044, a NPN silicon planar transistor in a 2-lead SOT437 flange package. The BLV2044 features internal input- and output matching to achieve high power gain and collector efficiency, and to ease the design of wideband circuits. Other features of the BLV2044 are gold top metallization for excellent reliability and emitter ballasting resistors for optimum temperature profile. When operated from a 26 V supply in class-AB mode the transistor has a minimum power gain of 8 dB and a minimum collector efficiency of 40% at 15 W CW output power level. Two-tone IMD performance is typically –30 dBc

2 CIRCUIT DESCRIPTION

The circuit diagram of the amplifier is given in Fig.1. Substrate material used in double copper-clad Rogers 6006, with a dielectrical constant of 6.15 and a substrate thickness of 0.635 mm (0.025"). Low Q matching networks at input- and outputside of the transistor are designed for an optimum gain flatness and efficiency over the PCS band. Bypass capacitors C5 and C7 resonate at approximately 2 GHz. Capacitors C2, C3 and C8 are added to improve intermodulation distortion. A list of components and stripline dimensions is given in Table 1. Figure 2 includes printed-circuit board and component layout for PCS applications.

3 DC BIAS CIRCUIT

Figure 3 does include an example for a temperature compensated DC bias circuit, which operates from a 15 V supply voltage and ensures a constant bias voltage. R5 is added in series for a flat response of the intermodulation distortion over the amplifier's total dynamic range. See application note AN98026 for more background information.

4 RF MEASUREMENT RESULTS

All measurements were taken at 26 V supply voltage at a frequency of 1950 MHz and a heatsink temperature of 25 °C. Both input and output were fixed tuned.

- Gp and ηc = f(PL), PL = f(Pin)
- Gp = f(Pd), IMD = f(PL), d3 = f(PL).

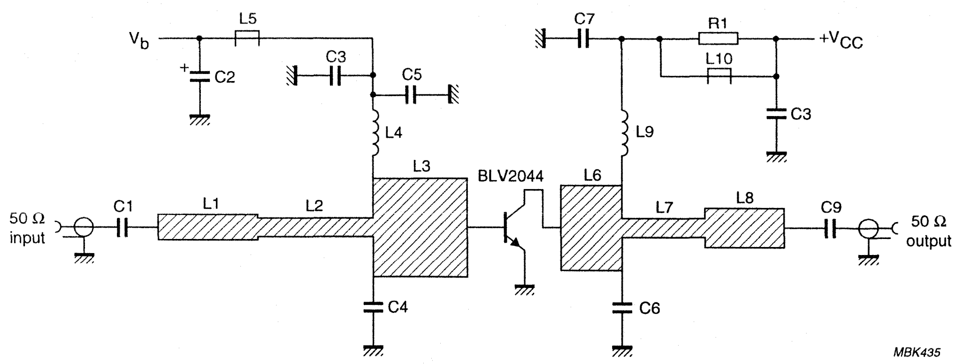
Important: demoboard must be placed on a heatsink in order to get a proper cooling.

Single-tone performance curves are presented in, Figs 4 to 7 at an I_{cq} of 40 mA. Figure 8 presents the gain expansion versus drive level at serval I_{cq} settings. Two-tone intermodulation behaviour of the amplifier is presented in Figs 9 and 10.

5 CONCLUSIONS

The amplifier described can be used in PCS applications and is able to deliver 15 W CW power with a gain of 9 dB and an efficiency of 47%. For two-tone operation IMD-3 is below –32 dBc for optimum I_{cq} setting.

The matching networks applied also allow operation in the DCS 1800 band.



See Table 1: List of components.

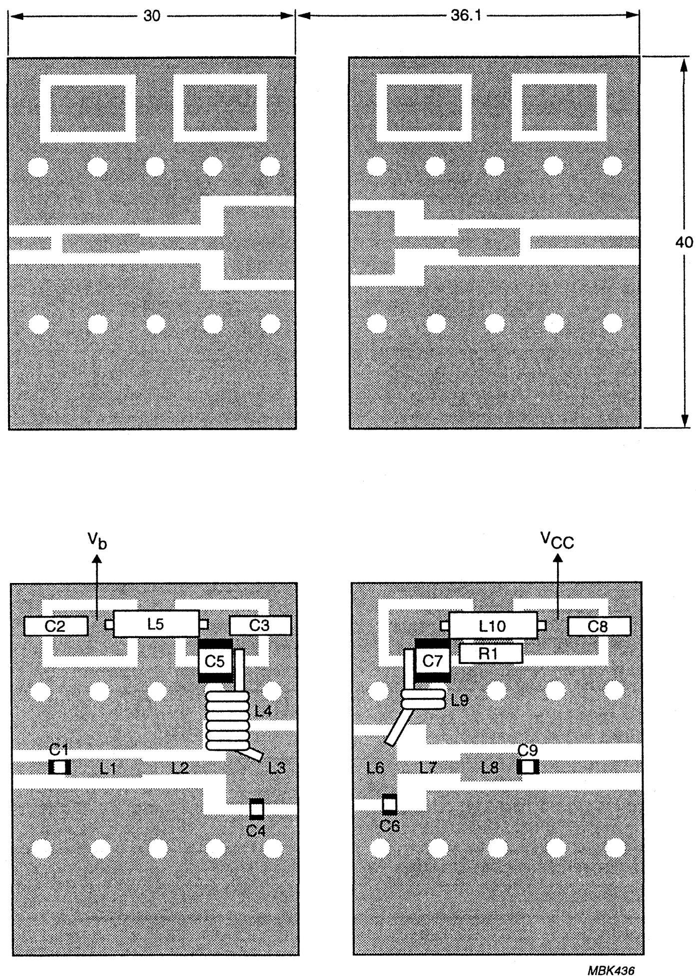
Fig.1 Class-AB testcircuit for 1.8 to 2 GHz.

Table 1 List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C9	multilayer ceramic chip capacitor; note 1	30 pF		
C2	tantal SMD capacitor	35 V; 10 μF		
C3	multilayer ceramic chip capacitor	22 nF		2222 629 08223
C4	multilayer ceramic chip capacitor; note 1	1.1 pF		
C5, C7	multilayer ceramic chip capacitor; note 2	20 pF		
C6	multilayer ceramic chip capacitor; note 1	1.2 pF		
C3	multilayer ceramic chip capacitor	100 nF		2222 852 47104
L1	stripline; note 3	31 Ω	7.8 × 2 mm	
L2	stripline; note 3	40 Ω	8.8 × 1.4 mm	
L3	stripline; note 3	10 Ω	8 × 8 mm	
L4	5 turns enamelled 1 mm copper wire	38 nH	int. dia = 3 mm; length = 8 mm	
L5, L10	grade 4S2 ferroxcube chip-bead			4330 030 36301
L6	stripline; note 3	12 Ω	5 × 7 mm	
L7	stripline; note 3	40 Ω	6.7 × 1.4 mm	
L8	stripline; note 3	23 Ω	6.4 × 3 mm	
L9	2 turns enamelled 1 mm copper wire	9 nH	int. dia = 3 mm; length = 4 mm	
R1	metal film resistor	10 Ω; 0.4 W		2311 153 51009

Notes

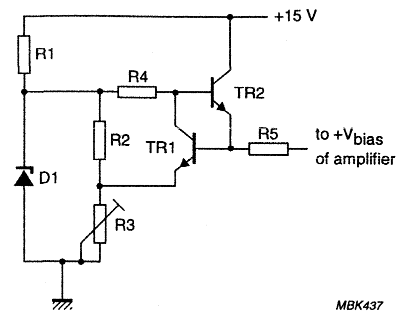
1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. The striplines are on a double copper-clad Printed-circuit board with epoxy fibre-glass dielectric ($\varepsilon_r = 6.15$); thickness 0.64 mm.



Dimensions in mm.

The components are situated on one side of the copper-clad epoxy fibre-glass board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.2 printed-circuit board and component layout for 1.8 to 2 GHz class-AB testcircuit.

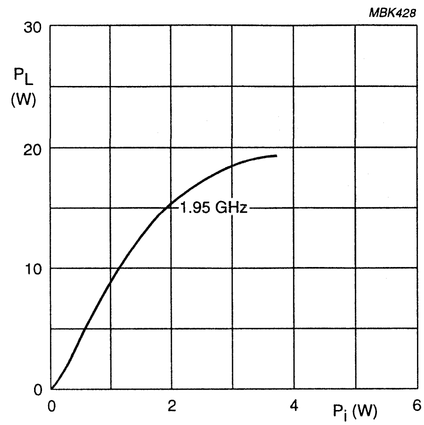


See Table 2.

Fig.3 Class AB bias network.

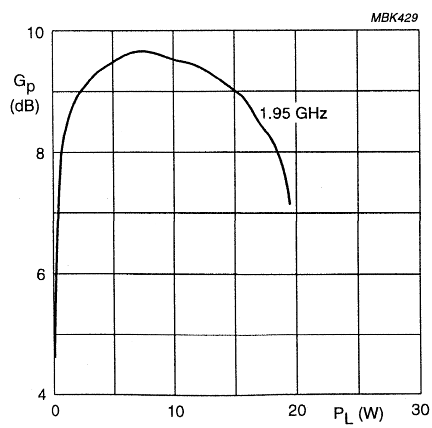
Table 2

COMPONENTS	TYPE NUMBER	DESCRIPTION
Semiconductors		
D1	BZX84, C6V2	SMD Zener Diode
T1	MJD31C	SMD NPN Transistor
T2	BC846C	SMC NPN Transistor
Resistors		
R1	1.1 kΩ	SMD resistor Philips 1206
R2	4.3 kΩ	SMD resistor Philips 1206
R3	500 Ω	Bourns 10 turn
R4	3 kΩ	SMD resistor Philips 1206
R5	3.3 Ω	SMD resistor Philips 1206
R6	11 Ω	SMD resistor Philips 1206



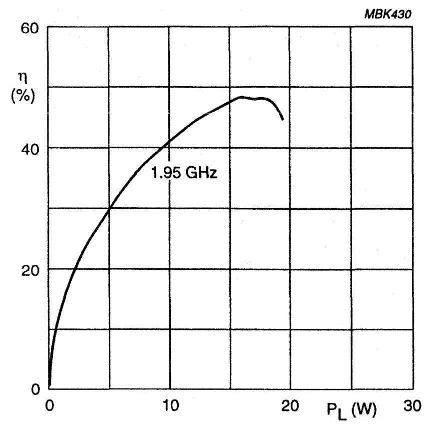
V_{CE} = 26 V; I_{cq} = 40 mA.

Fig.4 Output power versus input power; typical value.



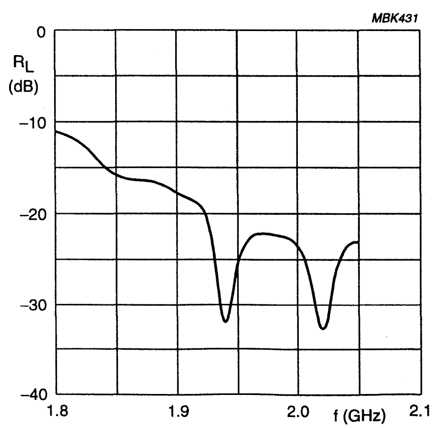
V_{CE} = 26 V; I_{cq} = 40 mA.

Fig.5 Power gain versus output power; typical level.



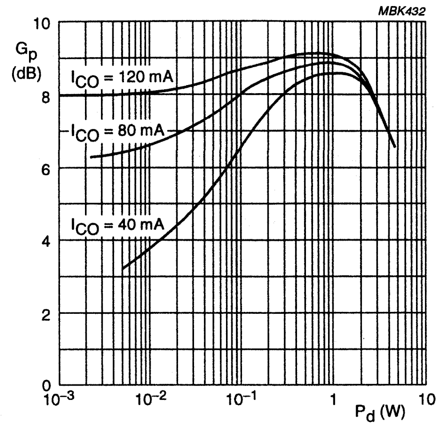
V_{CE} = 26 V; I_{cq} = 40 mA.

Fig.6 Efficiency versus output power; typical level.



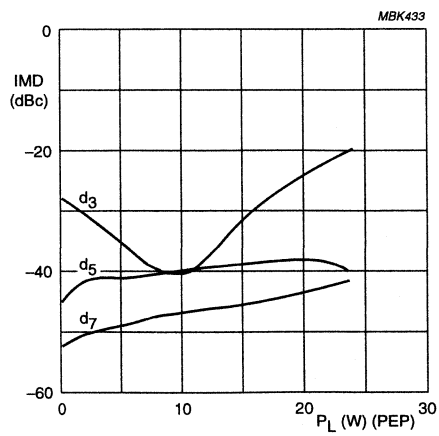
V_{CE} = 26 V; I_{cq} = 40 mA.

Fig.7 Input return loss versus frequency.



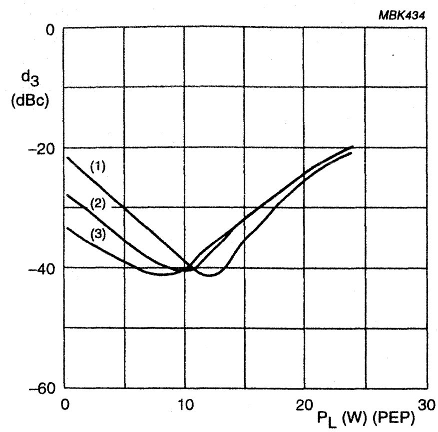
V_{CE} = 26 V; f = 1950 MHz.

Fig.8 Power gain expansion as a function of the drive power: typical values.



V_{CE} = 26 V; I_{cq} = 40 mA; f_2 = 1950 MHz; f_1 = 1950.1 MHz.

Fig.9 Intermodulation distortion as a function of the load power: typical values.



V_{CE} = 26 V; f_1 = 1950 MHz; f_2 = 1950.1 MHz.

(1) I_{cq} = 20 mA.

(2) I_{cq} = 40 mA.

(3) I_{cq} = 60 mA.

Fig.10 Intermodulation distortion as a function of the load power: typical values.

30 W class-AB amplifier with the BLV2045 for 1 930 – 1 990 MHz (PCS)

Application Note AN98023

1 INTRODUCTION

In this application note a 30 W linear base station amplifier for the 1 930 – 1 990 MHz (PCS) band is given.
The amplifier is equipped with the Philips BLV2045, a NPN silicon planar transistor in a 2-lead SOT390 flange package. The BLV2045 features internal input- and output matching to achieve high power gain and collector efficiency and to ease the design of wideband circuits. Other features of the BLV2045 are gold top metallization for excellent reliability, and emitter ballasting resistors for optimum temperature profile. When operated from a 26 V supply in class AB mode the transistor has a minimum power gain of 8 dB and a minimum collector efficiency of 40% at a 30 W CW output power level. Two-tone IMD performance is typically –30 dBc.

2 CIRCUIT DESCRIPTION

The circuit diagram and list of components of the amplifier is given in Fig.1. Substrate material used in double copper-clad Rogers 6006, with a dielectrical constant of 6.15 and a substrate thickness of 0.635 mm (0.025 inch). Low Q matching networks at input- and output of the transistor are designed for an optimum gain flatness and efficiency over the entire band. Bypass capacitors C5 and C7 resonate at approximately 2 GHz. Capacitors C2, C3 and C8 are added to improve intermodulation distortion. Figure 2 includes component layout and printed-circuit board for both PCS applications.

3 DC BIAS CIRCUIT

Figure 3 does include an example for a temperature compensated DC bias circuit, which operates from a 15 V supply voltage and ensures a constant bias voltage. R5 is added for a flat response of the intermodulation distortion over the amplifier's total dynamic range. See application note AN98026 for background.

4 RF MEASUREMENT RESULTS

All measurements were taken at 26 V supply voltage at the frequencies of 1900 and 1990 MHz and a heatsink temperature of 25 °C. Both input and output were fixed tuned. The single tone performance of the amplifier is given in the Figs 4 to 7 at a I_{cq} of 80 mA. Figure 8 presents the gain expansion versus drive level at several I_{cq} settings. Two tone intermodulation behaviour of the amplifier is given in Figs 9 and 10.

5 CONCLUSIONS

The amplifier described can be used in PCS applications and is able to deliver 30 W CW power with a gain of 8.5 dB and an efficiency of 46%. For two-tone operation IMD-3 is below –30 dBc for optimal I_{cq} setting. The matching networks applied also allow operation in the 1805 – 1880 MHz band (PCN).

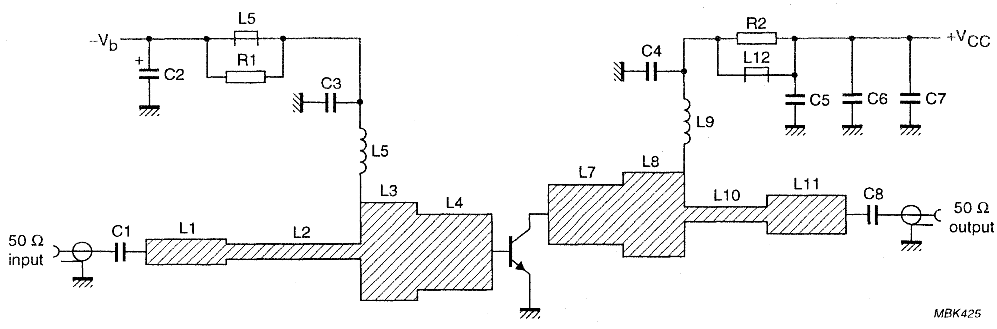


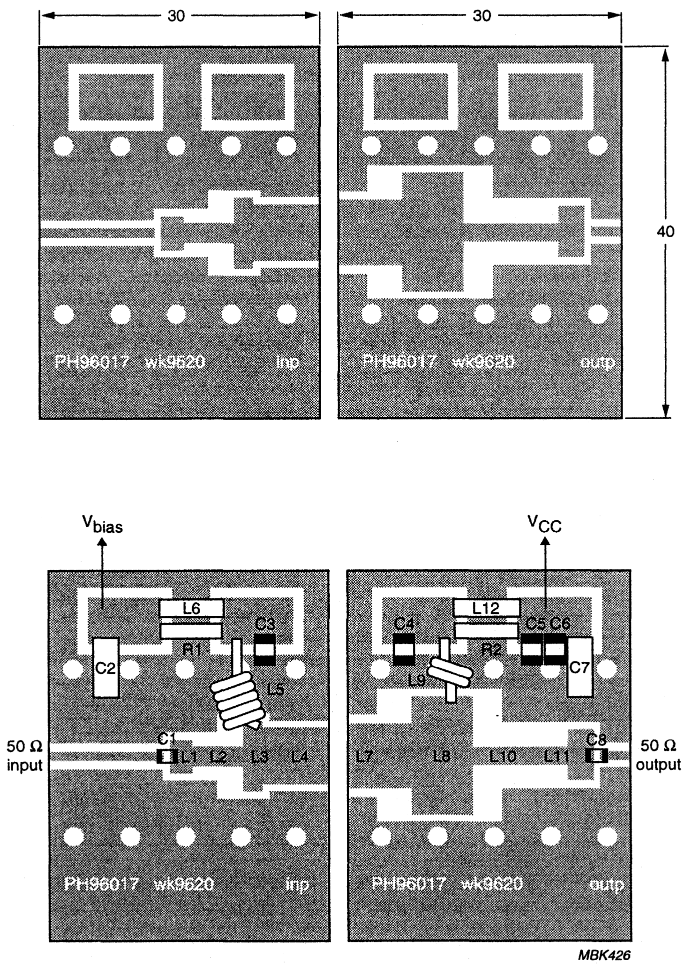
Fig.1 Class-AB testcircuit for 1.8 to 2 GHz.

Table 1 List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C8	multilayer ceramic chip capacitor; note 1	30 pF		
C2, C7	tantal SMD capacitor	35 V; 10 μF		
C3, C4	multilayer ceramic chip capacitor; note 2	20 pF		
C5	multilayer ceramic chip capacitor	22 nF		2222 629 08223
C6	multilayer ceramic chip capacitor	100 nF		2222 852 47104
L1	stripline; note 3	20.5 Ω	2.5 × 3.5 mm	
L2	stripline; note 3	29.8 Ω	5.6 × 2.1 mm	
L3	stripline; note 3	11 Ω	2 × 7.4 mm	
L4	stripline; note 3	13.2 Ω	7.2 × 6 mm	
L5	5 turns enamelled 1 mm copper wire	38 nH	int. dia = 3 mm; length = 8 mm	
L6, L12	grade 4S2 ferroxcube chip-bead			4330 030 36301
L7	stripline; note 3	11.5 Ω	6.6 × 7.1 mm	
L8	stripline; note 3	6.9 Ω	6.4 × 12.6 mm	
L9	2 turns enamelled 1 mm copper wire	9 nH	int. dia = 3 mm; length = 4 mm	
L10	stripline; note 3	35.8 Ω	9.9 × 1.6 mm	
L11	stripline; note 3	14.4 Ω	2.7 × 5.4 mm	
R1, R2	metal film resistor	10 Ω; 0.4 W		2311 153 51009

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. The striplines are on a double copper-clad PCB with epoxy fibre-glass dielectric (ε_r = 6.15); thickness 0.64 mm.



Dimensions in mm.

The components are situated on one side of the copper-clad epoxy fibre-glass board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.2 Component layout and printed-circuit board for 1.8 to 2 GHz class-AB testcircuit.

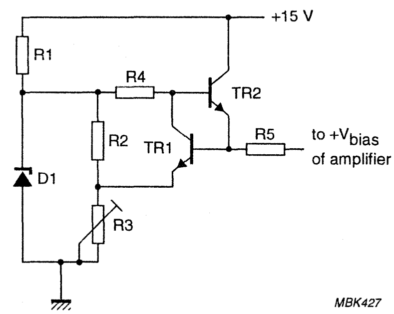


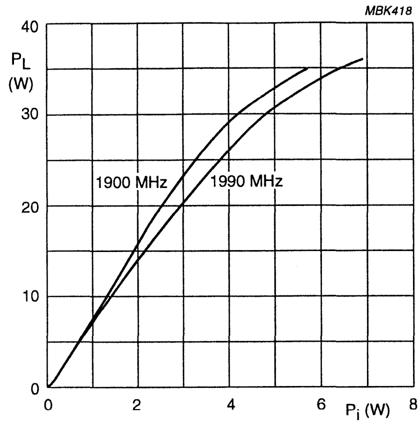
Fig.3 Class AB bias network.

Table 2 Semiconductors

COMPONENTS	TYPE NUMBER	DESCRIPTION
D1	BZX84, C6V2	SMD Zener Diode
T1	MJD31C	SMD NPN Transistor
T2	BC846C	SMC NPN Transistor

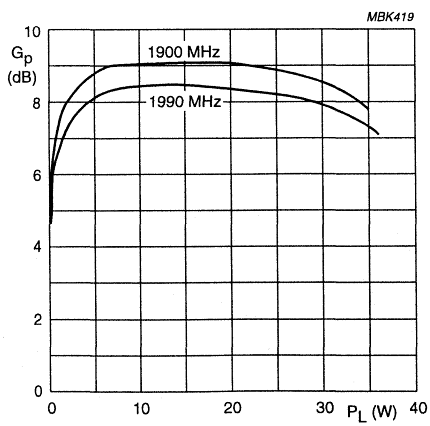
Table 3 Resistors

COMPONENTS	VALUES	DESCRIPTION
R1	1.1 kΩ	SMD resistor Philips 1206
R2	4.3 kΩ	SMD resistor Philips 1206
R3	500 Ω	Bourns 10 turn
R4	3 kΩ	SMD resistor Philips 1206
R5	3.3 Ω	SMD resistor Philips 1206



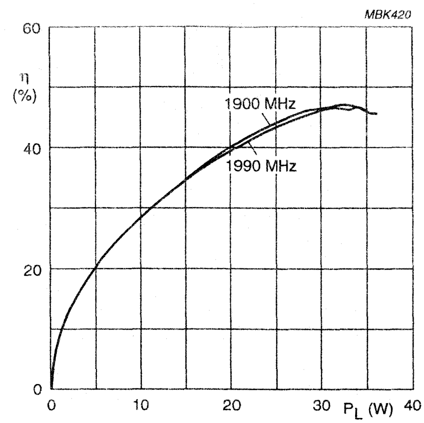
V_{CE} = 26 V; I_{cq} = 80 mA.

Fig.4 Output power as a function of input power; typical values.



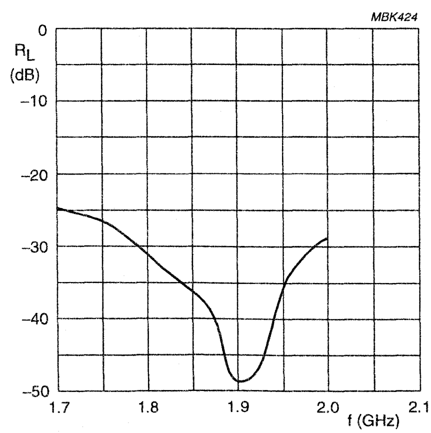
V_{CE} = 26 V; I_{cq} = 80 mA.

Fig.5 Power gain versus output power; typical values.



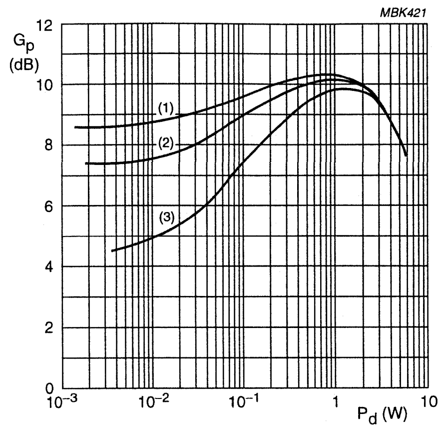
V_{CE} = 26 V; I_{cq} = 80 mA.

Fig.6 Collector-efficiency as a function of output power; typical values.



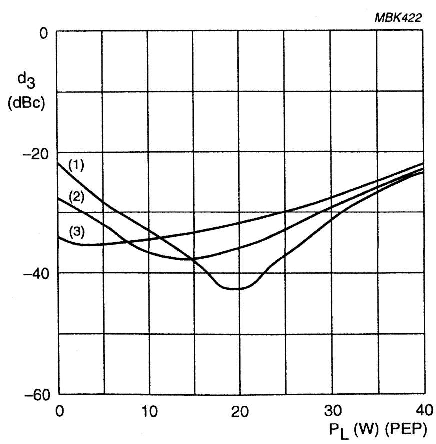
V_{CE} = 26 V; I_{cq} = 80 mA.

Fig.7 Input return loss as a function of frequency.



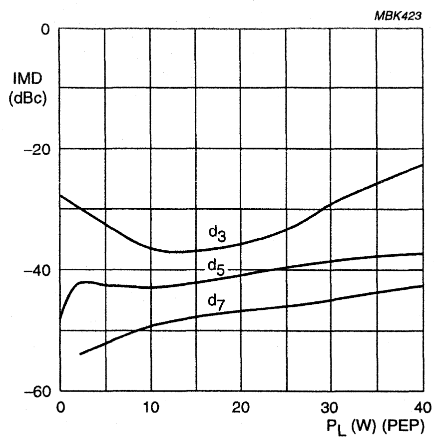
V_{CE} = 26 V; f = 1950 MHz.
(1) I_{CQ} = 240 mA.
(2) I_{CQ} = 160 mA.
(3) I_{CQ} = 80 mA.

Fig.8 Power gain expansion as a function of the drive power; typical values.



V_{CE} = 26 V; f_1 = 1950 MHz; f_2 = 1950.1 MHz.
(1) I_{CQ} = 40 mA.
(2) I_{CQ} = 80 mA.
(3) I_{CQ} = 120 mA.

Fig.9 Intermodulation distortion as a function of the load power; typical values.



V_{CE} = 26 V; I_{cq} = 80 mA; f_1 = 1950 MHz; f_2 = 1950.1 MHz.

Fig.10 Intermodulation distortion as a function of the load power; typical values.

50 W base station power amplifier for DCS1800 and PCS1900

Application Note
AN98024

1 ABSTRACT

In the fast emerging market of wireless communications, ease of design, high performance and low production costs are important design key parameters. This paper describes a 50 W modular base station power amplifier design for DCS1800 and PCS1900. The low cost reliable concept, that allows for very fast design cycles, consists of a 50 W power transistor driven by a power module and a low cost wide band transistor. The design is realised on a low cost substrate material and, at 26 V supply voltage, an overall gain larger than 47 dB has been reached at 50 W continuous wave output power.

2 INTRODUCTION

This paper will discuss the realisation of a 3 stage silicon bipolar 50 W RF line up solution for DCS1800 (1 805 to 1 880 MHz) and PCS1900 (1 930 to 1 990 MHz) (GMSK modulation). As a target, the minimum overall gain was set to 47 dB, corresponding with 1 mW input to achieve 50 W (+47 dBm) RF output power into a 50 Ω load. 26 V supply voltage and a bias/switching voltage of 5 V are assumed to be available in base station power supplies. The low loss and low cost printed-circuit board used, is a Rogers RT4000 series epoxy based board (32 mils) with enhanced RF performance compared to FR4.

The design maintains the possibility to test each stage separately as well as the overall performance.

The gain criteria for the line up is defined as follows: pre-driver gain larger than 15 dB, driver gain larger than 24 dB and final stage gain larger than 8 dB. These requirements can be obtained using the following Philips components (see Fig.1): stage 1: BFG425W wide band transistor, stage 2: BGY1816 or BGY1916 power module (depending on the frequency band) and stage 3: BLV2046 Si power transistor. In the following paragraphs these devices will be discussed in detail, the final paragraph will discuss the full line up with measurement results.

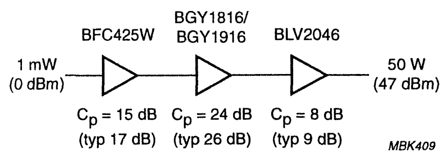


Fig.1 The 50 W line-up.

The pre-driver is biased in class A and matched for wide band operation over 1 800 to 2000 MHz (no tune design). The 5 V supply powers the BFG425W and can switch the bias circuit of the module and final amplifier on/off e.g. for trouble shouting of the base station. The module is factory optimised for gain, efficiency and output power for the DCS (BGY1816) and PCS (BGY1916) band with internal biasing circuitry (no tune design). With only design time necessary for the final amplifier (minimum tuning), a quick and cheap base station power amplifier can be designed.

Nominal operating collector efficiency for the module is 35% at 16 W. Bearing this in mind and a 45% typical efficiency of the BLV2046, the overall line-up efficiency is 35% at 50 W.

3 PRE-DRIVER (BFG425W)

The BFG400W series wide band silicon transistors are using Double Poly Silicon technology. With a Ft over 20 GHz, high gain and low noise properties, the BFG400W series can be used for many applications.

To drive the module it is calculated that 20 mW output power is required. The BFG425W is the best choice in the BFG400W series to accomplish this target. With it's small footprint (typ. 2.0 × 1.25 mm, SOT343R, see Fig.2) and SMD components, a compact pre driver can be build for the module to keep valuable board space to a minimum and take advantage of pick and place machines during production.

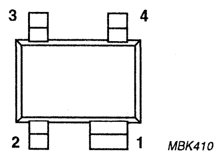


Fig.2 The SOT343R package.

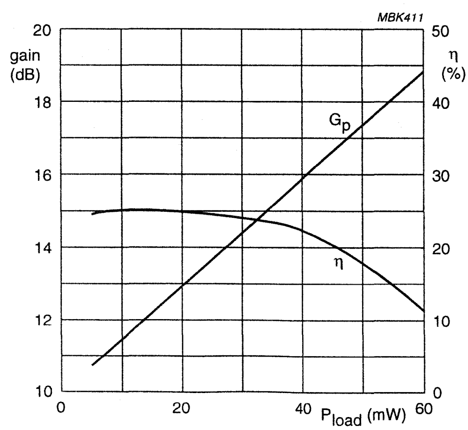


Fig.3 Gain and efficiency of BFG425W.

Biased in class A, the BFG425W is set to 30 mA and V_{CE} = 4 V, S parameters were measured and analysed for stability, matching and gain flatness. Computer simulations (HP-MDS) calculated the necessary matching component values and topology, optimized for 1800 to 2000 MHz band. Calculations/measurements proved sufficient bandwidth, which allows a design without tuning in production.

Summary of results:

Table 1 The results of the BFG425W

BFG425W	RESULTS	CONDITIONS
Gain	15.0 dB	Pload = 20 mW
P1 dB	45 mW	
Efficiency	33%	Pload = 45 mW
ΔGain vs. Frequency	<1 dB	
ΔGain vs. Pload	<1 dB	
Return loss in	<–15 dB	
Return loss out	<–15 dB	

Analysis has proven the BFG425W to deliver sufficient output power and gain to drive the module and final amplifier without running into compression, see Fig.3.

4 DRIVER (BGY1816/BGY1916)

As driver, a power module is used to boost the pre-driver signal sufficiently to drive the final amplifier. Running from a 26 V rail (and 5 V bias) the module can easily generate 16 W of RF power into a 50 Ω load with a gain of 26 dB.

Advantages for using a module are the 50 Ω input and output impedance, the small size and the fact that no tuning is required in production (thus saving production time), all of these reducing Time to Market in both design and production phase of the complete amplifier. In addition the very competitive price of the module is an advantage.

Two modules are available, an 1800 MHz (BGY1816) and a 1900 MHz (BGY1916) version, each factory optimised for output power, gain flatness and efficiency for their particular frequency bands.

AIN is used as substrate carrier for all modules, to eliminate the hazardous BeO for power devices and to keep our environment safe. Al_2O_3 is not preferred in these modules as the temperature handling is roughly 10 times worse than AIN and inserts are necessary for heat sinking for the power related transistors. All traces are thin film, gold metallized, on the AIN substrate, thus guaranteeing a consistent product during production.

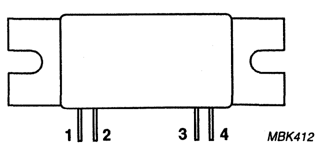


Fig.4 The SOT365 package.

The module consists of 3 stages silicon bipolar transistors. The package used is a SOT365 (16.5 × 48.0 mm, see Fig.4). The first stage is biased in class A to obtain high gain, linearity and a constant 50 Ω input impedance. The second and final stages are biased in class AB to increase the efficiency.

Each transistor is internally biased with a temperature compensated network. With these networks it is possible to adjust each individual transistor during production (if necessary) to assure specified gain expansion over power sweep and temperature range up to 85 °C.

An equaliser matching network between first and second stage is placed to control the gain slope over frequency. All RF-related dies are pre-matched with MOS capacitors to minimise component losses and guarantee (constant Q) gain performance during production. The matching networks consists of 0603 capacitors and distributed inductors. The final stage uses a collector matching network to improve broadband performance and efficiency. The final stage consists of 4 dies in parallel, each die capable to produce 6 W of RF power, thus producing 24 W of RF power in saturation. IR scans proved during RF operation (16 W) and under load mismatch condition (VSWR 1 : 5, all phases) that the junction temperature of any die remains well under 170 °C with a Tmb equal to 85 °C, necessary to guarantee module reliability and MTBF. Figure 5 shows the typical gain and efficiency performance of the BGY1816 module.

Summary of results:

Table 2 The results of the BGY1816

BGY1816	RESULTS
Gain	26 dB (typical, min spec 24 dB)
Efficiency	>30% @ 16 W
Psaturation	>22 W
Gain expansion	<1 dB
Gain ripple	<2 dB
DIMD	<–55 dBc (16 W, –40 dBc) @ 100 kHz
RIMD	<–55 dBc (16 W, –35 dBc) @ 100 kHz
IMD	<–23 dBc @ 16 W PEP @ 100 kHz
Ruggedness	1 : 5 all phases
Return loss input	<–15 dB
2nd Harmonic	<–40 dBc @ 16 W

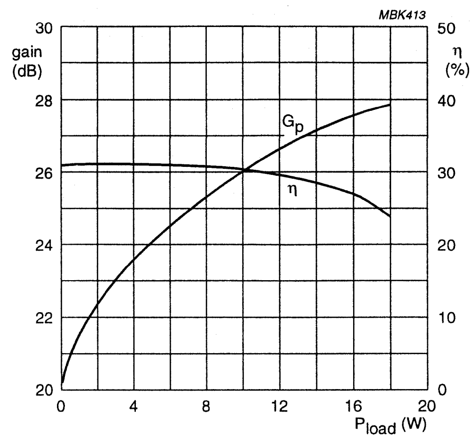


Fig.5 Gain and efficiency of BGY1816.

Due to it's compact size and high degree of integration, one saves valuable board space and keeps component costs and count down. Using an external pre-driver with this module a cheap and small line up can be designed for a micro cell or used as driver for a final amplifier.

5 FINAL STAGE (BLV2046)

As final stage the BLV2046 is used. The BLV2046 is a silicon NPN planar epitaxial transistor used in a class-AB common emitter configuration, capable of 50 W RF power with more than 8 dB gain and an efficiency larger than 40% in the 1 805 to 1 990 MHz band.

The transistor dies use a sub-micron interdigitated bipolar technology. To improve thermal stability and ruggedness, emitter ballasting resistors are used in combination with high breakdown voltages (typ. 80 V with open emitter).

The BLV2046 has internal input and output matching networks using MOS capacitors which allow an easier matching design for wide band circuits, and guarantee constant Q, gain performance and impedance behaviour during production. The TiPtAu top metallization ensures an excellent MTBF.

The encapsulation is a SOT460A package (22.9 × 6.3 mm) with a ceramic cap. The SOT460A (see Fig.6) is a non hermetic low cost package with very good thermal characteristics and low emitter inductance by means of metallized via holes.

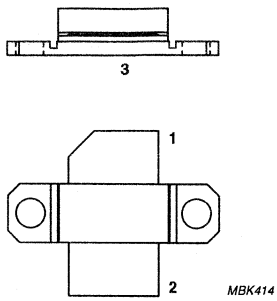


Fig.6 The SOT460A package.

To achieve the best compromise between gain expansion/linearity and efficiency, the BLV2046 is biased at 26 V with a quiescent current of 600 mA.

Summary of results:

Table 3 The results of the BLV2046

BLV2046	TYPICAL	CONDITIONS
Gain (dB)	8.5	at 50 W output power
Efficiency (%)	45	at 50 W output power
Gain expansion (dB)	<1	1805 to 1880 MHz
Gain ripple (dB)	<1	1805 to 1880 MHz
IMD (dBc)	–35	Pload = 50 W (PEP) @ Icq = 200 mA

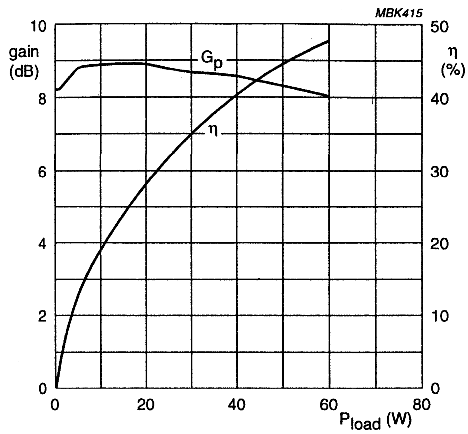


Fig.7 Gain and efficiency of the BLV2046.

The BLV2046 has proven to be a powerful single ended 50 W NPN silicon bipolar transistor as final stage to achieve a low cost, easy design, high efficiency and high gain amplifier. Although specified a 50 W transistor at 26 V supply, the transistor can easily generate 60 W of RF power with a (typical) gain of 8 dB and a (typical) efficiency of 45% into a 50 Ω load, see Fig.7.

6 FULL LINE-UP RESULTS

The full line up has been build on Rogers RT4000 series (32 mils), an epoxy based circuit board, closely resembling printed-circuit board used in the field. The line up exists of two boards one containing the pre-driver and driver, the second accommodates the final amplifier.

The two circuit boards are mounted on a brass base plate, which is mounted on a heat sink using forced air cooling.

As all inputs and outputs of the 3 stages are 50 Ω, the individual stages can easily be checked for performance or trouble shooting.

On the (pre)driver board a provision is made for a 5 V stabilising IC, powerful enough to feed the BGF425W, BGY1816 and the bias of the BLV2046.

During the tests the mounting base plate temperature was measured between 55 and 60 °C, T_{amb} = 24 °C.

As mentioned earlier, the line-up is a practically no tune design. To obtain maximum performance from the loading circuit of the BLV2046 one tuning capacitor has been used. Measurements of the output returnloss proved better then –10 dB.

Summary of results:

Table 4 The results of the total line-up

FULL LINE UP	RESULTS	CONDITIONS
Gain	>50 dB	Pload = 50 W
Efficiency	>36%	Pload = 50 W
ΔGain vs. frequency	<2 dB	1805 – 1880 MHz
ΔGain vs. Pload	<1 dB	Pload 1 – 50 W
Tmb	57 °C	T_{amb} = 25 °C
Return loss in	<–15 dB	Pload = 50 W
Return loss output	<–10 dB	
2nd Harmonic	<–35 dBc	

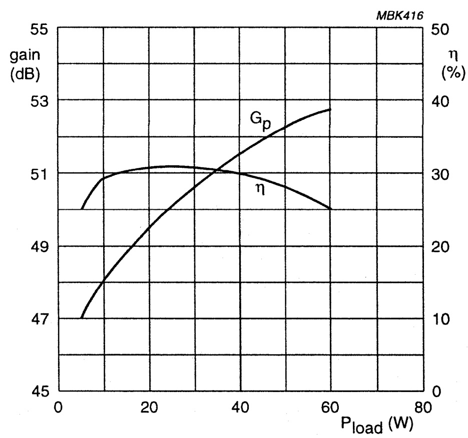


Fig.8 Gain and efficiency of the line-up.

7 CONCLUSION

A 50 W full line up base station amplifier has been presented for the PCS/DCS band. It has been proven that the line up can generate 50 W of RF output power with an overall gain larger than 47 dB with an overall efficiency of 36%. No instabilities were noticed in spite of the large gain. Gain flatness and gain expansion are smaller than 2 dB over the band and power range.

Using the combination BFG425W, BGY1816/BGY1916 and BLV2046 one can design a low cost PCS/DCS amplifier in a very short design cycle time. It is easy to manufacture, requires minimum tuning and small circuit board surface area.

8 LINE UP LAYOUT

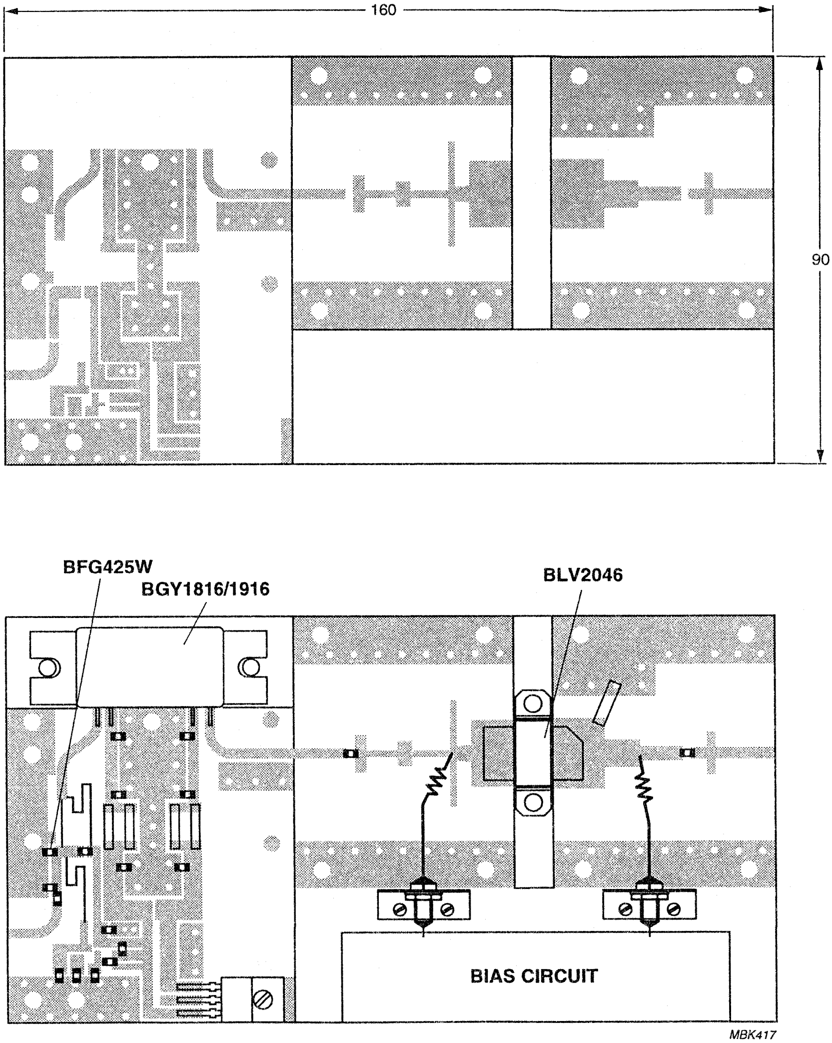


Fig.9 Layout of the line-up.

Remark: Fig.9 shows the layout of the 50 W line-up used to test the overall performance. It is meant as a demo-board, giving maximum flexibility for evaluation. For production the size of this board (160 × 90 mm) can easily be reduced by 50%.

MICROWAVE APPLICATIONS

APPLICATION NOTE

Broadband impedance matching for S-Band Transistors

Application Note
AN98029

1 INTRODUCTION

Due to fact that no accurate model or S-parameters exist which describe RF power transistors, the design of RF power amplifiers is often done in an empirical way. Not only is this method very time consuming, but it also means that it is at least doubtful whether the optimum performance of the transistor is obtained, especially when broadband matching is required. In this paper a method of designing an input and output matching circuit for a broadband power transistor operating in the low S-band (2.7 – 3.1 GHz) is described. The design and evaluation of the transistor is left out in this paper.

2 DESIGN METHOD

The whole design can be separated into the design and evaluation of the input and output circuit. This is done in the same way for both circuits. The following steps can be distinguished:

- Impedance measurement
- Fit impedance data to an appropriate model
- Design of lumped element input and output circuit
- Translation of lumped element to stripline
- Evaluation of stripline circuit with CAD-tools.

In the following each step will be discussed separately.

3 IMPEDANCE MEASUREMENT

The first step is to measure the impedance at nominal output power. This is done by tuning the device with slugtuners at the input and output to maximum output power and minimum reflection at the input with gradually increased input power. In Fig.1 the impedance measurement test set up is depicted.

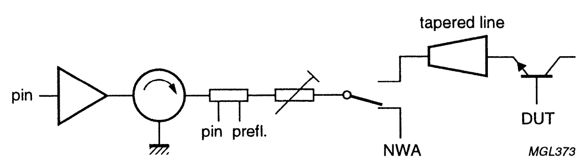


Fig.1 Impedance measurement set up.

In Fig.1 it can be seen that not the actual input impedance is measured, but the source-impedance. The input impedance is the complex conjugated of this source-impedance. This may be done under the assumption that minimum input reflection is achieved when source and load are complex conjugated. For the output the load impedance is directly measured. Also in Fig.1 it can be seen that between tuner and device a tapered line is connected. With this tapered line the relatively low impedance of the devices is transformed to a higher value thus ensuring that with the tuners all required impedance's can be obtained. This is especially required with high power devices where the slugtuners cannot handle a high VSWR. In the network analyzer the S-parameters of the tapered line are stored and the measured data is recalculated for the transformation of the tapered line. During deembedding of the tapered circuit the following errors can be introduced:

- Reference plane is not accurately defined
- Launcher is very thin compared to the lead of the transistor. This introduces a discontinuity (step in width) which can cause a large error.

The errors introduced may be as large as j6 Ω at 3 GHz. The Philips Data Handbook contains values for the input and load impedance of the transistor which are corrected for these errors.

4 FITTING DATA TO MODEL

Although no accurate two-port models exist to describe the transistor completely, simple equivalent one-port models which describe the input and output impedance of the transistor can be used to enable the use of CAD-Tools in the design of the matching circuit. In Fig.2 the model for the input of the transistor based on the internal matching topology is depicted in Fig.3 measured and fitted data are given in the Smith Chart. From the relation $B = \frac{f_0}{Q}$ it can be seen that for a large bandwidth a low Q-transformation at all stages is required. To evaluate this the one-port model proves to be a useful tool. The bandwidth limitations of the intrinsic transistor are dominated by the input rather than by the output. This also can be found in the transistor model. In the model the active die is represented by R_{DIE}. The first (internal) matching stage is formed by the first emitter bondwire (L_{E1}) and the prematch capacitor (C_{PRE}). L_{E2} represents the bondwire connecting die and prematch to the lead. L_P, C_P and L_{PAR} are parasitic elements caused by the header.

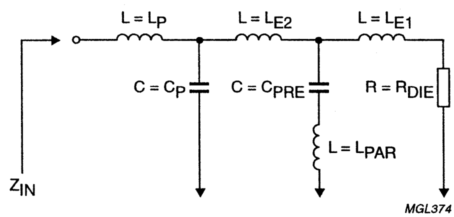


Fig.2 Input equivalent model.

Apart from bandwidth considerations, the location of the resonance frequency of the first matching stage at the input and of the resonance frequency of the internal shunt inductance (inshin) at the output also have a large influence on gain and efficiency. More on this subject can be found in Pitzalis[1]

(1) *"broad-band Microwave Class-C Transistor Amplifiers"*, Pitzalis and Gilson; IEEE Transactions on Microwave Theory and Techniques, November 1973.

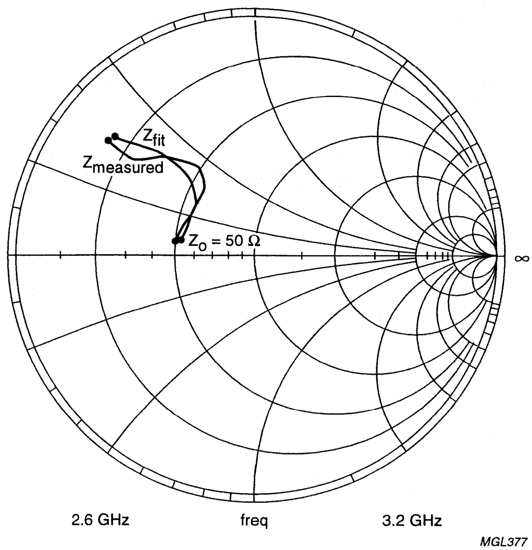


Fig.3 Measured and fitted data.

In Fig.4 the model of the output is given. Here the die is represented by a single resistor in combination with a capacitor which represents the output capacitance of the active die. The die is connected to the lead by means of L_{C1} and L_{C2}. The point of impact of the internal shunt inductance (L_{INS}) determines the ratio between L_{C1} and L_{C2}. C_{DC} is a DC-decoupling capacitor and C_{PAR} is modelling the parasitic capacitance caused by the header.

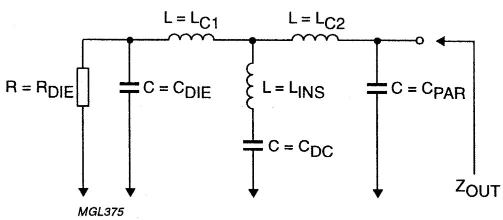


Fig.4 Output model.

A second method in designing the matching circuit is to use the measured data in a dataset. This has the disadvantage that inconsistency in data will have a larger influence than when a model is used.

A second advantage of the use of a model is that this gives the possibility to evaluate the influence of production spread of each parameter on the performance (e.g. Γ_{IN}).

5 LUMPED ELEMENT INPUT AND OUTPUT CIRCUIT

Before designing the input and output circuit with stripline techniques it is preferred to synthesize a low pass lumped element prototype first. The advantage of using a lumped element model first is:

- Optimum solution easier and faster found with CAD-Tools
- Better insight in feasibility of found solution. High inductance are very difficult to realize in stripline techniques. An inductance may also converge to zero (or negative values) indicating that the given low pass structure is not appropriate.

Similar to the requirements for the internal matching network, the external matching circuit (see Fig.5) must also be a low Q design to ensure broadband performance of the device.

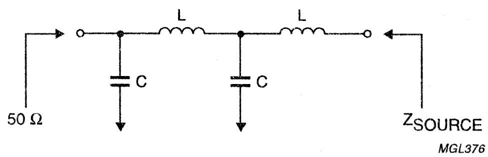


Fig.5 Lumped element model input circuit.

After having found the optimum values for the lumped elements, these can be translated to stripline elements.

This is done by using the basic formula's[1] to find the initial values for stripline circuit which then can be optimized with CAD-tools.

(1) A very good description of microstrip matching networks can be found in: *"Microwave Transistor Amplifiers"*, Guillermo Gonzalez.

6 EVALUATION OF STRIPLINE CIRCUIT

Although stripline models used in CAD-tools such as MDS are fairly accurate, they still have their limitations (such as steps, crosses and substrate thickness). To examine whether these limitations de not mask any significant errors in the design a field simulator can be used (e.g. Momentum). The output of such a simulator is a datafile containing the S-parameters of the stripline circuit. In order to prevent the introduction of additional errors in the simulator output, special attention should be paid to the following:

- Use the appropriate port definition and location of the reference plane. Be aware of any unexpected steps in width at the edge of the simulated circuit.
- Make sure that the MESH is sufficiently small, especially at discontinuities.
- Use a sufficient number of frequency points.

With the combination of simulator output and transistor model an accurate idea of the performance of the transistor in the matching circuit can be obtained without having to go through the time and money consuming process of ordering and assembling printed-circuit boards. When measuring the printed-circuit board with a network analyzer it should be noted that an error can be made due to the difference in width between printed-circuit board and launcher (see Chapter 3). In Fig.6 the input reflection can be seen of the BLS2731-10 in a 50 Ω matching circuit. Both measured and simulated data show a similar curve, only the minimum value is reached at a different frequency. this difference between measured and simulated curve can be explained by the following:

- Small air gaps between reference plane of transistor and edge of printed-circuit boards.
- Impedance data used in the design of the printed-circuit board is from an average device. The measured device may differ from average due to normal production spread.
- Placing components such as DC-blocking.
- Influence bias circuit.
- Connectors not incorporated in simulation.

Also in Fig.6 it can be seen that excellent matching is achieved over the entire frequency band from 2.7 – 3.1 GHz. For the output a similar performance is found.

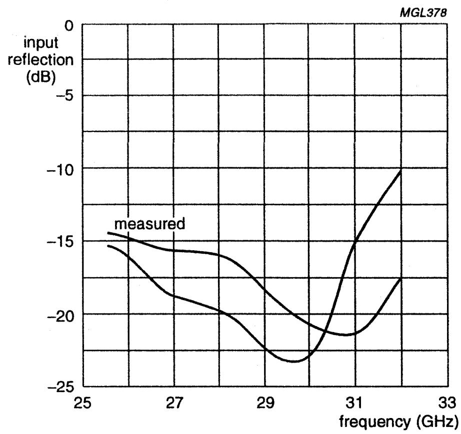


Fig.6 Measured and simulated input reflection of BLS2731-10.

7 CONCLUSIONS

Although the lack of an accurate model for S-band high power transistors would suggest that the use of CAD-tools in the design of matching circuits is impossible, it is shown that with the use of the impedance data from the data handbook and a simple model for the input and output impedance an excellent matching can be achieved. This enables RF-engineers not only to design and evaluate printed-circuit board much faster, but also over a much larger bandwidth.

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Data handbook system

DATA HANDBOOK SYSTEM

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